20W High Performance, Single Synchronous Step-Up Converter

General Description

The uP6018Q is a high-efficiency, single synchronous boost converter suitable for up to 20W applications in Power Bank and E-Cigarette. The proprietary RCOT$_{TM}$ technology provides fast transient response and high noise immunity. It supports ceramic output capacitors. This combination is ideal for building modern low duty ratio, untra-fast load step response DC-DC converters. The output voltage ranges from 4V to 15V, and the conversion input voltage ranges is from 3V to 5.5V. The switching frequency is fixed 450kHz. It is available in a space saving WQFN4x4-32L package.

Ordering Information

Order Number	Package Type	Remark
uP6018QQMI	WQFN4x 4-32L	

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.
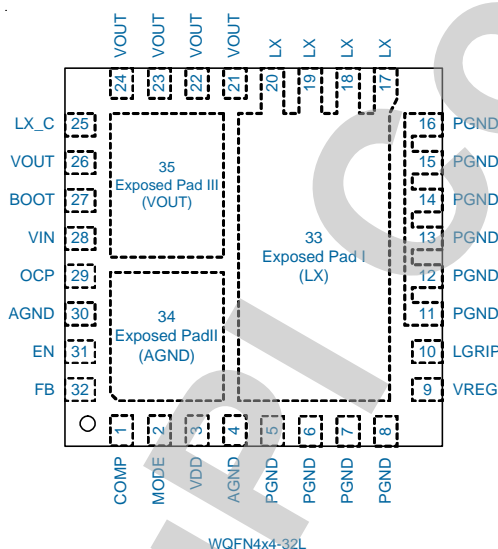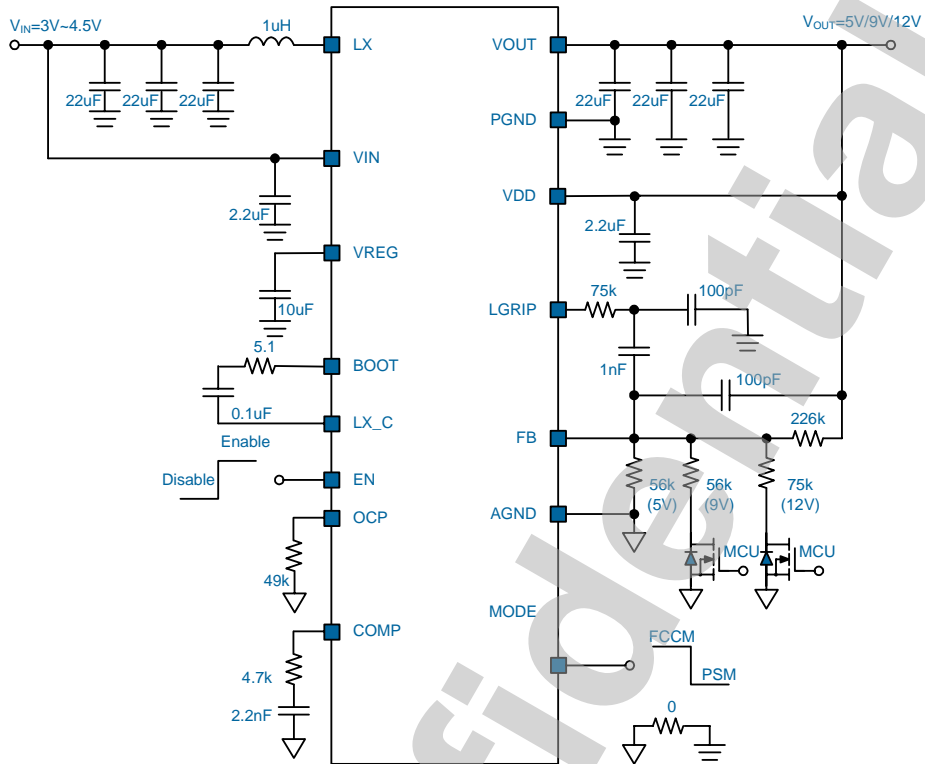
Features

☐ **Wide Input Voltage Range: 3V to 5.5V**

☐ **Output Voltage Range: 4V to 15V**

☐ **Wide Output Load Range: Up to 20W**

☐ **Built-In 1% 1V Reference**

☐ **Built-In LDO Linear Voltage Regulator**

☐ **RCOT$_{TM}$ (Robust Constant On-Time) Control Architecture**

☐ **450kHz Switching Frequency**

☐ **4000ppm/°C R$_{DS(ON)}$ Current Sensing**

☐ **8ms Soft Start**

☐ **Built-in OVP/UVP/OCP/OTP**

☐ **WQFN4x4-32L Package**

☐ **RoHS Compliant and Halogen Free**

Applications

☐ **Portable Charging Devices**

☐ **Power Bank**

☐ **I/O Supplies**

☐ **System Power Supplies**

Pin Configuration

WQFN4x4-32L

Typical Application Circuit

V_{IN}=3V~4.5V 1uH LX

22uF 22uF 22uF

VIN

2.2uF

VREG

10uF

5.1 BOOT

0.1uF LX_C

Enable

Disable EN

OCP

49k

COMP

4.7k

2.2nF

VOUT V_{OUT}=5V/9V/12V

22uF 22uF 22uF

PGND

VDD

2.2uF

75k 100pF LGRIP

1nF 100pF

FB 226k

56k 56k 75k
(5V) (9V) (12V)

AGND MCU MCU

MODE

FCCM

PSM

0

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	COMP	**Boost Converter Compensation.** Connect a compensation network to ground.
2	MODE	**Operation mode selection pin for the device in light load condition.** When this pin is connected to ground, the device works in forced Pulse-Skip mode. When this pin is pulled high, the device works in Force CCM mode.
3	VDD	**Converter Power Supply Input.** This pin provides bias voltage for the IC and powers the internal 5V linear regulators. Connect this pin to VOUT and bypass it with an R/C filter.
4,30,34	AGND	**Signal Ground.** Connect the return of all small signal components to this pin.
5,6,7,8,11,12, 13,14,15,16	PGND	**Converter Power GND Pin.**
9	VREG	**5V LDO Output and Gate Drive Supply Voltage Input.**
10	LGRIP	**Low Side Gate Driver Ripple Injection.** Connect a series RC form LGRIP to GND and FB to compensate the control loop.
17,18,19,20,33	LX	**Internal Switches Output.** Connect this pin to the output inductor.
21,22,23,24,26,35	VOUT	**Converter Output Pins.** Bypass output voltage with a minimum 22uFx3 ceramic capacitor.
25	LX_C	**Internal Switches Output.** Connect the bootstrap capacitor C_{BOOT} to BOOT pin.
27	BOOT	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver.** Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the LX_C pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC. Externally connected to VREG with a Schottky diode via bootstrap MOSFET switch.
28	VIN	**Power Supply Input.** Input voltage that supplies current to the output voltage.
29	OCP	**Over Current Protection Setting.** Connect a resistor from this pin to GND to set the over current protection level.
31	EN	**Chip Enable.** Short to GND to disable the device.
32	FB	**Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.

Functional Block Diagram
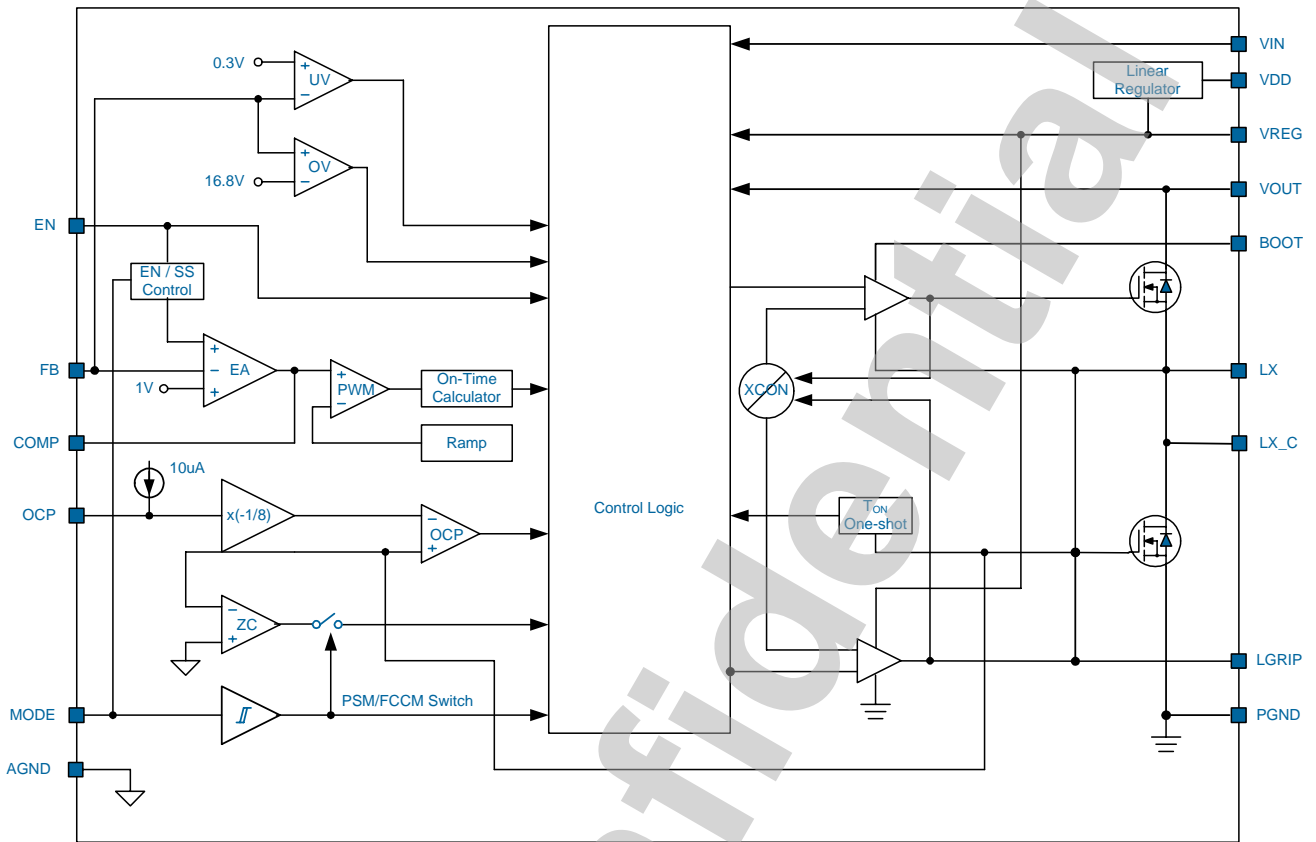
The uP6018Q implements a unique RCOT$_{TM}$ control topology for the synchronous boost. The RCOT$_{TM}$ supports extremely low ESR output capacitors and makes the design easier and robust. The output voltage ranges from 4V to 15V. The conversion input voltage ranges from 3V up to 5.5V.

Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The uP6018Q has a MODE pin to select between Force CCM and Pulse-skip for light load conditions. The strong gate drivers allow low R$_{DS(ON)}$ FETs for high-current applications.

Enable and Soft Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.8V), the converter enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5V at the VREG pin. In the second phase, an internal DAC starts ramping up the reference voltage from 0V to 1V. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

On-Time Control and Frequency

The uP6018Q does not have a dedicated oscillator that determines switching frequency. However, the device runs with pseudo-constant frequency by feed-forwarding the input and output voltages into its on-time one-shot timer. The RCOT$_{TM}$ control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage. This makes the switching frequency fairly constant in steady state conditions over wide input voltage range.

The off-time is modulated by a PWM comparator. The FB node voltage (the mid-point of resistor divider) is compared to the internal 1V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off-time is extended until the current level falls below the threshold.

Light Load Condition in Pulse-Skip Operation

While the MODE pin is connected to ground, uP6018Q automatically reduces the switching frequency at light load conditions to maintain high efficiency. This reduction of the frequency is achieved smoothly and without increasing VOUT ripples or load regulation. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than requires the next ON cycle.

The transition pin from discontinuous to continuous conduction mode can be calculated as:

$$I_{OUT} = \frac{1}{2 \times f_{OSC} \times L_{OUT}} \times \frac{V_{IN}^2}{V_{OUT}} \times (1 - \frac{V_{IN}}{V_{OUT}})$$

Over Current Limit

the uP6018Q monitors the inductor peak current by low side MOSFET R$_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than V$_{OCSET}$. When triggered, the over current limit will keep low side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level and consequently causes V$_{OUT}$ to decrease faster until UVP occurs and shuts down the uP6018Q.

The peak current limit threshold is set by connecting a resistor from OCP to GND. The OCP pin will sink a 10uA current source and create a voltage drop across R$_{CS}$ as the V$_{OCSET}$. V$_{OCSET}$ = 10uA x R$_{OCP}$. When the voltage drop across the low side MOSFET equals the voltage across the setting resistor, the peak current limit will be activated.

The voltage across LX and GND pins is compared with V$_{OCSET}$ for current limit. The peak current limit level is calculated as:

$$I_{PEAK\_LIM} = \frac{V_{OCSET}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where I$_{RIPPLE}$ is the peak-to-peak inductor ripple current at steady state.

Over Voltage/Under Voltage Protection

The uP6018Q monitors output voltage to detect over voltage and under voltage. When the output voltage becomes higher than 14.5V, the OVP is triggered, low side MOSFET is off and the high side MOSFET is on. When the feedback voltage is lower than 0.3V, the UVP is triggered, then high side MOSFET and low side MOSFET are latched. This function is enabled after 5ms following EN has become high.

UVLO Protection

The uP6018Q uses VIN under voltage lockout protection (UVLO). When the VIN voltage is lower than the UVLO threshold voltage, the switch mode power supply shuts off. This is non-latch protection.

Over Temperature Protection

The uP6018Q monitors the temperature of itself. If the temperature exceeds typical 130°C, the uP6018Q will be turned off. This is the non-latch protection. It will be recovered once temperature is lower than 100°C.

Absolute Maximum Rating

(Note 1)

Supply Voltage, VOUT and VDD -- -0.3V to +26V

LX Pin Voltage to GND --- -0.3V to (VOUT+ -0.3V)

BOOT Pin Voltage -- $-V_{LX}$-0.3V to V_{LX}+6V

VIN and VREG Pin Voltage --- -0.3V to +6V

Other Pins to GND --- -0.3V to +6V

Storage Temperature Range --- -55°C to +150°C

Lead Temperature (Soldering, 10 sec) --- 260°C

ESD Rating (Note 2)

    HBM (Human Body Mode) --- 2kV

    MM (Machine Mode) --- 200V

Thermal Information

Package Thermal Resistance (Note 3)

    WQFN4x4-32L $\theta_{JA, controller}$ --- 54°C/W

    WQFN4x4-32L $\theta_{JA, HS}$ --- 42°C/W

    WQFN4x4-32L $\theta_{JA, LS}$ --- 38°C/W

    WQFN4x4-32L $\theta_{JC, controller}$ --- 21°C/W

    WQFN4x4-32L $\theta_{JC, HS}$ --- 10°C/W

    WQFN4x4-32L $\theta_{JC, LS}$ -- 6°C/W

Power Dissipation, P_D @ T_A = 25°C

    WQFN4x4-32L $P_{D, controller}$ --- 1.85W

    WQFN4x4-32L $P_{D, HS}$ --- 2.38W

    WQFN4x4-32L $P_{D, LS}$ --- 2.63W

Recommended Operation Conditions

(Note 4)

Input Voltage, V_{IN} -- 3V to 5.5V

Output Voltage, V_{OUT} --- 4V to 13V

Output Load, P_{OUTmax} -- 20W

Operating Junction Temperature Range --- -40°C to +125°C

Operating Ambient Temperature Range -- -40°C to +85°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{DD} = 5V, T_A =25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Power Supply							
VIN UVLO Threshold	$V_{UVLOVIN}$	Rising		2.83	2.9	2.97	V
		Hysteresis		0.15	0.2	0.25	V
VIN Supply Current	I_{VIN}	V_{EN} = 5V, V_{FB} =1.1V, I_{OUT} = No Load		--	360	--	uA
VDD Supply Current	I_{VDD}	V_{EN} = 5V, V_{FB} =1.1V, I_{OUT} = No Load		--	0.6	1	mA
VIN Shutdown Current	I_{VIN_SD}	V_{EN} = 0V, I_{OUT} = No Load		--	--	10	uA
VDD Shutdown Current	I_{VDD_SD}	V_{EN} = 0V, I_{OUT} = No Load		--	--	1	uA
Internal Reference Voltage							
Feedback Voltage	V_{FB}	CCM condition, T_A = 25°C		0.99	1	1.01	V
VFB Input Current	I_{FB}	V_{FB} = 1V, T_A = 25°C		--	0.01	0.2	uA
VFB of VOUT Discharge	V_{FB_DIS}	VOUT discharge		--	1.1	--	V
		Hysteresis		--	0.05	--	
Power Switches							
Upper Switch Resistance	$R_{UG,DSON}$			--	17.7	--	mΩ
Lower Switch Resistance	$R_{LG,DSON}$			--	6	--	mΩ
Duty and Frequency Control							
Minimum Off-ime	T_{OFF_MIN}	V_{IN} = 3.6V, V_{OUT} = 5V		--	700	--	ns
Minimum On-Time	T_{ON_MIN}	V_{IN} = 3.6V		--	240	--	ns
Frequency	F_{SW}	V_{IN} = 3.7V, V_{OUT} = 9V@CCM		--	450	--	kHz
Soft Start							
Soft Start Time	T_{SS}	From VEN high to VOUT = 95%		--	8	--	ms
Logic Threshold							
EN Pin Threshold Voltage	V_{EN}	Enable		1.8	--	--	V
		Disable		--	--	0.5	
On-Time	T_{ON}	R_{RT} = open, f_{LX} = 450kHz V_{IN} = 3.7V, V_{OUT} = 9V, I_{OUT}= No Load		--	1.22	--	us
EN Input Current	I_{EN}	VEN = 5V		--	--	1	uA
Protection: Current Sense							
OCP Source Current	I_{CS}	V_{OCP} = 1V		9	10	11	uA
		Temp coef		--	4000	--	ppm/°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection: UVP and OVP						
OVP Threshold Voltage	V_{OVP}	Percentage of V_{DD}	15.3	16.8	18.3	V
UVP Threshold Voltage	V_{UVP}	Percentage of V_{FB}	--	0.3	--	V
UVP Propagation Delay Time	T_{UVPDEL}		--	3.3	--	ms
Output UVP Delay Time	T_{UVPEN}	From Enable to UVP Workable	--	13.5	--	ms
VREG LDO Voltage						
LDO Output Voltage	V_{REG}		4.625	5.0	5.375	V
LDO Output Current	I_{REG}		--	--	50	mA
LDO Drop Out Voltage	V_{DROP}	VDD = 4.5V, I_{REG} = 20mA	--	300	--	mV
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SDN}	Shutdown Temperature	--	130	--	°C
		Hysteresis	--	30	--	°C

This page is intentionally left blank and will be updated when data is available.

Setting Output Voltage

The output voltage is set by an external resistor divider. With the given feedback voltage, VFB, and feedback bias current, IFB, the voltage divider can be calculated as:
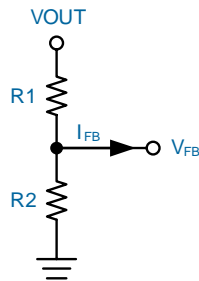
$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

The internal VREF is 1V with 1% accuracy.

Component Selection

External component selection begins with inductor value selection based on the considerations of the output voltage, output current, and the maximum/minimum input voltages.

Inductor Selection

Inductor selection should consider the inductor value, rated current, DCR, size, core material, and cost. The inductor value is selected based on the consideration of inductor ripple current and the inductor rated saturation current should be higher than the peak current at maximum load. The inductor should have low core loss at 450kHz and low DCR for better efficiency. Depending on the application, the inductor values 1uH is recommended.

Input Capacitor Selection

For better input voltage filtering, the low ESR of capacitor is highly recommended. The VIN pin is the power supply for the uP6018Q. A 2.2uF ceramic bypass capacitor is recommended as close as possible to the VIN pin of the IC. The VREG pin is the output of the internal LDO. A ceramic capacitor of more than 1uF is required at the VREG pin to get a stable operation of the LDO. For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is needed to have large input capacitance to make the input voltage ripple less. It is recommended to use three 22uF X5R or X7R type ceramic capacitors for most applications.

Output Capacitor Selection

For small output voltage ripple, it is recommends a low-ESR ceramic capacitor. To use three 22uF ceramic output capacitors work for most applications is recommended. Larger capacitor values can be used to improve the load transient response. Take care when evaluating a capacitor¡¦s de-rating under DC bias. The bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, reserve margin on the voltage rating to ensure adequate effective capacitance.
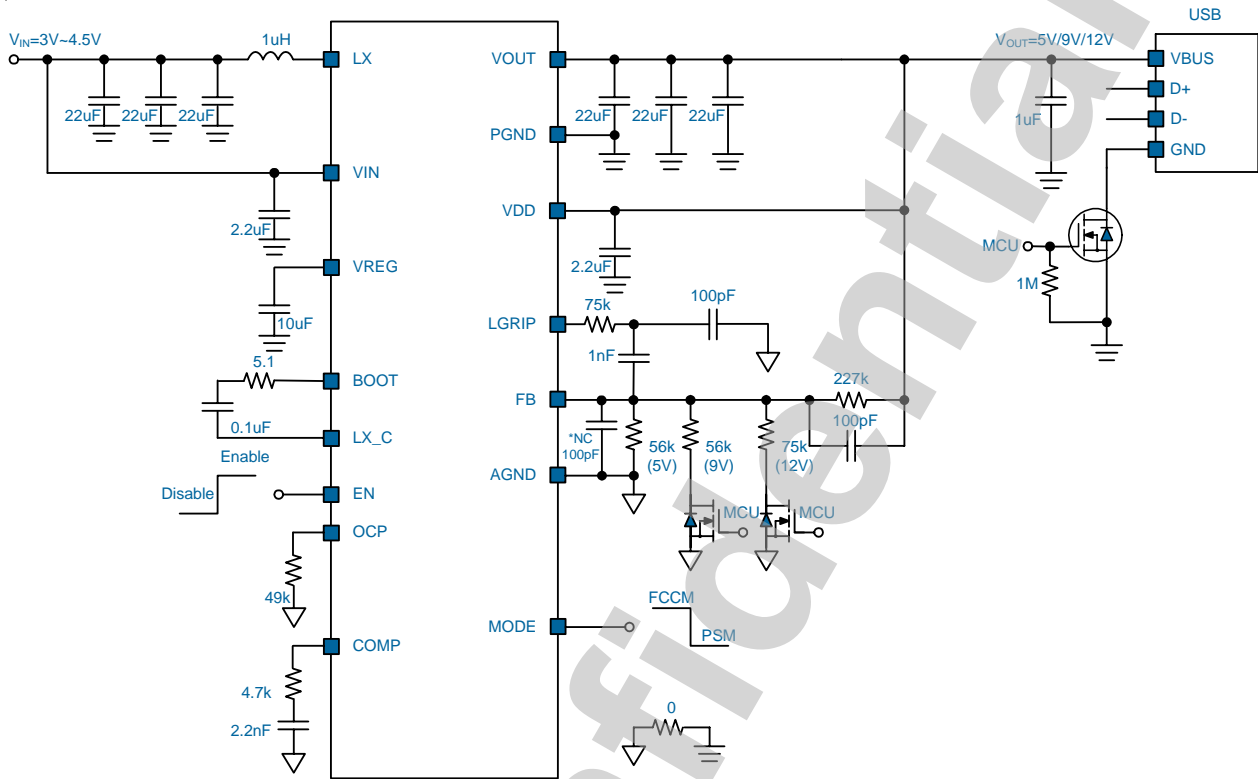
From the required output voltage ripple, the output ripple voltage can be calculated as:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

Where f_{SW} = switching frequency, C_{OUT} = output capacitance and ΔI_L = inductor ripple current, ESR = equivalent series resistance of the used output capacitor.

Application Circuit with True Output Short Protection
With external N-MOSFET control

*Fb pin reserve a 0402 MLCC cap to AGND, default NC.

Layout Consideration

For best performance of the uP6018Q, the following guidelines are recommended.

1. Input and output capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.

2. The GND should be connected to a strong ground plane for heat sinking and noise protection.

3. Keep the main current traces as short and wide as possible.

4. LX node of DC-DC converter is with high frequency voltage swing. To prevent radiation of high frequency noise, the inductor should be placed close to the IC.

5. Please keep VIN, FB, LGRIP and OCP trace away from the noise source such as LX node and place C_{VIN} close to the IC and connected to ground plane to reduce supply ripple.

6. Place the feedback components as close as possible to the IC and keep away from the noise source.

7. Since the uP6018Q is high performance converter and also running high currents, the layout should be consideration of the thermal as well. A thermal pad improves the thermal capabilities of the package, please soldered exposed pad to the large plate.

8. The exposed pad III(VOUT) have the most heating of the IC (shown as figure1), please increase VOUT copper plane as wide as possible to get better thermal performance.
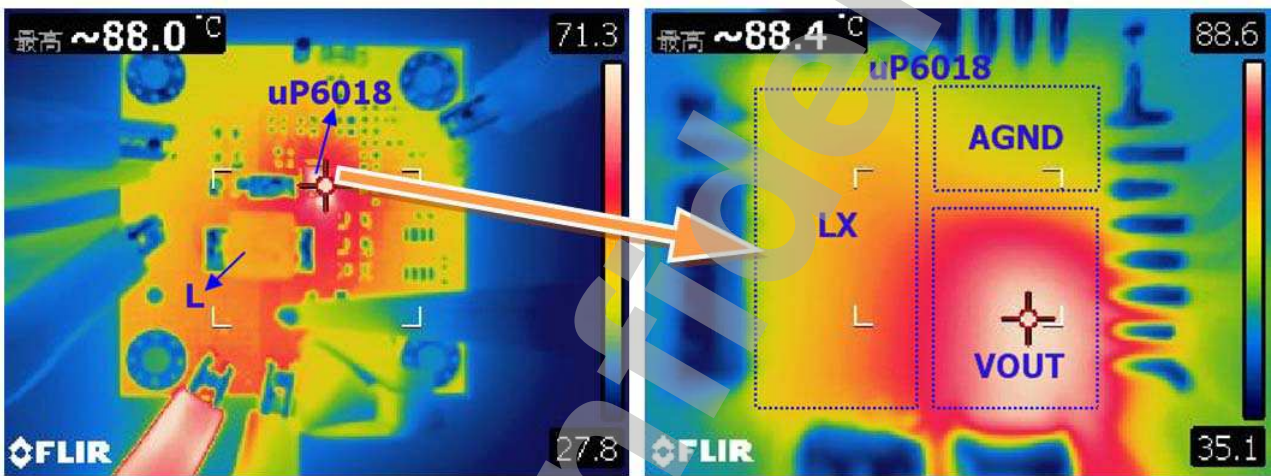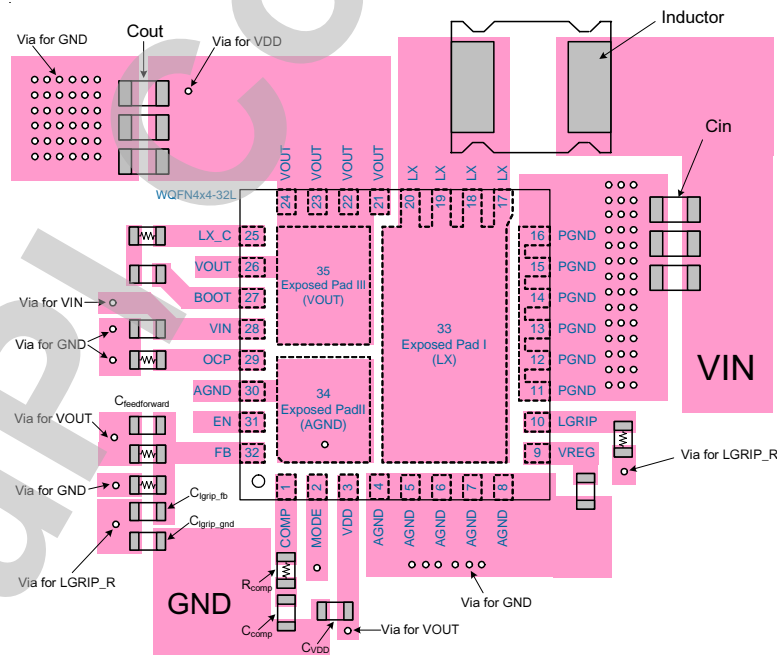

Figure 1. Thermal Image

Figure 2. Layout Reference of WQFN4x4-32L

Package Information

WQFN4x4 - 32L

Pin 1 mark

Bottom View - Exposed Pad

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the taerms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use or application of any product or circuit; nor for any infringements of patents or other rights of third parties which may result from its use or application, including but not limited to any consequential or incidental damages. No uPI components are designed, intended or authorized for use in military, aerospace, automotive applications nor in systems for surgical implantation or life-sustaining. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

COPYRIGHT (c) 2015, UPI SEMICONDUCTOR CORP.

uPI Semiconductor Corp.

Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666   FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062   FAX : 886.2.8751.5064