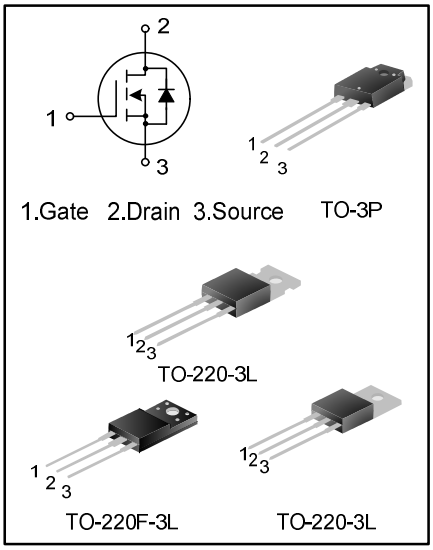
13A, 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF13N50T/F/PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

This device is widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 13A, 500V, $R_{DS(on)(typ.)}$= 0.44Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF13N50F	TO-220F-3L	SVF13N50F	Pb free	Tube
SVF13N50T	TO-220-3L	SVF13N50T	Pb free	Tube
SVF13N50PN	TO-3P	13N50	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVF13N50T	SVF13N50F	SVF13N50PN	
Drain-Source Voltage		V_{DS}	500			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	13			A
	T_C=100°C		8.2			
Drain Current Pulsed		I_{DM}	52			A
Power Dissipation(T_C=25°C)		P_D	190	51	218	W
- Derate above 25°C			1.52	0.41	1.74	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	663			mJ
Operation Junction Temperature Rating		T_J	-55～+150			°C
Storage Temperature Rating		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF13N50T	SVF13N50F	SVF13N50PN	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.66	2.45	0.57	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain –Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V，I_D=250μA	500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V，V_{GS}=0V	--	--	1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V，V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}，I_D=250μA	2.0	--	4.0	V
On State Resistance	$R_{DS(on)}$	V_{GS}=10V，I_D=6.5A	--	0.44	0.52	Ω
Input Capacitance	C_{iss}	V_{DS}=25V，V_{GS}=0V，f=1.0MHZ	--	1340	--	pF
Output Capacitance	C_{oss}		--	170	--	
Reverse Transfer Capacitance	C_{rss}		--	13.0	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=250V，I_D=13A，R_G=4.7Ω，V_{GS}=10V (Note 2,3)	--	25.53	--	ns
Turn-on Rise Time	t_r		--	48.80	--	
Turn-off Delay Time	$t_{d(off)}$		--	72.33	--	
Turn-off Fall Time	t_f		--	40.27	--	
Total Gate Charge	Q_g	V_{DS}=400V，I_D=13A，V_{GS}=10V (Note 2,3)	--	29.5	--	nC
Gate-Source Charge	Q_{gs}		--	8.00	--	
Gate-Drain Charge	Q_{gd}		--	12.3	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	13	A
Pulsed Source Current	I_{SM}		--	--	52	
Diode Forward Voltage	V_{SD}	I_S=13A，V_{GS}=0V	--	--	1.3	V
Reverse Recovery Time	T_{rr}	I_S=13A，V_{GS}=0V，dI_F/dt=100A/μS (Note 2)	--	495	--	ns
Reverse Recovery Charge	Q_{rr}		--	5.0	--	μC

Notes:

1. L=30mH, I_{AS}=7.5A, V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

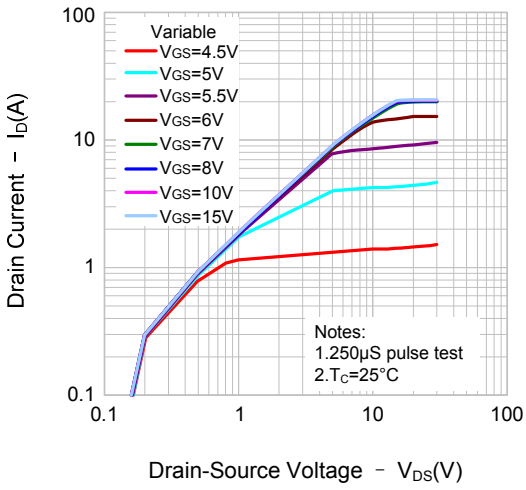


Figure 2. Transfer Characteristics

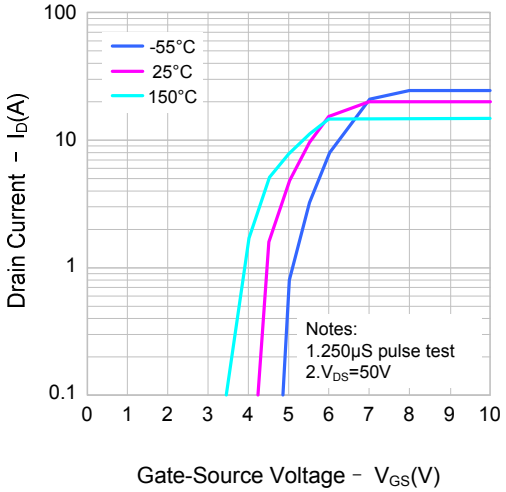


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

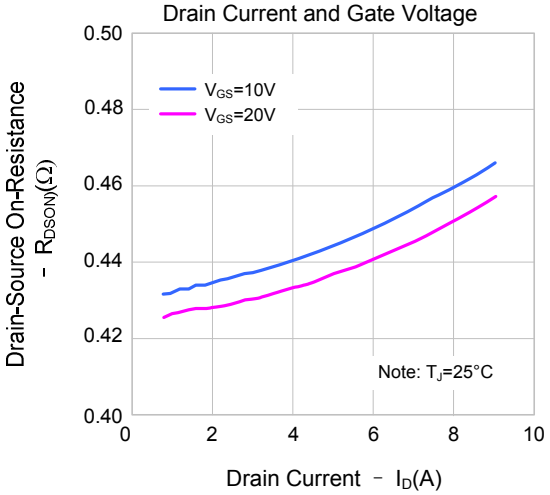
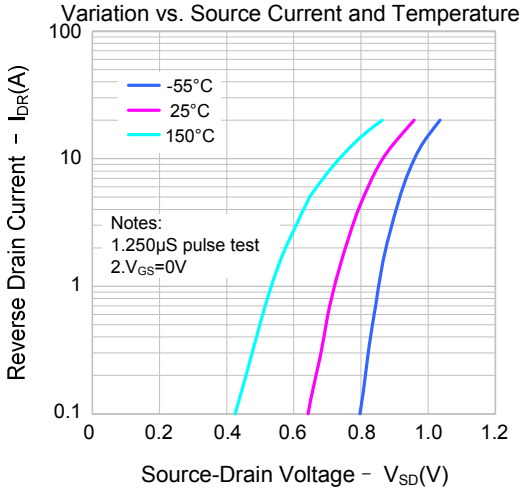


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

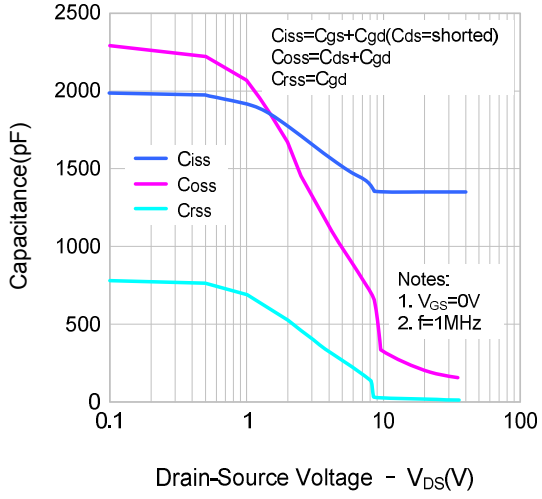


Figure 6. Gate Charge Characteristics

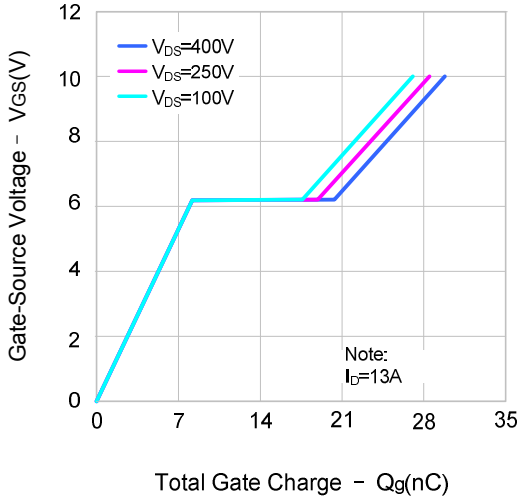


Figure 7. Breakdown Voltage Variation vs. Temperature

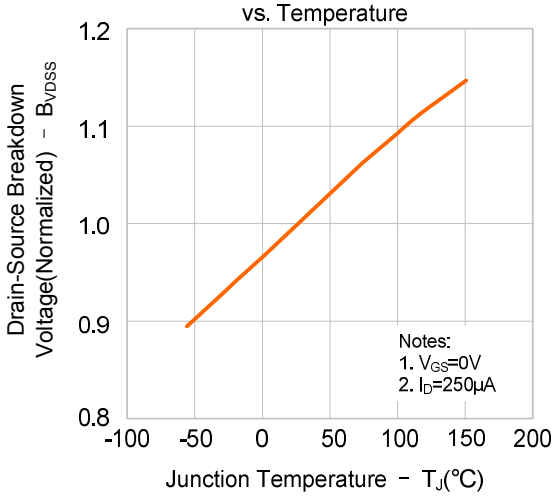


Figure 8. On-resistance Variation vs. Temperature

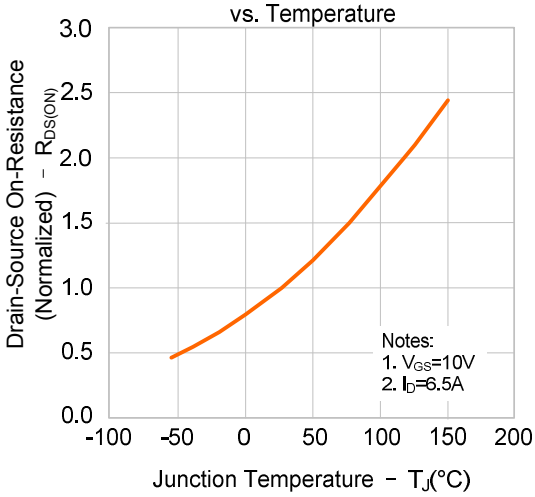


Figure 9-1. Max. Safe Operating Area(SVF13N50T)

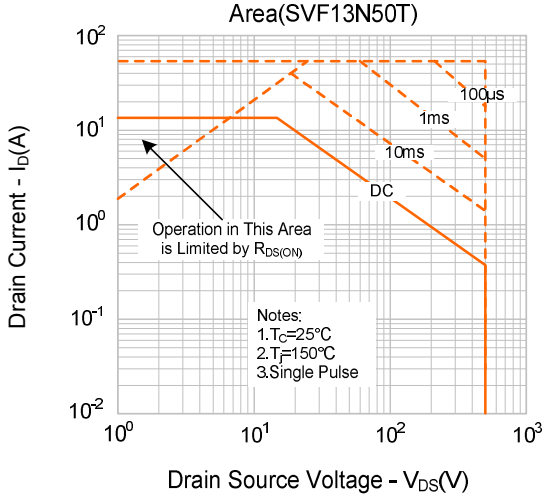
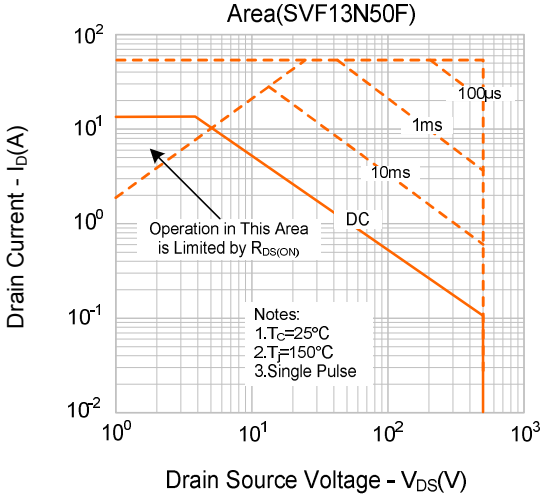


Figure 9-2. Max. Safe Operating Area(SVF13N50F)



TYPICAL CHARACTERISTICS(continued)

Figure 9-3. Max. Safe Operating Area(SVF13N50PN)

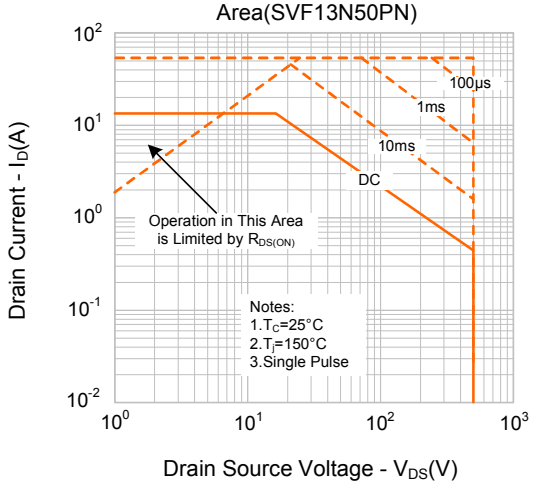
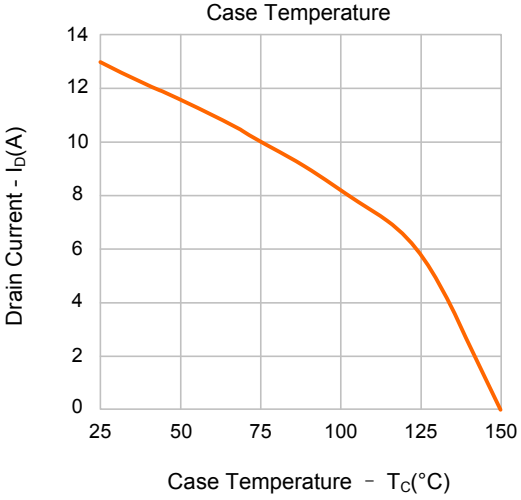
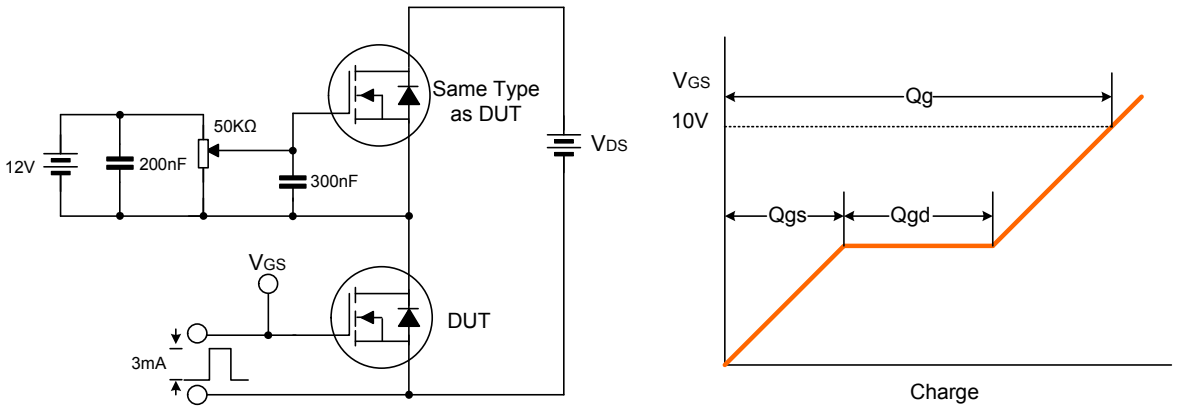


Figure 10. Maximum Drain Current vs. Case Temperature

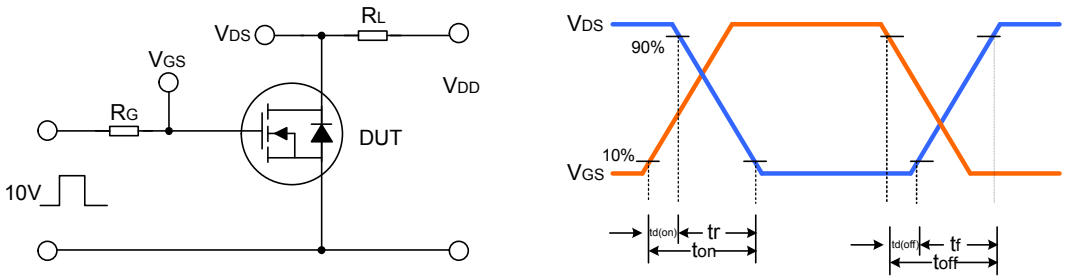


TYPICAL TEST CIRCUIT

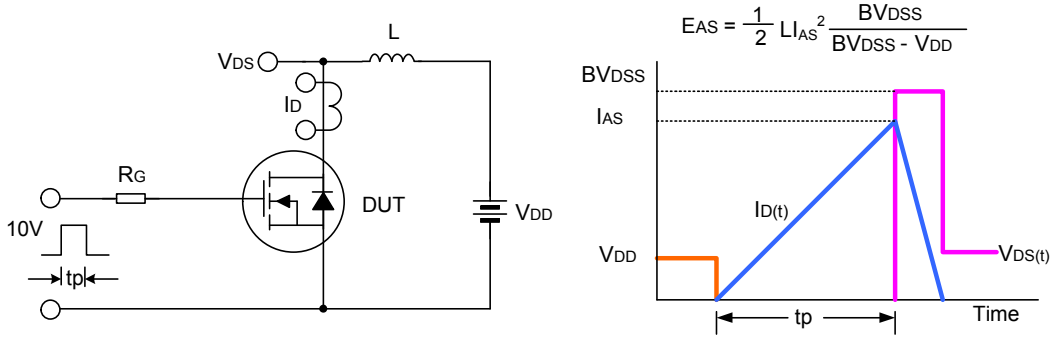
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



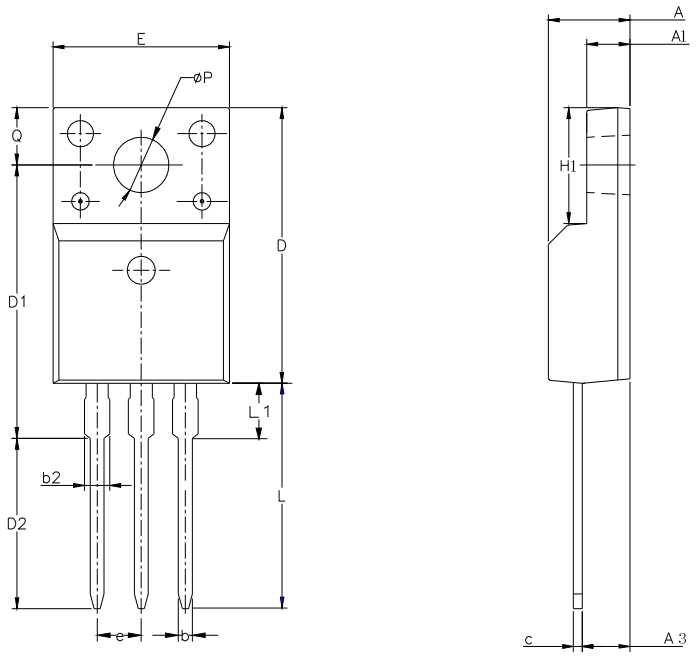
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220F-3L

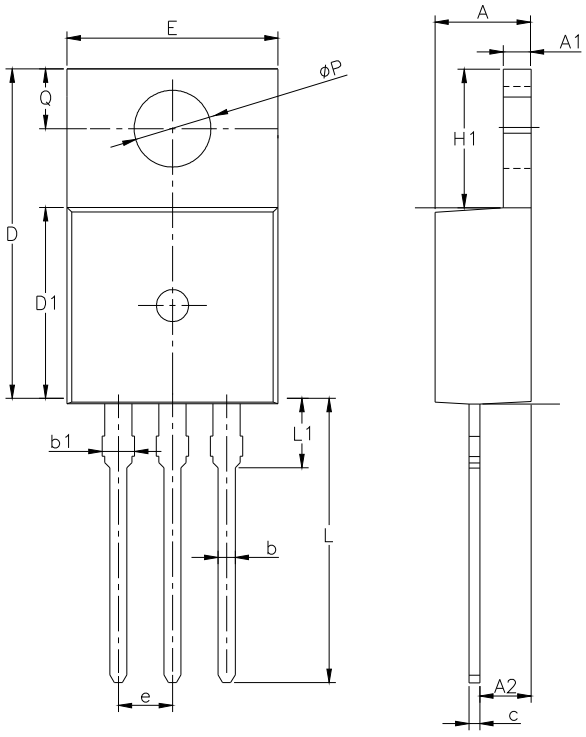
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
øP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-220-3L

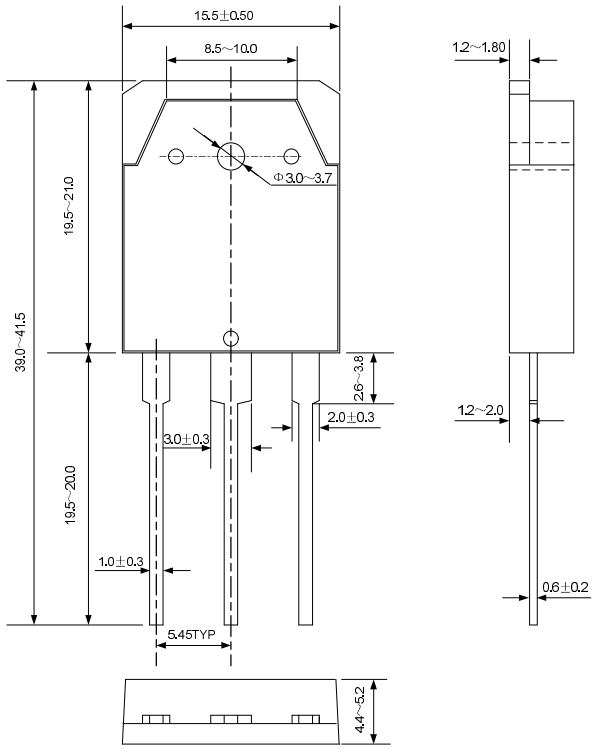
单位: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
øP	3.40	3.70	3.90
Q	2.60	—	3.20

PACKAGE OUTLINE

TO-3P **UNIT: mm**



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Rev.: 2.0
Revision History:
1. Add another solid figure of TO-220-3L

Rev.: 1.9
Revision History:
1. Modify the Electrical characteristics

Rev.: 1.8
Revision History:
1. Modify the package information of TO-220F-3L
2. Modify the package information of TO-220-3L

Rev.: 1.7
Revision History:
1. Modify the thermal characteristics

Rev.: 1.6
Revision History:
1. Modify the ordering information

Rev.: 1.5
Revision History:
1. Change the schematic diagram of MOS

Rev.: 1.4
Revision History:
1. Modify “ELECTRICAL CHARACTERISTICS”

Rev.: 1.3
Revision History:
1. Modify the values of T_{rr} and Q_{rr}

Rev.: 1.2
Revision History:
1. Add the halogen free information of SVF13N50F

Rev.: 1.1
Revision History:
1. Modify “PACKAGE OUTLINE”

Rev.: 1.0
Revision History:
1. Original