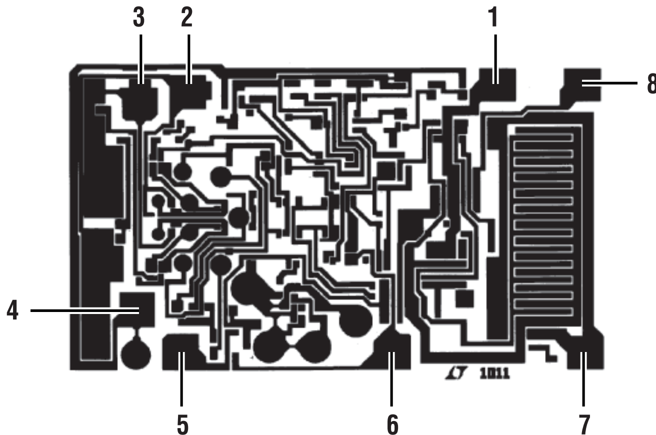
RH1011
Voltage Comparator



Die Size: 80 × 48 mils
Thickness: 12 mils
Backside Metal: Gold

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH1011	RH1011 DICE
RH1011	RH1011 DWF

Note: DWF = Dice in wafer form

PAD FUNCTION

1. Ground
2. +IN
3. –IN
4. V^-
5. Balance
6. Balance/Strobe
7. Output
8. V^+

Note: Backside (substrate) may be connected to V^- or no connection

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 36V
Output to Negative Supply 50V
Ground to Negative Supply 30V
Differential Input Voltage .... ±36V
Voltage at STROBE Pad 5V
Input Voltage .... Equal to Supplies
Output Short-Circuit Duration .... 10 sec
Junction Temperature... 150°C

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

DICE ELECTRICAL TEST LIMITS $V_S = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$, $T_J = 25°C$, $V_{GND} = V^-$

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2) $R_S \le 50k$ (Note 3)		1.5 2.0	mV mV
I_{OS}	Input Offset Current	(Note 3)		4	nA
I_B	Input Bias Current	(Note 2) (Note 3)		50 65	nA nA
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm15V$, $R_L = 1k$, $-10V \le V_{OUT} \le 14.5V$ $V_S = 5V$, $R_L = 500\Omega$, $0.5V \le V_{OUT} \le 4.5V$	200 50		V/mV V/mV
CMRR	Common Mode Rejection Ratio		90		dB
	Input Voltage Range	$V_S = \pm15V$ V_S = Single 5V	–14.5 0.5	13 3	V V
V_{OL}	Output Saturation Voltage	$V_{IN}^- = 5mV$, $V_{GND} = 0V$, $I_{SINK} = 8mA$ $I_{SINK} = 50mA$		0.4 1.5	V V
	Output Leakage Current	$V_{IN}^+ = 5mV$, $V_{GND} = -15V$ $V_{OUT} = 20V$		10	nA
	Positive Supply Current	(Note 4)		4	mA
	Negative Supply Current	(Note 4)		2.5	mA
	Strobe Current	Minimum to Ensure Output Transistor Is Off (Notes 4, 5, 6)	500		µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Output is sinking 1.5mA with $V_{OUT} = 0V$.

Note 3: These specifications apply for all supply voltages from a single 5V to ±15V, the entire input voltage range and for both high and low output states. The high state is $I_{SINK} \ge 100\mu A$, $V_{OUT} \ge (V^+ - 1V)$ and the low state is $I_{SINK} \le 8mA$, $V_{OUT} \le 0.8V$. Therefore, this specification defines a worst-case error band that includes effects due to common mode signals, voltage gain and output load.

Note 4: $V_{GND} = 0V$

Note 5: Do not short the STROBE pad to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500µA will strobe the RH1011 if speed is not important. External leakage on the STROBE pin in excess of 0.2µA when the strobe is "off" can cause offset voltage shifts.

Note 6: Guaranteed by design, characterization or correlation to other tested parameters.

Note 7: Please refer to LTC standard product data sheets for all other applicable information.

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much "softer" than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-1011

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/LT 0603 REV B • PRINTED IN USA

LINEAR TECHNOLOGY

© LINEAR TECHNOLOGY CORPORATION 2000