Features

- Also known as SMCS116SpW
- Single Bidirectional SpaceWire link allowing
  - Full duplex communication
  - Transmit rate from 1.25 up to 200 Mbit/s in each direction
  - Supports Serial Transfer Universal Protocol (STUP)
- Derived from the T7906 Single Point to Point IEEE 1355 High Speed Controller
  - Known anomalies of the T7906 chip corrected
- Host interface
  - Gives read/write accesses to the AT7912F configuration registers
  - Gives read/write accesses to the SpaceWire channel
- ADC/ DAC interface
  - Allows direct connection of an ADC with a width of up to 16 bits
  - Allows direct connection of a DAC with up to 16 data lines and the required control signals
- FIFO interface
- RAM interface
  - 16-bit data bus and 16-bit address bus
  - Four chip selects to address 4 different memory partitions
- Two independent UART interfaces
- 24 Bidirectional General Purpose I/Os
- Two 32-Bit Timers / Event Counters
- SpaceWire Link Performance
  - At 3.3V : 100Mbit/s full duplex communication
  - At 5V : 200Mbit/s full duplex communication
- Operating range
  - Voltages
    - 3V to 3.6V
    - 4.5V to 5.5V
  - Temperature
    - - 55°C to +125°C
- Maximum Power consumption
  - At 3.6V with a 5MHz clock: 150mW
  - At 5.5V with a 5MHz clock: 700mW
- Radiation Performance
  - Total dose tested successfully up to 50 Krad (Si)
  - No single event latchup below a LET of 80 MeV/mg/cm2
- ESD better than 2000V
- Quality Grades
  - QML-Q or V with SMD
- Package: 100pins MQFPF
- Mass: 3grams

Single SpaceWire link High Speed Controller

AT7912F

7829A–AERO–10/08

1. Description

The AT7912F provides an interface between a SpaceWire link according to the SpaceWire Standard ECSS-E-50-12A and several different interfaces.

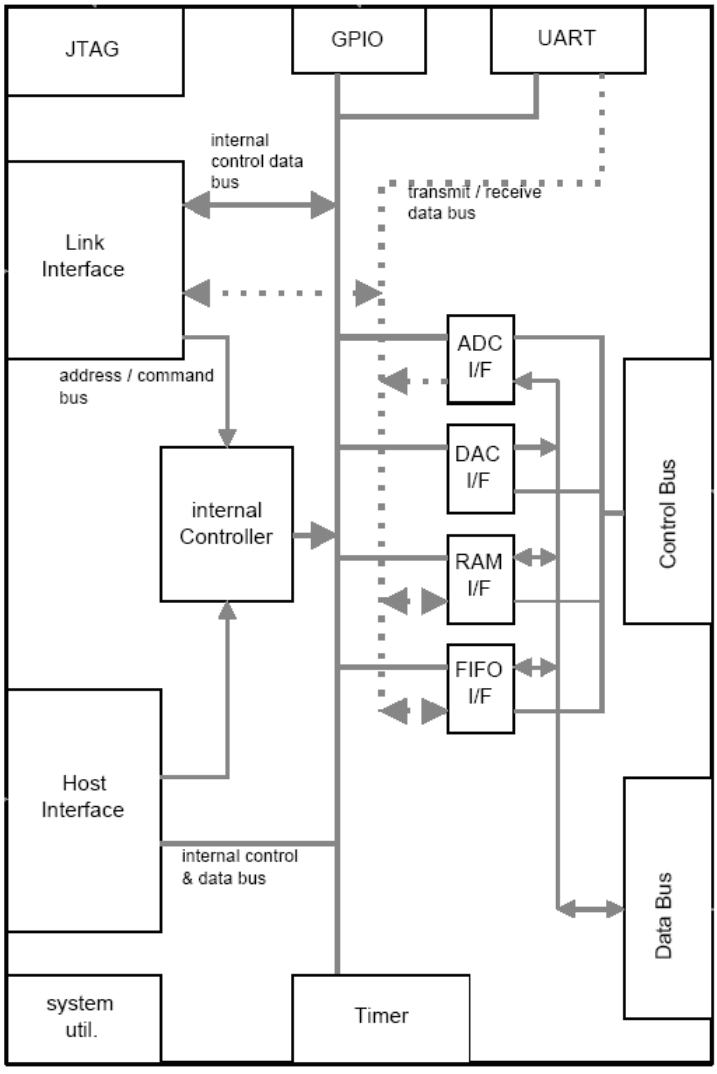
The AT7912F was designed by EADS Astrium in Germany under the name 'SMCS116SpW" for "Scalable Multi-channel Communication Subsystem for SpaceWire". It is manufactured using the SEU hardened cell library from Atmel MG2RT CMOS 0.5µm radiation tolerant sea of gates technology.

For any technical question relative to the functionality of the AT7912F please contact Atmel technical support at **assp-applab.hotline@nto.atmel.com**.

This document should be read in conjunction with **EADS Astrium 'SMCS116SpW User Manual'**. This user manual is available at **www.atmel.com**.

A block diagram of the AT7912F is given in figure 1.

Figure 1. AT7912F Block Diagram



The AT7912F provides one SpaceWire serial communication link with up to 200 Mbit/s data transmit rate. It features a link disconnect detection and parity check at character

level as well as an additional checksum generation/check at packet level. The AT7912F supports both the standard SpaceWire link protocol (transparent mode) and the STUP (Serial Transfer Universal Protocol) for efficient packet oriented data transfer.

In addition to the serial SpaceWire link, the AT7912F provides several different interfaces:

- Host interface
- ADC interface
- DAC interface
- RAM interface
- FIFO interface
- General purpose I/O
- UART interfaces
- Timers / Event Counters
- JTAG (IEEE 1149.1)

2. Pin Configuration

Table 2-1. Pin assignment

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
1	PLLOUT	**26**	IOB9	**51**	DATA4	**76**	TMR2_CLK
2	GND	**27**	VCC	**52**	DATA5	**77**	RxD1
3	VCC	**28**	GND	**53**	DATA6	**78**	TMR1_EXP
4	VCC	**29**	IOB10	**54**	DATA7	**79**	TMR2_EXP
5	LDO	**30**	IOB11	**55**	DATA8	**80**	TxD1
6	LSO	**31**	IOB12	**56**	VCC	**81**	HDATA0
7	LDI	**32**	IOB13	**57**	GND	**82**	HDATA1
8	LSI	**33**	IOB14	**58**	DATA9	**83**	HDATA2
9	GND	**34**	IOB15	**59**	DATA10	**84**	HDATA3
10	TCK	**35**	IOB16	**60**	DATA11	**85**	HDATA4
11	TMS	**36**	IOB17	**61**	VCC	**86**	HDATA5
12	TDI	**37**	IOB18	**62**	GND	**87**	HDATA6
13	TRST*	**38**	IOB19	**63**	DATA12	**88**	VCC
14	TDO	**39**	IOB20	**64**	DATA13	**89**	GND
15	GND	**40**	IOB21	**65**	DATA14	**90**	HDATA7
16	VCC	**41**	IOB22	**66**	DATA15	**91**	HDATNADR*
17	IOB0	**42**	IOB23	**67**	GPIO0	**92**	HSEL*
18	IOB1	**43**	IOB24	**68**	GPIO1	**93**	HWRNRD
19	IOB2	**44**	IOB25	**69**	GPIO2	**94**	HINTR*
20	IOB3	**45**	IOB26	**70**	GPIO3	**95**	RESET*
21	IOB4	**46**	IOB27	**71**	GPIO4	**96**	CLK
22	IOB5	**47**	DATA0	**72**	GPIO5	**97**	VCC_3VOLT
23	IOB6	**48**	DATA1	**73**	GPIO6	**98**	GND
24	IOB7	**49**	DATA2	**74**	GPIO7	**99**	GND
25	IOB8	**50**	DATA3	**75**	TMR1_CLK	**100**	VCC

3. Pin Description

Table 3-1. Pin description

Signal Name[1][3]	Type[2][4]	Function	5V ± 0.5V max. output current [mA]	3.3V ± 0.3V max. output current [mA]	load [pF]
HSEL*	I	When low, the external host selects the AT7912F host interface			
HWRnRD	I	Host interface write/read signal if HWRnRD is high during HSEL* low, the host writes data to the address register or to the AT7912F registers. if HWRnRD is low during HSEL* low, the host reads data from the address register or the AT7912F registers.			
HDATnADR	I	Host interface data/address signal if HDATnADR is high during read, the host reads/writes data from/to the internal AT7912F (data) registers. if HDATnADR is low during read, the host reads/writes address from/to the address register.			
HDATA(7:0)	I/O/Z	AT7912F data bus. HDATA(7:0) can be used as GPIO(2), if the Host interface is disabled	3	1.5	50
HINTR*	O	Host interrupt request line	3	1.5	50
TMR1_CLK	I	Timer1 clock (max. 12.5 MHz)			
TMR1_EXP	O	Timer1 expired. Asserted for one cycle if the value of counter1 is equal to the content of register TPERIOD1(3:0).	3	1.5	50
TMR2_CLK	I	Timer2 clock (max. 12.5 MHz)			
TMR2_EXP	O	Timer2 expired. Asserted for one cycle if the value of counter2 is equal to the content of register TPERIOD2(3:0).	3	1.5	50
RxD1	I	Receive data to UART1			
TxD1	O	Transmit data from UART1	3	1.5	50
LDI	I	Link Data Input			
LSI	I	Link Strobe Input			
LDO	O	Link Data Output	12	6	25
LSO	O	Link Strobe Output	12	6	25
DATA(15:0)	I/O/Z	Common AT7912F data bus	3	1.5	25
GPIO(7:0)	I/O	General purpose input/output lines	3	1.5	25
IOB(21:0)	I/O	Control bus. The AT7912F controls the connected interface via these lines.	6	3	25
IOB(24:22) IOB27	I/O		3	1.5	25
IOB(26:25)	I				
TRST*	I	Test Reset. Resets the test state machine			

Table 3-1. Pin description (Continued)

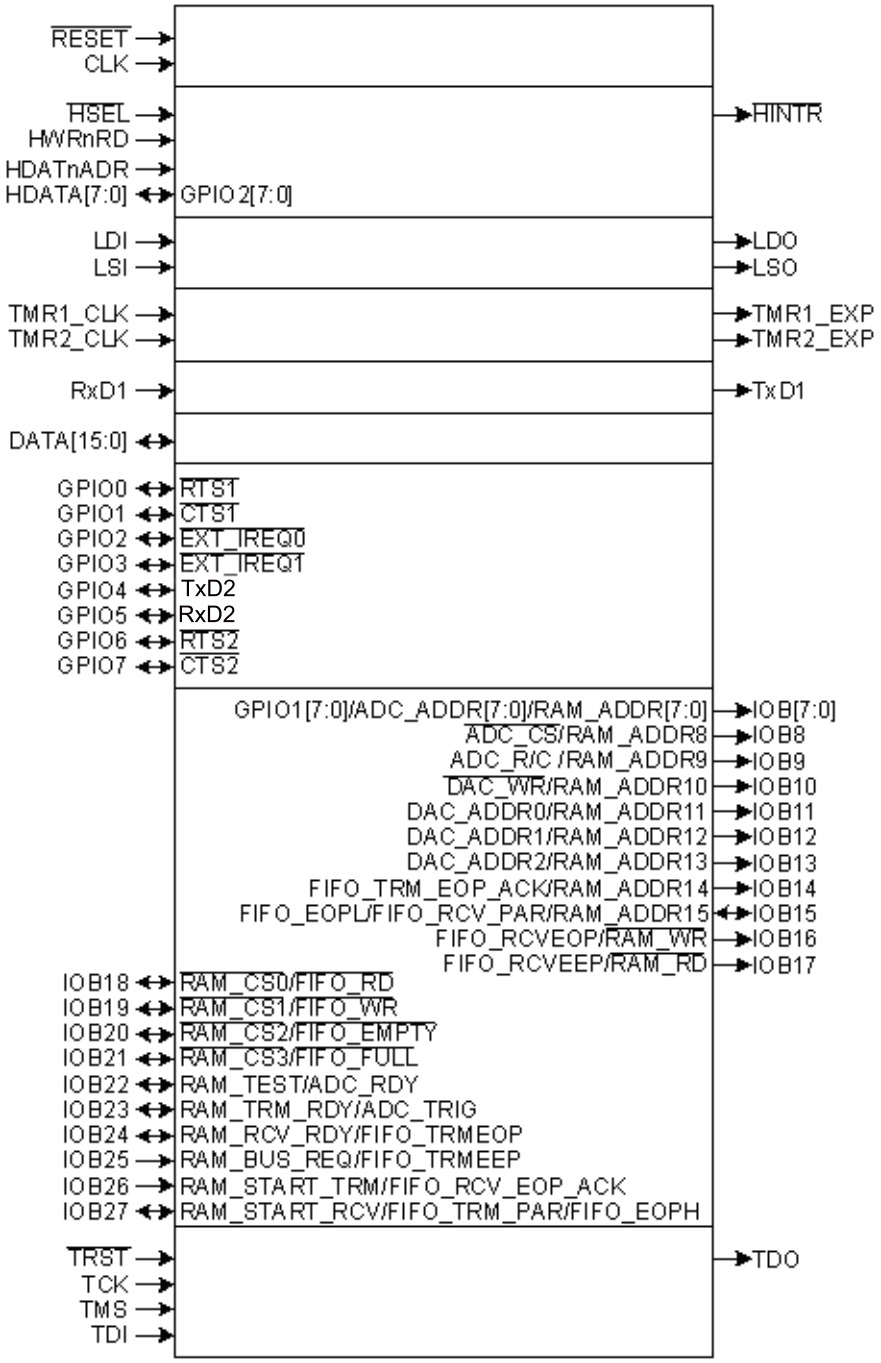
Signal Name[1][3]	Type[2][4]	Function	5V ± 0.5V max. output current [mA]	3.3V ± 0.3V max. output current [mA]	load [pF]
TCK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan			
TMS	I	Test Mode Select. Used to control the test state machine. This input should be left unconnected or tied to ground during normal operation			
TDI	I	Test Data Input. Provides serial data for the boundary scan logic			
TDO	O/Z	Test Data Output. Serial scan output of the boundary scan path	3	1.5	50
RESET*	I	AT7912F Reset. Sets the AT7912F to a known state. This input must be asserted (low) at power-up. The minimum width of RESET low is 2 cycles when CLK is running			
CLK	I	External clock input to AT7912F (max. 5 MHz)			
PLLOUT	O	Output of internal PLL. Used to connect a network of external RC filter devices.			
VCC_3VOLT	I	PLL Control signal Configure PLL for 3.3V or 5V operation VCC = 5 Volt: connect this signal with GND VCC = 3.3 Volt: connect this signal with VCC			
VCC		Power Supply			
GND		Ground			

Notes:
1. Groups of pins represent busses where the highest number is the MSB.
2. O = Output; I = Input; Z = High Impedance
3. (*) = active low signal
4. O/Z = if using a configuration with two AT7912Fs these signals can directly be connected together (WIROR)

3.1 Signals Organization

This section describes the signals of the AT7912F. Groups of signals represent buses where the highest number is the MSB.

Figure 3-1. Signals Organization



3.2 Shared I/O

Some of the functions of the AT7912F share the same I/O pins. This means that some functions are mutually exclusive. As an example, the GPIO port shares some of its I/O pins with the host interface. If the host interface is not used, these pins are available for GPIO; otherwise they are used as the host address and data bus. The selection of which functions are being used is made by programming the appropriate registers after a chip reset.

A short overview of the signals allocation for the various functions is given in the table below.

Table 3-2. Shared I/Os description

	Functions									
Signal	**GPIO**	**I/O**	**RAM Interface**	**I/O**	**FIFO Interface**	**I/O**	**DAC/ADC Interface**	**I/O**	**UART & Interrupts**	**I/O**
HDATA[7:0]	GPIO2[7:0]	I/O								
GPIO0	GPIO0_0	I/O							RTS1*	I
GPIO1	GPIO0_1	I/O							CTS1*	I
GPIO2	GPIO0_2	I/O							EXT_IRQ0*	I
GPIO3	GPIO0_3	I/O							EXT_IRQ1*	I
GPIO4	GPIO0_4	I/O							TxD2	O
GPIO5	GPIO0_5	I/O							RxD2	I
GPIO6	GPIO0_6	I/O							RTS2*	O
GPIO7	GPIO0_7	I/O							RTS2*	I
IOB[7:0]	GPIO1[7:0]	I/O	RAM_ADDR[7:0]	O			ADC_ADDR[7:0]	O		
IOB8			RAM_ADDR8	O			ADC_CS*	O		
IOB9			RAM_ADDR9	O			ADC_R/C*	O		
IOB10			RAM_ADDR10	O			DAC_WR*	O		
IOB11			RAM_ADDR11	O			DAC_ADDR0	O		
IOB12			RAM_ADDR12	O			DAC_ADDR1	O		
IOB13			RAM_ADDR13	O			DAC_ADDR2	O		
IOB14			RAM_ADDR14	O	FIFO_TRM_EOP_ACK	O				
IOB15			RAM_ADDR15	O	FIFO_RCV_PAR FIFO_EOPL	I/O				
IOB16			RAM_WR*	O	FIFO_RCVEOP	O				
IOB17			RAM_RD*	O	FIFO_RCVEEP	O				
IOB18			RAM_CS0*	O	FIFO_RD*	I/O				
IOB19			RAM_CS1*	O	FIFO_WR*	I/O				
IOB20			RAM_CS2*	O	FIFO_EMPTY*	I/O				

Table 3-2. Shared I/Os description (Continued)

Signal	Functions									
	GPIO	**I/O**	**RAM Interface**	**I/O**	**FIFO Interface**	**I/O**	**DAC/ADC Interface**	**I/O**	**UART & Interrupts**	**I/O**
IOB21			RAM_CS3*	O	FIFO_FULL*	I/O				
IOB22			RAM_TEST	O			ADC_RDY	I		
IOB23			RAM_TMR_RDY	O			ADC_TRIG	I		
IOB24			RAM_RCV_RDY	O	FIFO_TRMEOP	I				
IOB25			RAM_BUS_REQ*	I	FIFO_TRMEEP	I				
IOB26			RAM_START_TRM	I	FIFO_RCV_EOP_ACK	I				
IOB27			RAM_START_RCV	I	FIFO_TRM_PAR FIFO_EOPH	I/O				

4. Interfaces

The AT7912F provides an interface between a SpaceWire link according to the SpaceWire Standard ECSS-E-50-12A and several different interfaces:

- Host interface
- ADC/DAC interface
- RAM interface
- FIFO interface
- General purpose I/O
- UART interfaces
- Timers / Event Counters

4.1 Host Interface

Although the AT7912F is primarily designed to be remotely controlled, it can nevertheless be programmed and controlled by a local host if required. For that purpose the host interface provides 8 multiplexed data and address lines.

4.2 ADC/DAC interface

The ADC interface allows connecting an ADC with a width of up to 16 bits directly to the AT7912F. The AD conversion can be started by request via link or in a cyclic manner triggered by the on chip timers. When the AD conversion is ready, this is recognized by an external signal like "ready" or by an internal trigger, for example from the on chip timer. After reading the sample from the ADC it is then sent over the link. An 8-bit address generator is provided to allow multiplexing of analog signals. The address generator will start at a pre-programmed start address and will be incremented after each conversion.

The DAC interface is very similar to the ADC interface. It provides up to 16 data lines and the required control signals. The data to be sent to the DAC is received from the link and is stored in a register until the command "start DAC" is received. After that command the register values will be put to the DAC.

4.3 RAM Interface

The RAM interface provides a 16-bit data bus and 16-bit address bus. Four chip select lines allow addressing four different memory partitions (banks). This partitioning into different banks is done using 4 internal address boundary registers. These are 8 bit wide and provide a minimum page size of 1024 words. The memory interface can be programmed to use 0 to 7 wait states.

4.4 FIFO interface

The FIFO (8-bit or 16-bit data width) interface provides the control signals full, write, empty and read, depending on the direction of the data flow (receive/transmit).

Data received from the FIFO interface is sent over the SpaceWire link grouped in packets. The length of a packet (in bytes) can be specified either by setting an internal counter or by external signals. This interface can be programmed to use 0 to 7 wait states.

The FIFO interface handles two operating modes:

- An active mode where the AT7912F FIFO controller reads and writes from/to an external FIFO
- A passive mode where an external controller reads and writes from/to the AT7912F internal FIFO.

4.5 GPIO Interface

The general purpose I/O (GPIO Interface) provides up to 24 bidirectional signal lines. The direction (input or output) of each GPIO line can be set individually via register. Data to/from the GPIO lines is written / read via the GPIO data register. The GPIO provides 8 dedicated I/O lines, the remaining 16 lines of the port are shared with the ADC address and host data bus. These GPIO lines are available when the corresponding unit (e.g. the host data bus) of the AT7912F is not being used (disabled).

4.6 UART interface

Two independent UARTs are included in the AT7912F as well. One UART uses dedicated I/O lines whereas the second UART is sharing its pins with the GPIO port. The transmit rate of the UARTs in bps can be programmed via a 12-bit wide register with a maximum bit rate of about 780 kbit/s.

Each UART has a 4-byte FIFO in transmit, and a 4-byte FIFO in receive direction.

The UARTs can optionally use hardware handshake (rts/cts).

4.7 Timers / Event Counter

Two 32-bit on-chip timers are available on the AT7912F.

Each timer provides a 32-bit counter and a 32-bit reload register. The two timers can be operated independently or cascaded.

The timers can be used to set an external signal when the timeout value is reached. Each timer can generate periodic interrupts or only one interrupt, depending on configuration. An external output, TMR_EXP, signals to other devices that the timer count has expired. An external input, TMR_CLK, is provided which can be used as trigger source for the timer.

5. Operating Modes

5.1 Configuration of the AT7912F

The AT7912F provides registers and ports for configuration. Each register contains exactly one byte (read / write), whereas a port (e.g. a FIFO interface) behaves like a FIFO, meaning that multiple data bytes can be read or written from/to the port.

The ports of the AT7912F such as the FIFO, UART, ADC and RAM interfaces are accessed by a read/write command to the corresponding port address. In the case of FIFO, Host, UART and memory interfaces, a packet oriented access is also possible (meaning transferring multiple data bytes with a single command). The read/write selection of a command is done by setting bit 7 (MSB) of the first byte to one (read) or zero (write).

All internal registers are 8-bit wide addressable. Two simple commands, read and write, suffice to access all registers of the AT7912F.

Configuration/Programming of the AT7912F internal registers is done via either a simple protocol over the SpaceWire link or STUP over the SpaceWire link or directly via the host interface.

- The simple protocol over the SpaceWire, compatible with the T7906 (SCMCS116) link requires a command byte and, if necessary, one or more data bytes. The simple protocol ignores following bytes, if more bytes are sent.
- The STUP over the SpaceWire link uses 4 bytes for commands. It also supports logical addressing.
- The host interface provides a direct access to the internal registers through a 8-bit multiplexed address/data bus. After reset, the host interface is enabled.

After a chip reset the AT7912F is configured via the internal controller. This can be either by receiving the configuration data from the SpaceWire link or by an external controller connected to the host port of the AT7912F.

6. Test Interface

6.1 JTAG

This represents the boundary scan testing provisions specified by IEEE Standard 1149.1 of the Joint Testing Action Group (JTAG). The AT7912F test access port and on-chip circuitry is fully compliant with the IEEE 1149.1 specification. The test access port enables boundary scan testing of circuitry connected to the AT7912F I/O pins.

7. AT7912F differences with theT7906E

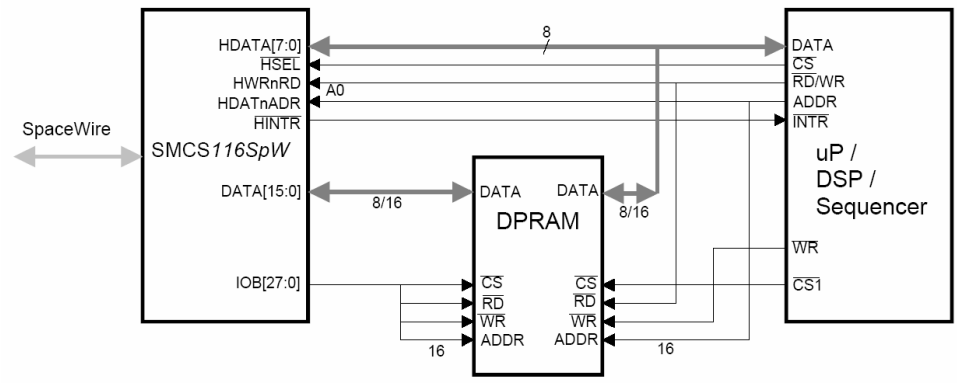
A few differences between the AT7912F and the T7906E exist in the registers, the signals and the pinout. These differences are detailed in the section 15 of the ‘SMCS116SpW User Manual”.

8. Typical Applications

Many applications require a SpaceWire link front end, however, no controller is required on the unit. Thanks to its communication memory interface, the AT7912F satisfies the requirements of these applications. Due to its small package and low power consumption it is an excellent alternative to FPGA based solutions.

A system using the AT7912F as a communication front-end for a microcontroller is shown in the following figure:

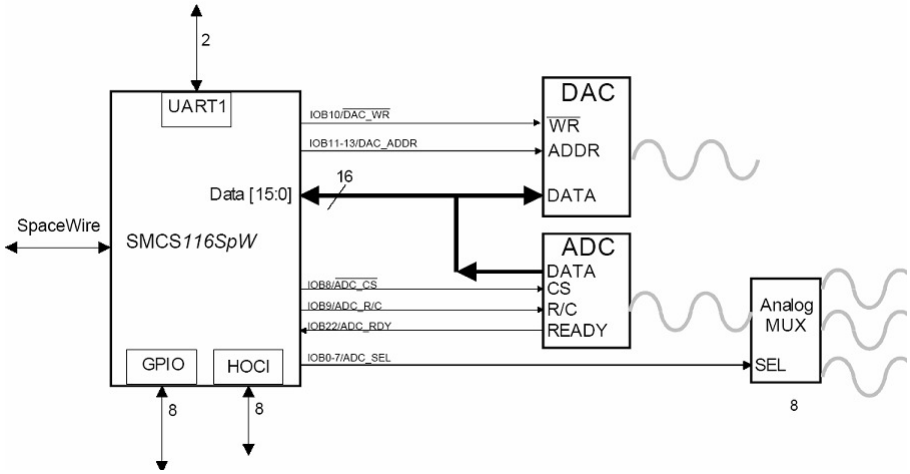
Figure 8-1. Processor Interface



Additional application targets of the AT7912F are modules and units without any built-in communication features, such as special image compression chips, application specific programmable logic or mass memory. The AT7912F is perfectly suited to be used on "non intelligent" modules such as A/D converter or sensor interfaces, due to its "control by link" feature and system control facilities. In addition, its fault tolerance feature makes the device very interesting for many critical industrial measurement and control systems.

Example applications of the AT7912F as communication and system controller on an interface node consisting of an ADC and DAC is given in the figure below:

Figure 8-2. ADC/DAC Interface



9. PLL Filter

The AT7912F embeds a PLL to generate its internal clock reference. The PLLOUT pin of the PLL is the output of the AT7912F that allows connection of the external filter of the PLL. The following figure presents the connection of the PLL filter.

Figure 9-1. PLL filter

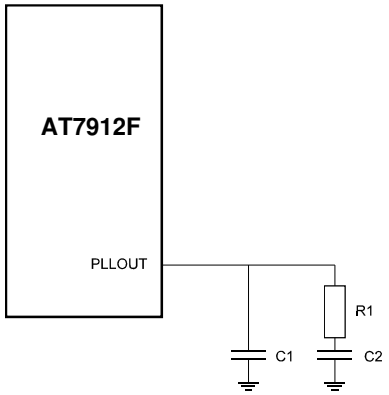


Table 9-1. PLL filter recommended components

R1	**1,5 kΩ ± 5%, ¼W**
C1	**22pF, ± 5%**
C2	**1.8nF, ± 5%**

10. Power Supply

To achieve its fast cycle time, the AT7912F is designed with high speed drivers on output pins. Large peak currents may pass through a circuit board's ground and power lines, especially when many output drivers are simultaneously charging or discharging their load capacitances. These transient currents can cause disturbances on the power and ground lines. To minimize these effects, the AT7912F provides separate supply pins for its internal logic and for its external drivers.

All GND pins should have a low impedance path to ground. A ground plane is required in AT7912F systems to reduce this impedance, minimizing noise.

The VCC pins should be bypassed to the ground plane using 8 high-frequency capacitors (0.1 µF ceramic). Keep each capacitor's lead and trace length to the pins as short as possible. This low inductive path provides the AT7912F with the peak currents required when its output drivers switch. The capacitors' ground leads should also be short and connect directly to the ground plane. This provides a low impedance return path for the load capacitance of the AT7912F output drivers.

The following pins must have a capacitor: 3, 4, 16, 27, 56, 61, 88 and 100.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7	V
I/O Voltage		-0.5 to VCC + 0.5	V
Operating Temperature Range (Ambient)	TA	-55 to +125	°C
Junction Temperature	TJ	175	°C
Storage Temperature Range	Tstg	-65 to +150	°C
Thermal resistance Junction to case	RThJC	5	°C/W

Stresses above those listed may cause permanent damage to the device.

11.2 DC Electrical Characteristics

The AT7912F can work with VCC = + 5 V ± 0.5 V and VCC = + 3.3V ± 0.3V. Although specified for TTL outputs, all AT7912F outputs are CMOS compatible and will drive to VCC and GND assuming no DC loads.

Table 11-2. 5V operating range DC Characteristics.

Parameter	Symbol	Min.	Max.	Unit	Conditions
Operating Voltage	VCC	4.5	5.5	V	
Input HIGH Voltage	VIH	2.2		V	
Input LOW Voltage	VIL		0.8	V	
Output HIGH Voltage	VOH	2.4		V	IOL = 1.5, 3, 6mA / VCC = VCC(min)
Output LOW Voltage	VOL		0.4	V	IOH = 1, 2, 4mA / VCC = VCC(min)
Output Short circuit current	IOS		90(1) 180(2) 270(3)	mA mA mA	VOUT = VCC VOUT = GND

Notes: 1. Applicable for HDATA[7:0], HINTR*, TMR1_EXP, TMR2_EXP, TxD1, DATA[15:0], GPIO[7:0], IOB[24:22], IOB27 and TDO pins
2. Applicable for IOB[21:0] pins
3. Applicable for LDO and LSO pins

Table 11-3. 3.3V operating range DC Characteristics.

Parameter	Symbol	Min.	Max.	Unit	Conditions
Operating Voltage	VCC	3.0	3.6	V	
Input HIGH Voltage	VIH	2.0		V	
Input LOW Voltage	VIL		0.8	V	
Output HIGH Voltage	VOH	2.4		V	IOL = 3, 6, 12mA / VCC = VCC(min)
Output LOW Voltage	VOL		0.4	V	IOH = 3, 6, 12mA / VCC = VCC(min)
Output Short circuit current	IOS		50(1) 100(2) 155(3	mA mA mA	VOUT = VCC VOUT = GND

Notes: 1. Applicable for HDATA[7:0], HINTR*, TMR1_EXP, TMR2_EXP, TxD1, DATA[15:0], GPIO[7:0], IOB[24:22], IOB27 and TDO pins
2. Applicable for IOB[21:0] pins
3. Applicable for LDO and LSO pins

11.3 Power consumption

Maximum power consumption figures at Vcc = 5.5V; -55°C; CLK = 5 MHz are presented in the following table.

Table 11-4. 5V Power Consumption

Operation Mode	Power consumption [mA]
not clocked	2
AT7912F in RESET	22
AT7912F in IDLE (1)	75
Maximum	120

1. IDLE means clk = 5 MHz, link started and running at 10Mbit/s, no activity on the other interfaces.

Maximum power consumption figures at Vcc = 3.6V; -55°C; CLK = 5 MHz are presented in the following table.

Table 11-5. 3.3V Power Consumption

Operation Mode	Power consumption [mA]
not clocked	1
AT7912F in RESET	10
AT7912F in IDLE (1)	23
Maximum	40

1. IDLE means clk = 5 MHz, link started and running at 10Mbit/s, no activity on the other interfaces.

11.4 AC Electrical Characteristics

The following table gives the worst case timings measured by Atmel on the 4.5V to 5.5V operating range

Table 11-6. 5V operating range timings.

Parameter	Symbol	Min.	Max.	Unit
Propagation delay TCK Low to TDO Low	Tp1		20	ns
Propagation delay CLK High to TMR1_EXP Low	Tp2		23	ns
Propagation delay CLK High to LDO Low	Tp3		16	ns
Propagation delay CLK High to HINTR* Low	Tp4		25	ns
Propagation delay CLK High to IOB18 Low	Tp5		16	ns

The following table gives the worst case timings measured by Atmel on the 3.0V to 3.6V operating range

Table 11-7. 3.3V operating range timings

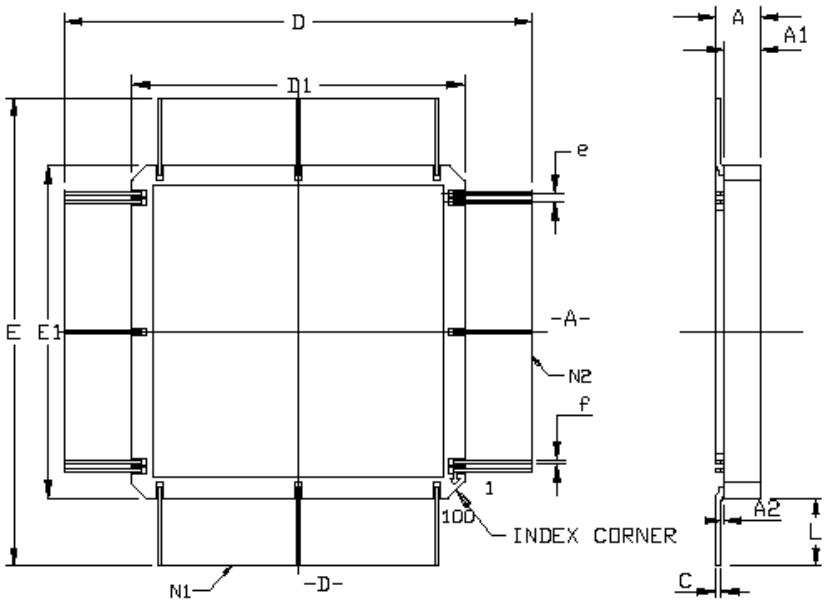
Parameter	Symbol	Min.	Max.	Unit
Propagation delay TCK Low to TDO Low	Tp1		33	ns
Propagation delay CLK High to TMR1_EXP Low	Tp2		38	ns
Propagation delay CLK High to LDO Low	Tp3		27	ns
Propagation delay CLK High to HINTR* Low	Tp4		41	ns
Propagation delay CLK High to IOB18 Low	Tp5		27	ns

For guaranteed timings on the two operating voltage ranges, refer to the section 12 of the ‘SMCS116SpW User Manual’

12. Package Drawings

12.1 MQFPF100

100 pins Ceramic Quad Flat Pack (MQFPF 100)



	Min	Max	Min	Max
A	2.21	2.67	.087	.105
C	0.15	0.20	.006	.008
D	31.80	32.80	1.252	1.291
D1	18.80	19.30	.740	.760
E	31.80	32.80	1.252	1.450
E1	18.80	19.30	.740	.760
e	0.635 BSC		.025 BSC	
f	0.254 REF		.010 REF	
A1	1.83	2.24	.072	.088
A2	0.203 REF		.008 REF	
L	6.50	6.75	.256	.266
N1	25		25	
N2	25		25	

* Lid is connected to ground.

13. Ordering Information

Part-number	Temperature Range	Package	Quality Flow
AT7912FKF-E	25°C	MQFPF100	Engineering sample
5962_08A0202QXC	-55°C to +125°C	MQFPF100	QML_Q
5962_08A0202VXC	-55°C to +125°C	MQFPF100	QML_V

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