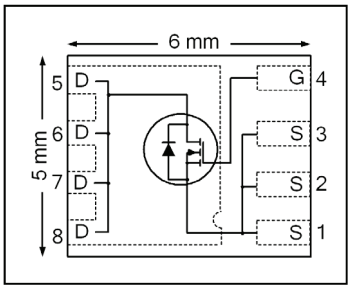
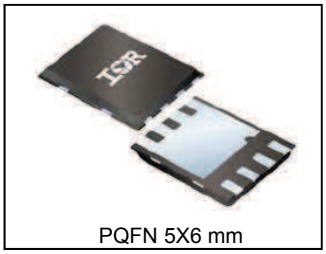
HEXFET® Power MOSFET

**Application**
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC converters
- DC/AC Inverters




| | |
|---|---|
| $V_{DSS}$ | 60V |
| $R_{DS(on)}$ typ. | 2.6mΩ |
| max | 3.2mΩ |
| $I_{D\ (Silicon\ Limited)}$ | 147A① |
| $I_{D\ (Package\ Limited)}$ | 100A① |

**Benefits**
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant


PQFN 5X6 mm

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRFH7085PbF | PQFN 5mm x 6mm | Tape and Reel | 4000 | IRFH7085TRPbF |

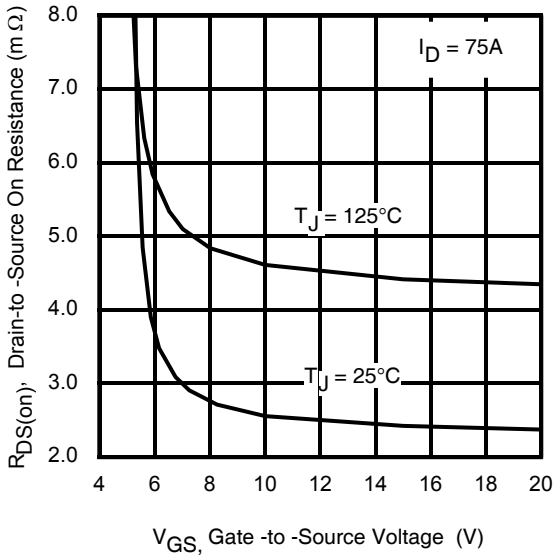



**Fig 1.** Typical On-Resistance vs. Gate Voltage

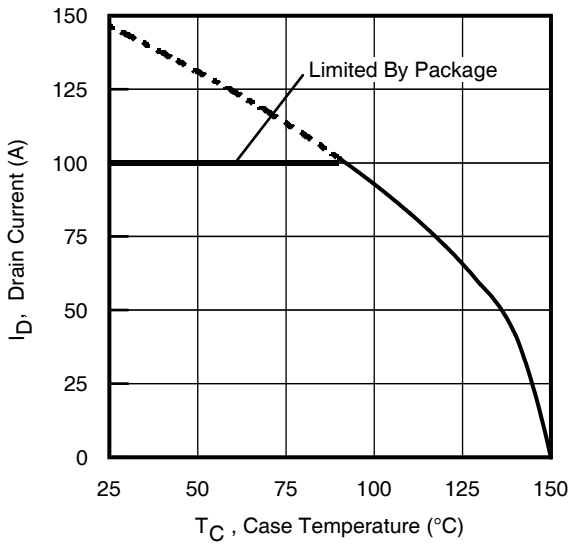



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_A$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 23 | A |
| $I_D$ @ $T_{C(Bottom)}$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 147① | |
| $I_D$ @ $T_{C(Bottom)}$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 93 | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Package Limited) | 100① | |
| $I_{DM}$ | Pulsed Drain Current ② | 590 | A |
| $P_D$ @ $T_C$ = 25°C | Maximum Power Dissipation | 156 | W |
| | Linear Derating Factor | 1.25 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |

**Avalanche Characteristics**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ③ | 319 | mJ |
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ⑨ | 554 | |
| $I_{AR}$ | Avalanche Current ② | See Fig 15, 16, 23a, 23b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ② | | mJ |

**Thermal Resistance**

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ (Bottom) | Junction-to-Case ⑧ | 0.5 | 0.8 | °C/W |
| $R_{\theta JC}$ (Top) | Junction-to-Case ⑧ | ––– | 20 | |
| $R_{\theta JA}$ | Junction-to-Ambient ⑩ | ––– | 34 | |
| $R_{\theta JA}$ (<10s) | Junction-to-Ambient | ––– | 22 | |

**Static @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 60 | ––– | ––– | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | ––– | 43 | ––– | mV/°C | Reference to 25°C, $I_D$ = 1.0mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | ––– | 2.6 | 3.2 | mΩ | $V_{GS}$ = 10V, $I_D$ = 75A |
| | | ––– | 3.6 | ––– | | $V_{GS}$ = 6.0V, $I_D$ = 38A |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.1 | ––– | 3.7 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 150µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | ––– | ––– | 1.0 | µA | $V_{DS}$ = 60V, $V_{GS}$ = 0V |
| | | ––– | ––– | 150 | | $V_{DS}$ = 60V,$V_{GS}$ = 0V,$T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | ––– | ––– | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | ––– | ––– | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Gate Resistance | ––– | 1.4 | ––– | Ω | |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 113µH, $R_G$ = 50Ω, $I_{AS}$ = 75A, $V_{GS}$ = 10V.

④ $I_{SD} \le$ 75A, di/dt ≤ 1280A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ $R_\theta$ is measured at $T_J$ approximately 90°C.

⑨ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 1mH, $R_G$ = 50Ω, $I_{AS}$ = 33A, $V_{GS}$ =10V.

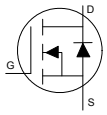
⑩ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
http://www.irf.com/technical-info/appnotes/an-994.pdf

**Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 140 | — | — | S | $V_{DS}$ = 10V, $I_D$ = 75A |
| $Q_g$ | Total Gate Charge | — | 110 | 165 | nC | $I_D$ = 75A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 30 | — | | $V_{DS}$ = 30V |
| $Q_{gd}$ | Gate-to-Drain Charge | — | 36 | — | | $V_{GS}$ = 10V |
| $Q_{sync}$ | Total Gate Charge Sync. (Qg - Qgd) | — | 74 | — | | |
| $t_{d(on)}$ | Turn-On Delay Time | — | 13 | — | ns | $V_{DD}$ = 30V |
| $t_r$ | Rise Time | — | 25 | — | | $I_D$ = 30A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 63 | — | | $R_G$ = 2.7Ω |
| $t_f$ | Fall Time | — | 23 | — | | $V_{GS}$ = 10V⑤ |
| $C_{iss}$ | Input Capacitance | — | 6460 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 560 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 380 | — | | $f$ = 1.0MHz |
| $C_{oss\ eff.(ER)}$ | Effective Output Capacitance (Energy Related) | — | 570 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 48V⑦ |
| $C_{oss\ eff.(TR)}$ | Output Capacitance (Time Related) | — | 715 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 48V⑥ |

**Diode Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 147① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ② | — | — | 590 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.2 | V | $T_J$ = 25°C, $I_S$ = 75A, $V_{GS}$ = 0V ⑤ |
| dv/dt | Peak Diode Recovery dv/dt ④ | — | 3.0 | — | V/ns | $T_J$ = 150°C, $I_S$ = 75A, $V_{DS}$ = 60V⑤ |
| $t_{rr}$ | Reverse Recovery Time | — | 31 | — | ns | $T_J$ = 25°C $V_{DD}$ = 51V |
| | | — | 30 | — | | $T_J$ = 125°C $I_F$ = 75A, |
| $Q_{rr}$ | Reverse Recovery Charge | — | 39 | — | nC | $T_J$ = 25°C di/dt = 100A/μs ⑤ |
| | | — | 33 | — | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | — | 1.9 | — | A | $T_J$ = 25°C |

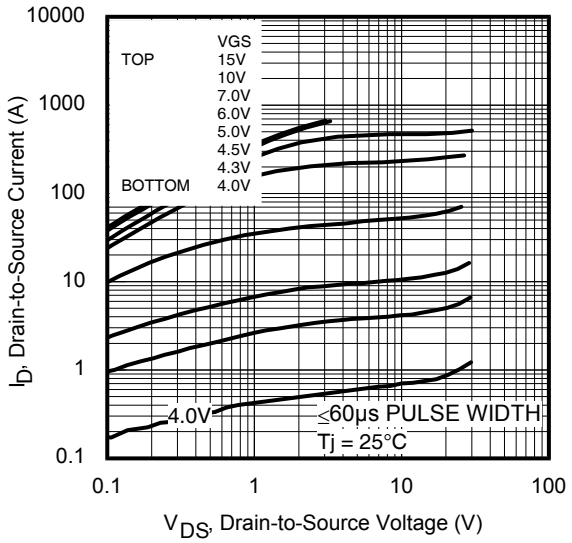



**Fig 3.** Typical Output Characteristics

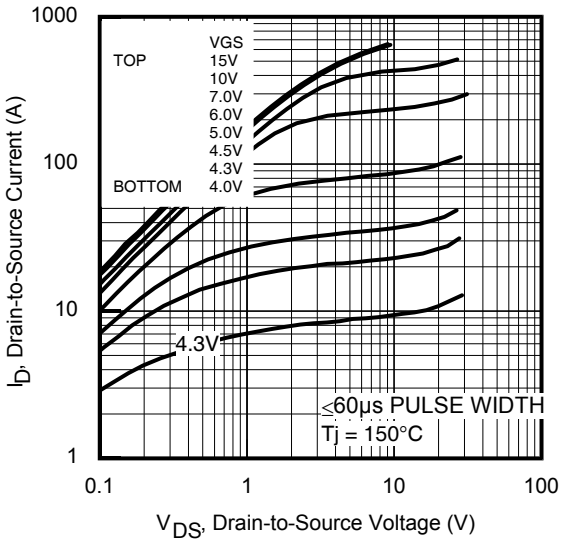



**Fig 4.** Typical Output Characteristics

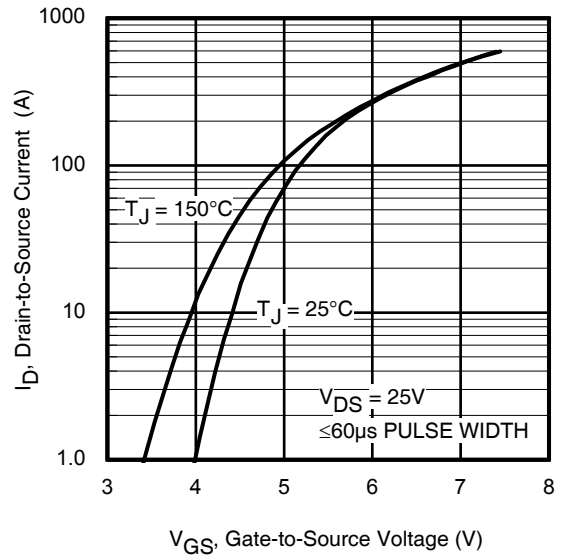



**Fig 5.** Typical Transfer Characteristics

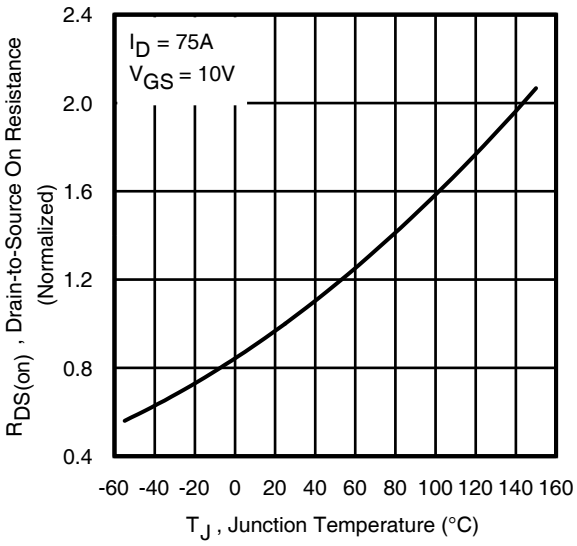



**Fig 6.** Normalized On-Resistance vs. Temperature

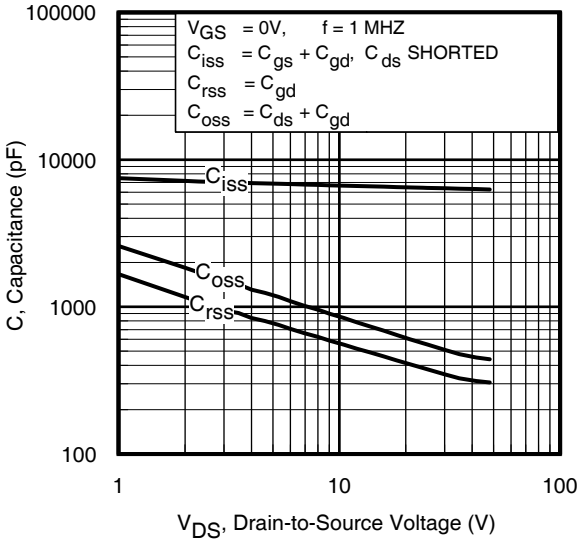



**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

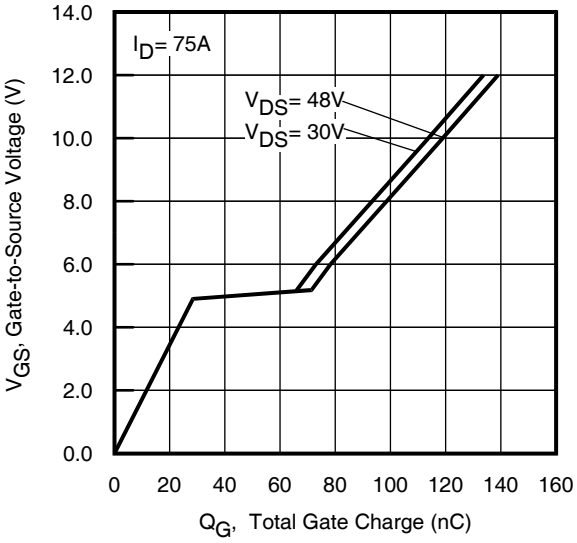



**Fig 8.** Typical Gate Charge vs. Gate-to-Source Voltage

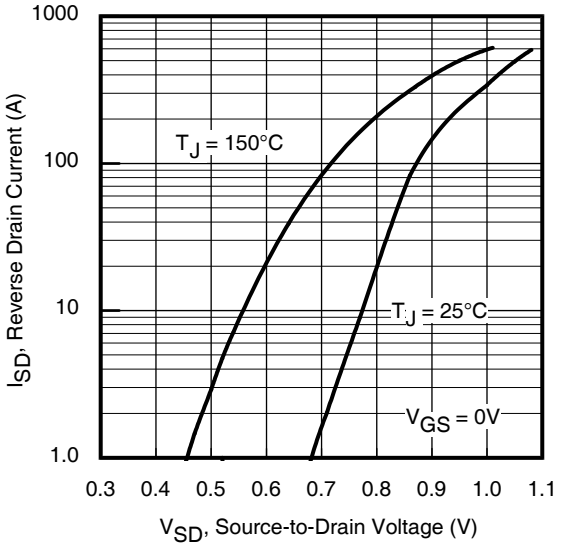



**Fig 9.** Typical Source-Drain Diode Forward Voltage

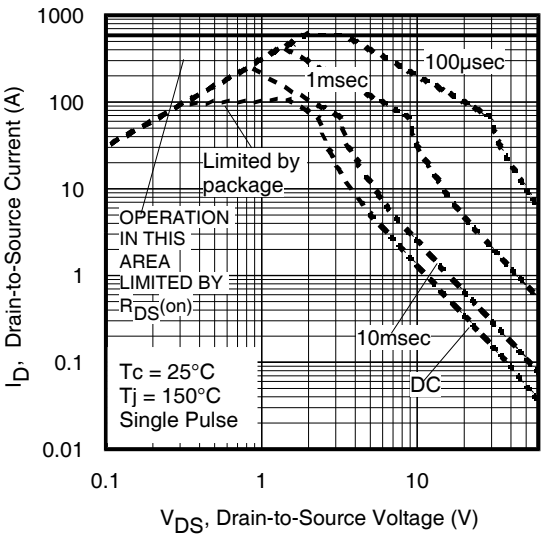



**Fig 10.** Maximum Safe Operating Area

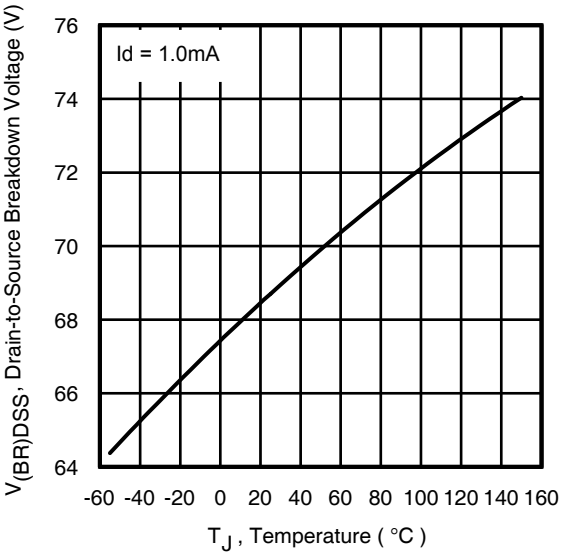



**Fig 11.** Drain-to-Source Breakdown Voltage

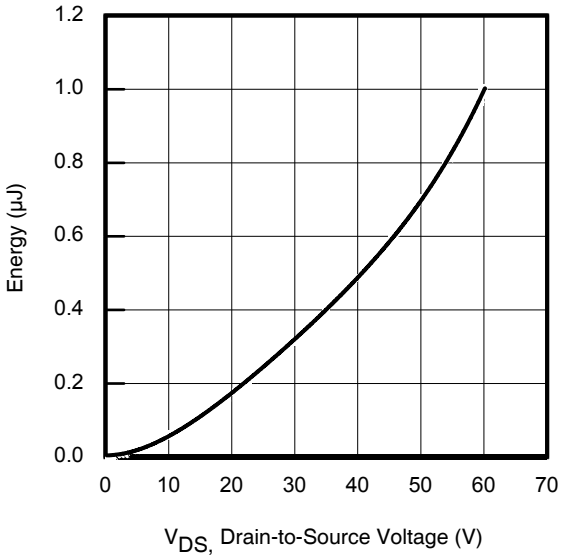



**Fig 12.** Typical $C_{oss}$ Stored Energy

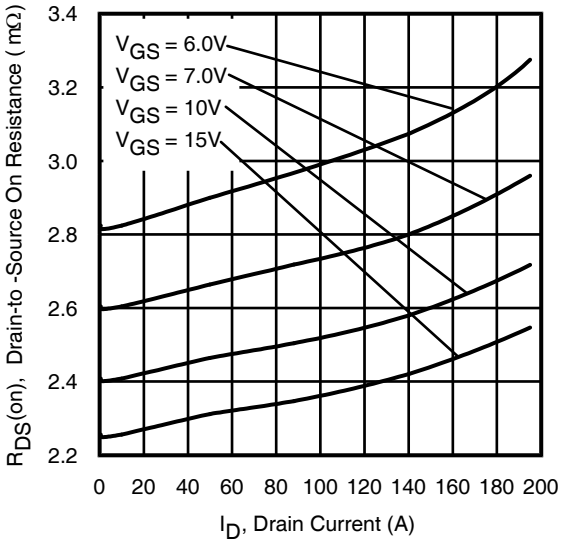



**Fig 13.** Typical On-Resistance vs. Drain Current

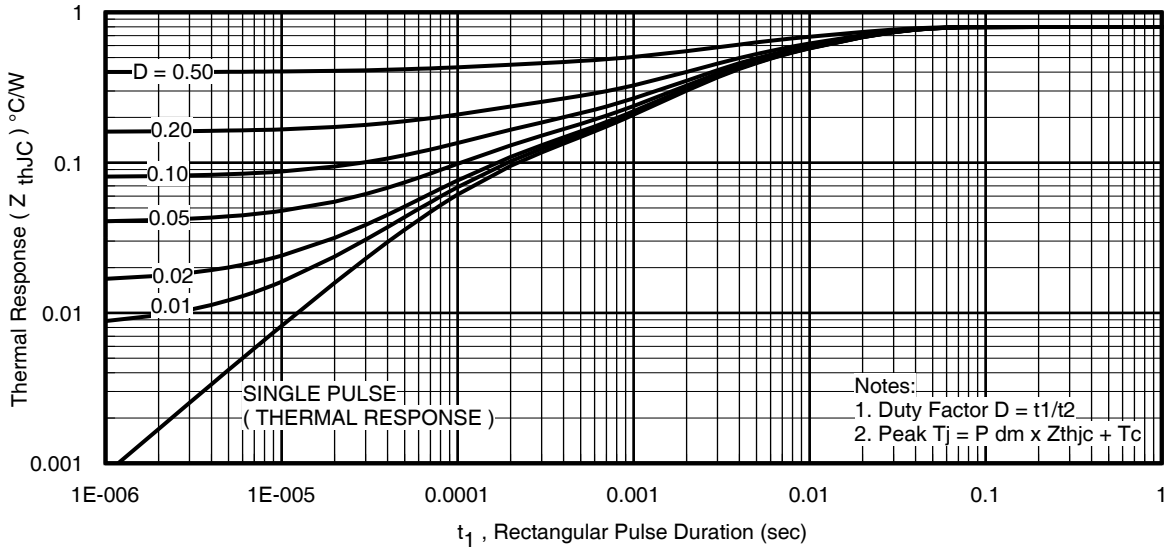



**Fig 14.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

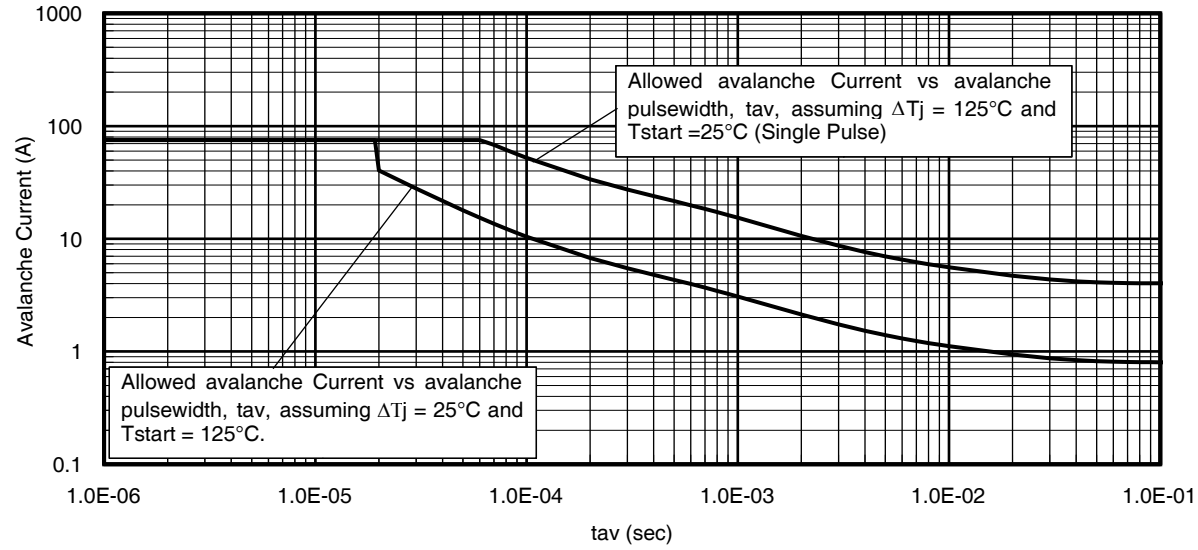



**Fig 15.** Typical Avalanche Current vs. Pulse Width

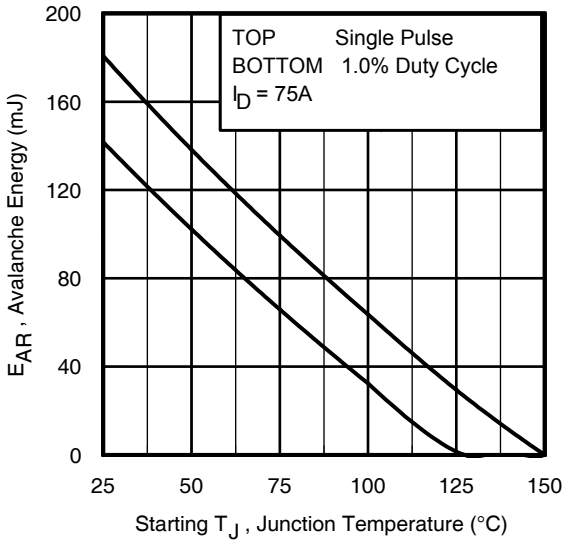



**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as$T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 14, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
   PD (ave) = 1/2 ( 1.3·BV·$I_{av}$) = $\Delta T/ Z_{thJC}$
   $I_{av} = 2\Delta T/ [1.3 \cdot BV \cdot Z_{th}]$
   $E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

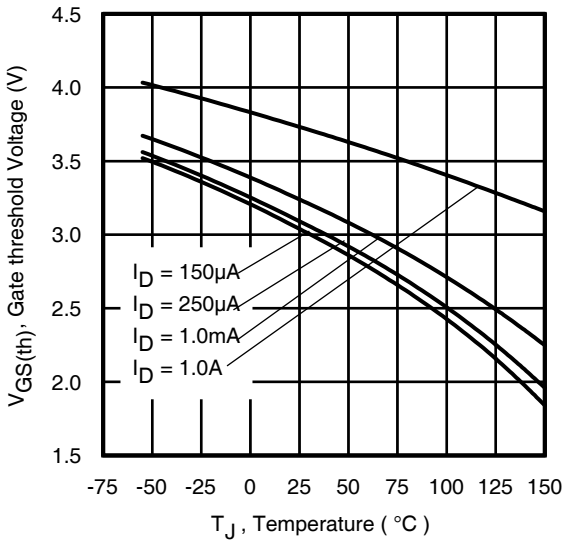



**Fig 17.** Threshold Voltage vs. Temperature

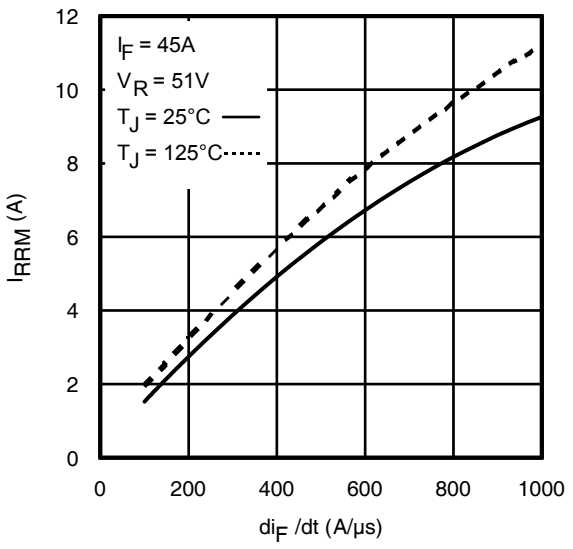



**Fig 18.** Typical Recovery Current vs. dif/dt

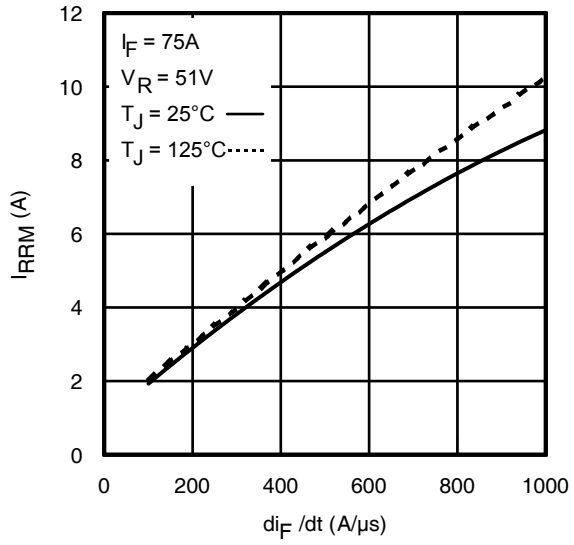



**Fig 19.** Typical Recovery Current vs. dif/dt

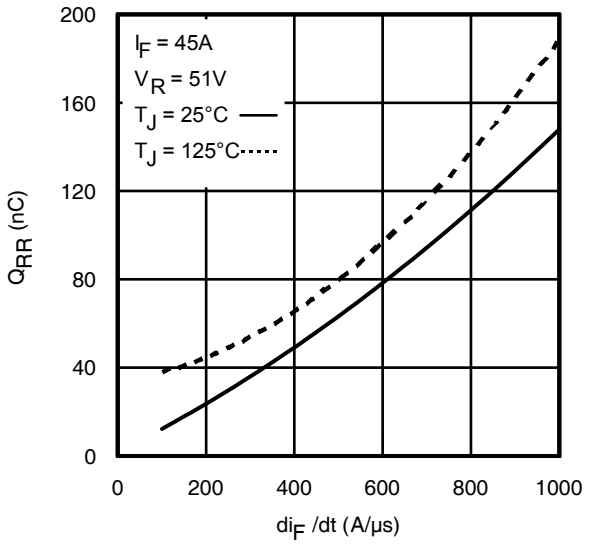



**Fig 20.** Typical Stored Charge vs. dif/dt

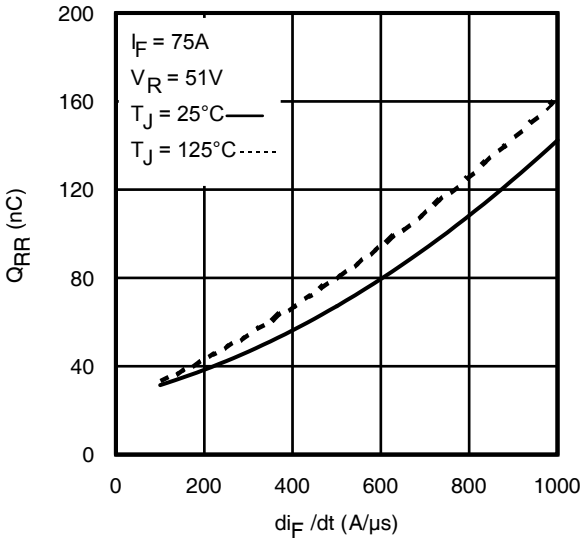



**Fig 21.** Typical Stored Charge vs. dif/dt

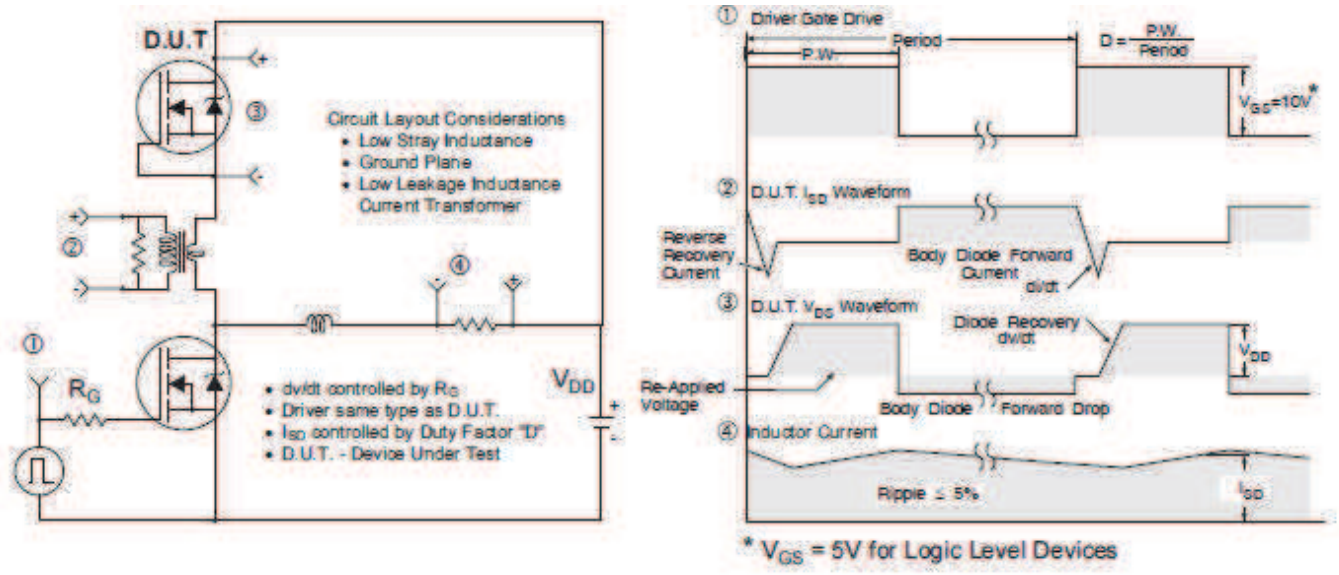



**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

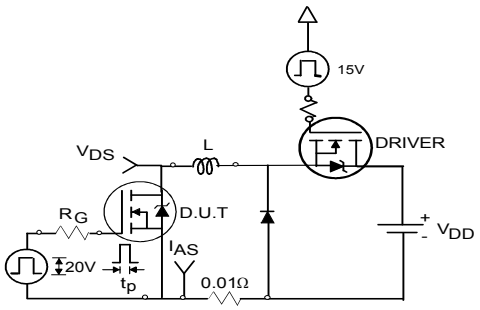



**Fig 23a.** Unclamped Inductive Test Circuit

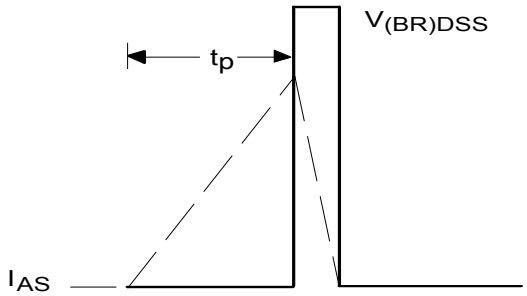



**Fig 23b.** Unclamped Inductive Waveforms

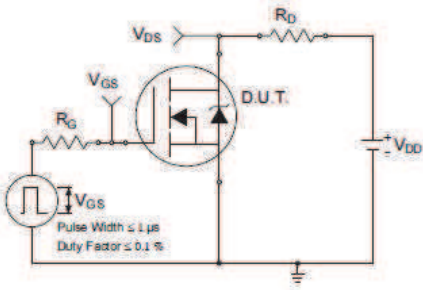



**Fig 24a.** Switching Time Test Circuit

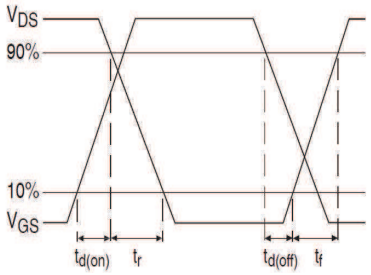



**Fig 24b.** Switching Time Waveforms

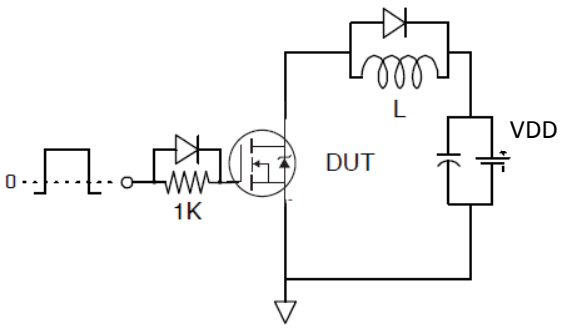



**Fig 25a.** Gate Charge Test Circuit

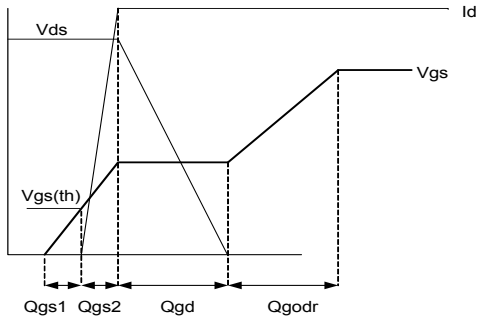
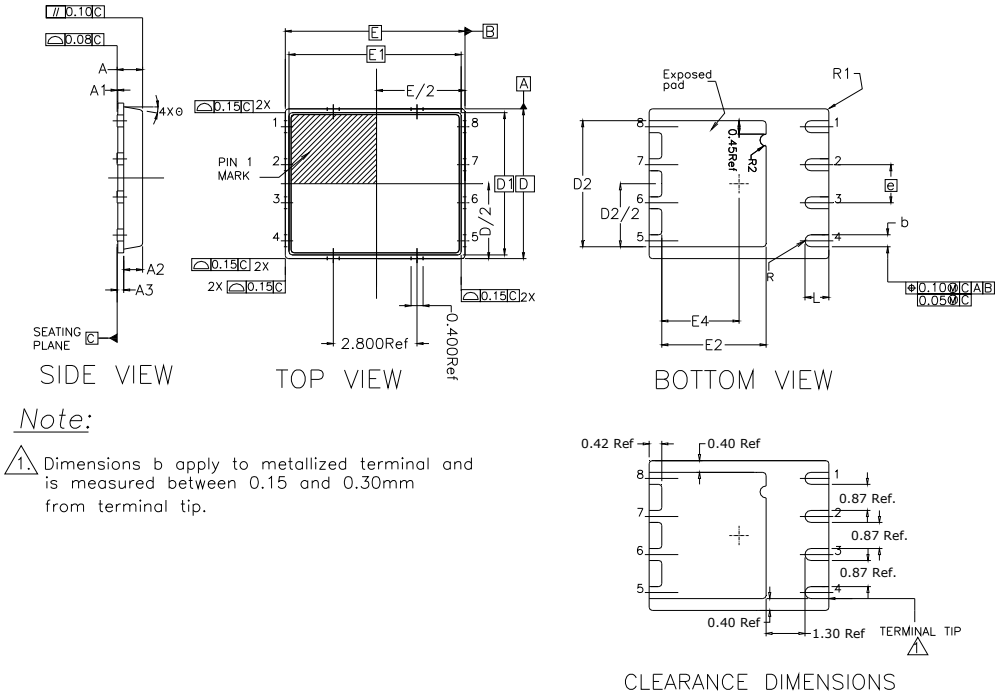



**Fig 25b.** Gate Charge Waveform

## PQFN 5x6 Outline "B" Package Details

| DIM / SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.800 | 0.830 | 0.900 |
| A1 | 0.000 | 0.020 | 0.050 |
| A2 | 0.580 | 0.630 | 0.680 |
| A3 | | 0.200 REF | |
| θ | 0° | 10° | 12° |
| b | 0.350 | 0.400 | 0.470 |
| D | 4.850 | 5.000 | 5.150 |
| D1 | 4.675 | 4.750 | 4.825 |
| D2 | 4.100 | 4.210 | 4.300 |
| e | | 1.270 BSC | |
| E | 5.850 | 6.000 | 6.150 |
| E1 | 5.675 | 5.750 | 5.825 |
| E2 | 3.380 | 3.480 | 3.580 |
| E4 | 2.480 | 2.580 | 2.680 |
| L | 0.700 | 0.800 | 0.900 |
| R | | 0.200 REF | |
| R1 | | 0.100 REF | |
| R2 | 0.150 | 0.200 | 0.250 |



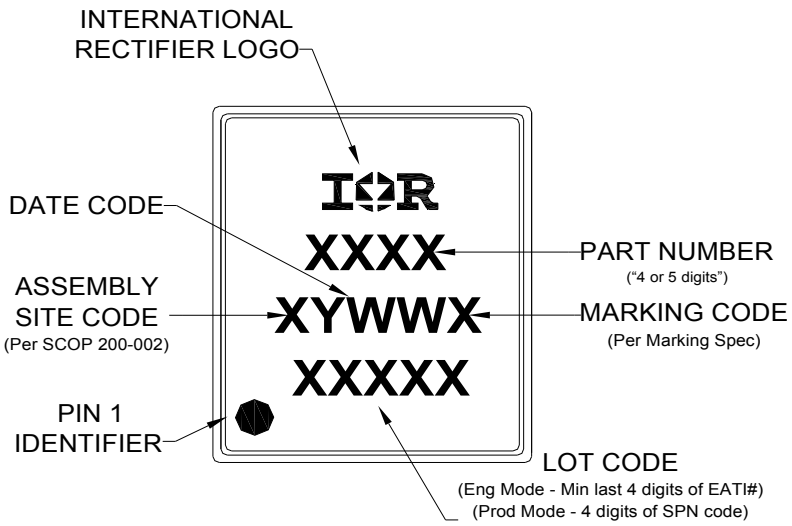




For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf

For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

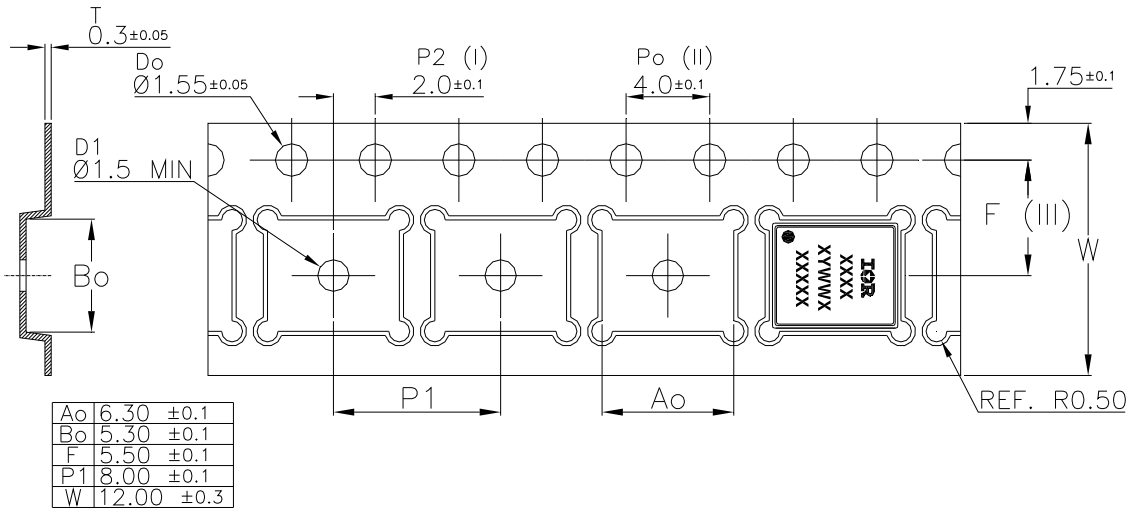
## PQFN 5x6 Outline "B" Part Marking




Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

**PQFN 5x6 Outline "B" Tape and Reel**




| | | |
|---|---|---|
| Ao | 6.30 | ±0.1 |
| Bo | 5.30 | ±0.1 |
| F | 5.50 | ±0.1 |
| P1 | 8.00 | ±0.1 |
| W | 12.00 | ±0.3 |

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

**Qualification Information†**

| | | |
|---|---|---|
| **Qualification level** | Industrial<br>(per JEDEC JESD47F †† guidelines ) | |
| **Moisture Sensitivity Level** | PQFN 5mm x 6mm | MSL1<br>(per JEDEC J-STD-020D††) |
| **RoHS Compliant** | Yes | |

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

| Date | Comments |
|---|---|
| 11/7/2014 | • Added $E_{AS\ (L\ =1mH)}$ = 554mJ on page 2<br>• Added note 9 "Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 1mH, $R_G$ = 50Ω, $I_{AS}$ = 33A, $V_{GS}$ =10V". on page 2<br>• Added Pd @ Tc = 25°C on Absolute Max Rating table on page 2 |

International
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To contact International Rectifier, please visit http://www.irf.com/whoto-call/

  