AN1268
APPLICATION NOTE

An Overview of the LPC Flash Interface

CONTENTS

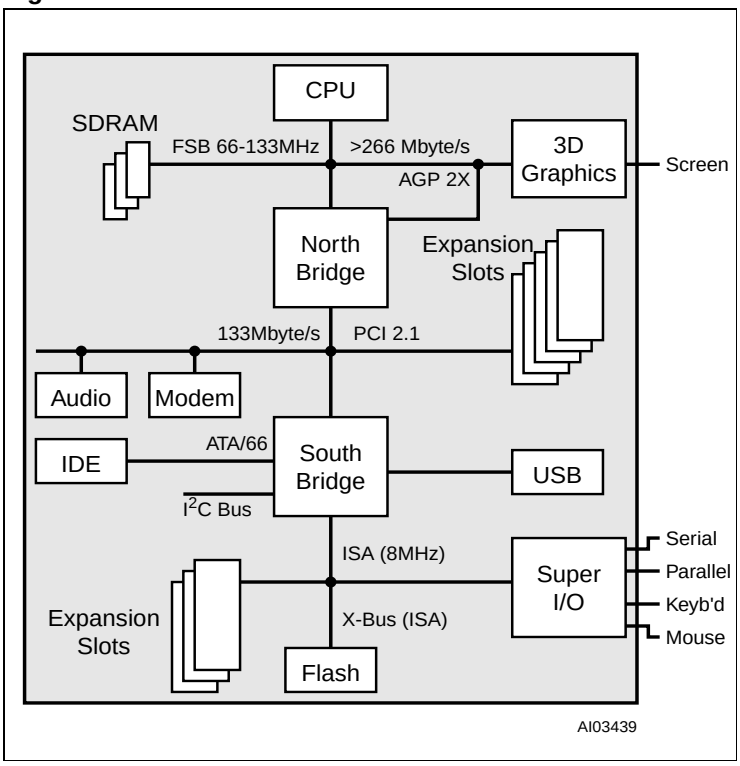
INTRODUCTION

STMicroelectronics new M50FW040 Firmware Hub takes advantage of a new motherboard intra-connect protocol known as the Low Pin Count Interface Specification or LPC. The LPC bus is a high-speed interface between a motherboard chipset and onboard peripheral functions. The LPC bus is quickly becoming the replacement for the slower Industry Standard Architecture (ISA or X-bus) on motherboards for connection of Super I/O, system management and, now, Flash for the system BIOS.

WHY A NEW INTERFACE?

Earlier PC systems contained an 8/16-bit expansion bus called the ISA bus; the BIOS was connected to a subset of this bus, often referred to as the X-bus. This architecture provided flexibility for add-in card designers and system designers but the ISA bus was slow and had interoperability problems due to lack of standardization of software and hardware. The PC motherboard with ISA/X-bus architecture is shown in Figure 1.

Figure 1. Earlier PC Architecture with ISA/X-bus



The LPC interface was defined as part of the evolution to a legacy-free and more user friendly PC architecture. It also has higher bandwidth potential, operating at 33 MHz rather than the 8 MHz ISA bus.

Since early 1998 there has been an industry wide push to eliminate the ISA bus from PC systems in an effort to reduce the cost of service calls to system and Operating System suppliers. Several key industry partners defined this transition initially in the PC97 Design Guidelines. The follow-on specifications (PC99) have provided an even more detailed transition plan that endorses plug-and-play compliance as the preferred expansion mechanism. In the same way that PCI, USB, and P1394 interfaces have provided a migration path away from ISA bus expansion cards, the LPC bus provides a transition to eliminate ISA motherboard devices. Table 1 shows the migration history of the key motherboard subsystems and I/O interfaces.

Table 1. Evolution of Motherboard Interconnect Technology

Subsystem	Legacy	Non-Legacy
Audio	ISA	PCI, AC'97, USB
Expansion Cards	ISA/EISA	PCI, USB
Network	ISA	PCI, USB
Graphics	ISA	PCI, AGP, Embedded
Modem	ISA	PCI, USB, AC'97
Hard Disk	IDE	EIDE, P1394
Super I/O	ISA	PCI, LPC
BIOS	ISA (X-bus)	LPC

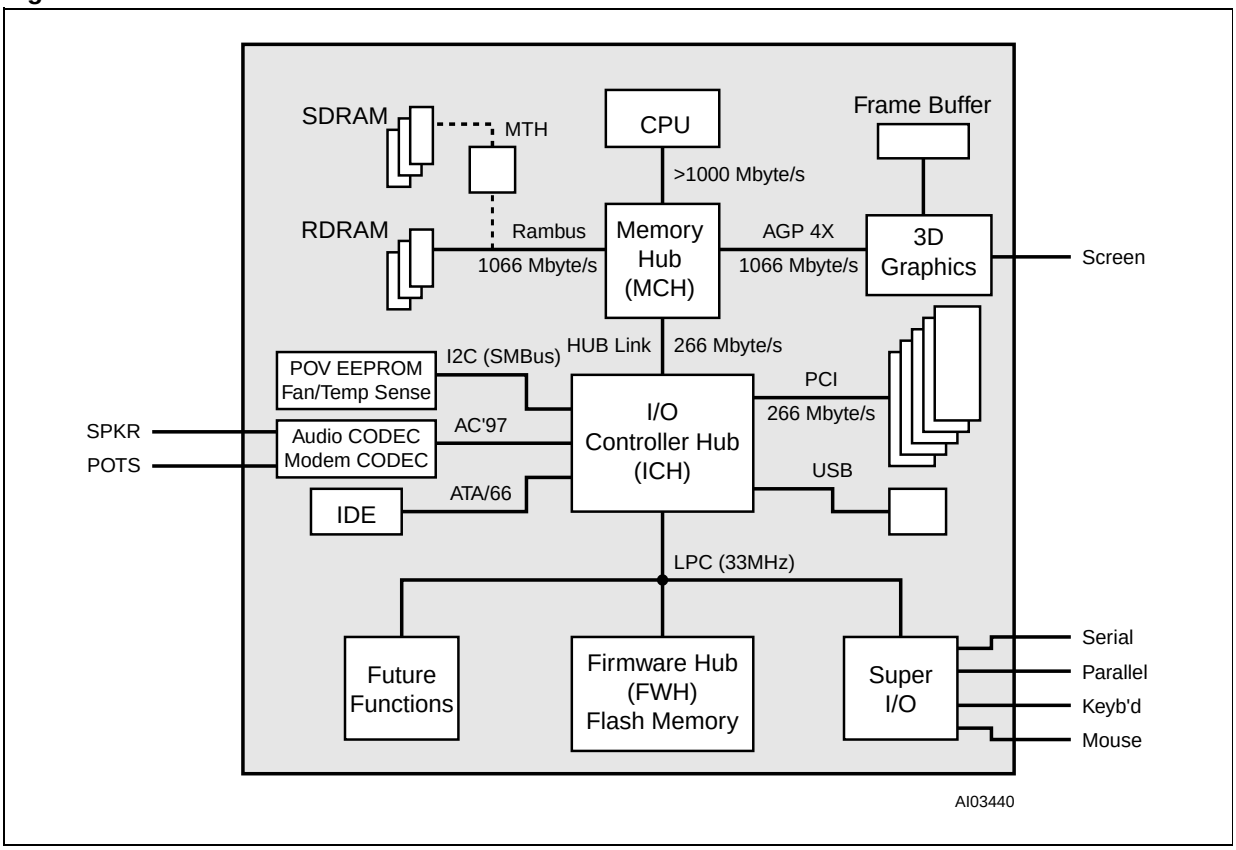
As shown in Table 1, the peripheral I/O functions that previously connected via the ISA bus have moved to plug-and-play structures such as PCI and USB. As this migration occurred, the only remaining function attached to the ISA bus was the Flash Memory containing the BIOS. LPC was invented as a better way to interconnect the core chipset and onboard peripheral functions.

WHAT IS THE LPC PROTOCOL?

The LPC bus is a multiplexed bus running at 33 MHz synchronously with the PCI bus. It uses PCI driver technology on the I/O pins in order to sustain high throughput rates. “Low Pin Count” refers to the fact that the interface only requires 7 to 13 signal pins, compared to 30 or more for the ISA bus. The LPC bus was first introduced on Intel’s 810 chipset in 1999.

The LPC bus matches the low-latency hub interconnect better than the ISA bus, resulting in better overall system performance. The LPC bus is capable of performing all the X-bus cycle types, including Memory, I/O, DMA, Bus Master, in addition to the FWH cycles that access the Flash Memory. FWH accesses utilize unique read/write LPC bus cycles to access the memory array, block locking, status, and GPI registers of the FWH Flash Memory. The LPC bus interface is synchronous; it uses PCI clock protocol and signaling resulting in more controlled transfer rates and less conflicts with system resources. From a system point of view, overall performance can be better than ISA bus systems because the busses are more balanced. There is less opportunity for high latency peripherals to slow performance of upstream busses.

Figure 2. New Motherboard Architecture with Firmware Hub



HOW DOES THE FWH FLASH MEMORY COMMUNICATE ON THE LPC BUS?

The LPC bus consists of 7 essential and 6 optional signals. The STMicroelectronics M50FW040 utilizes the 7 essential signals and does not use the 6 optional signals that are normally reserved for bus mastering and DMA functions. Please refer to the M50FW040 data sheet for specification of the ST firmware hub pin descriptions, including the non-LPC signals such as Top Block Lock, Reset and ID Select signals.

Table 2. Low Pin Count Interface Signals

LPC Signal	M50FW040 Pin	Required	Description
LAD0-LAD3	FWH0-FWH3	Y	Multiplexed command/address/data bus
$\overline{\text{LFRAME}}$	FWH4	Y	Indicates the start of a new cycle or aborts a cycle
$\overline{\text{LRESET}}$	$\overline{\text{INIT}}$	Y	PCI Reset
LCLK	CLK	Y	33MHz PCI Clock
Optional LPC Signals			
$\overline{\text{LDRQ}}$	–	N	Encoded DMA request from peripheral
SERIRQ	–	N	Serialized IRQ request from peripheral
$\overline{\text{CLKRUN}}$	–	N	DMA/Bus Master PCI CLKRUN signal
$\overline{\text{PME}}$	–	N	Power management event signal, PCI $\overline{\text{PME}}$
$\overline{\text{LPCPD}}$	–	N	Peripheral power down input
$\overline{\text{LSMI}}$	–	N	Peripheral SMI output pin

The LPC bus uses a multiplexed protocol on the 4-bit LAD0-LAD3 bus to transfer command, address, and data information serially between the host and peripherals (M50FW040 FWH is considered a peripheral). A cycle is started on the rising edge of LCLK when $\overline{\text{LFRAME}}$ is asserted and a valid cycle type is driven on LAD0-LAD3 by the host.

The FWH Flash Memory uses LPC signals, but uses cycle types which are unique. Valid cycle types for the FWH Flash Memory are 1101b (read) and 1110b (write). These are the only cycle types recognized by the M50FW040 and they are ignored by other motherboard peripherals. These unique cycle types have been designed specifically to avoid conflicts with other devices.

All the other LPC cycle types are ignored by the FWH.

FWH Read Cycles

Valid FWH read cycles are initiated by the I/O Controller Hub (ICH) asserting 1101b on FWH0-FWH3 with FWH4 Low. All data transfers are valid on the rising edge of each clock cycle. The FWH read waveforms are shown in Figure 3, followed by a description of each clock cycle in Table 3.

Figure 3. FWH Read Cycle Waveforms

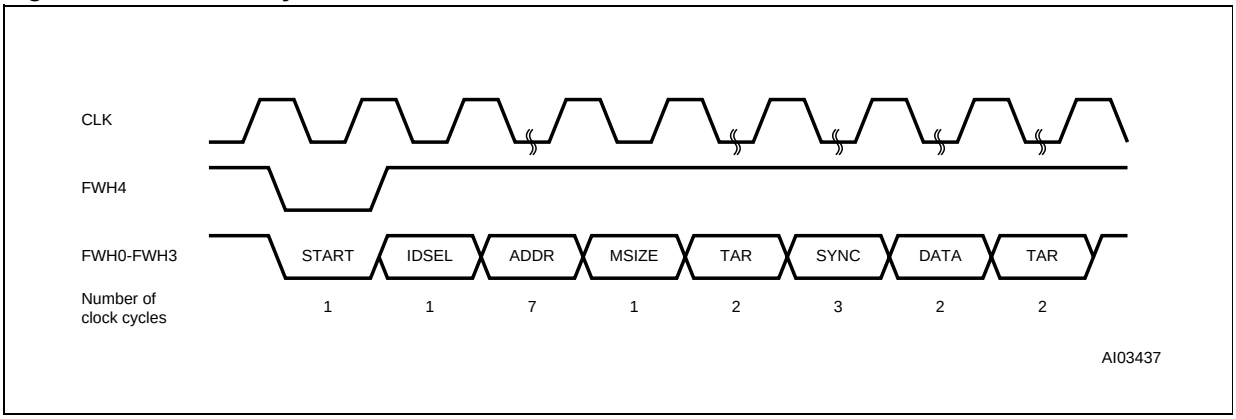


Table 3. FWH Read Cycle Signal Descriptions

Signal	Clock Cycles	FWH0-FWH3	Peripheral I/O	Description
START	1	1101b	I	On the rising edge of CLK with FWH4 Low, the contents of FWH0-FWH3 indicate the start of a FWH Read cycle.
IDSEL	1	XXXX	I	Indicates which FWH Flash Memory is selected. The value on FWH0-FWH3 is compared to the IDSEL strapping on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed.
ADDR	7	XXXX	I	A 28-bit address phase is transferred starting with the most significant nibble first.
MSIZE	1	0000b	I	Always 0000b (single byte transfer).
TAR	1	1111b	I	LPC host drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
TAR	1	1111b (float)	O	The FWH Flash Memory takes control of FWH0-FWH3 during this cycle.
WSYNC	2	0101b	O	The FWH Flash Memory drives FWH0-FWH3 to 0101b (short wait-sync) for two clock cycles, indicating that the data is not yet available.
RSYNC	1	0000b	O	The FWH Flash Memory drives FWH0-FWH3 to 0000b, indicating that data will be available during the next clock cycle.
DATA	2	XXXX	O	Data transfer is two CLK cycles, starting with the least significant nibble.
TAR	1	1111b	O	The FWH Flash Memory drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
TAR	1	1111b (float)	N/A	The FWH Flash Memory floats its outputs, the LPC host takes control of FWH0-FWH3.

FWH Write Cycles

Valid FWH write cycles are initiated by the I/O Controller Hub asserting 1110b on FWH0-FWH3 with FWH4 Low. All data transfers are valid on the rising edge of each clock cycle. The FWH write waveforms are shown in Figure 4, a description of each clock cycle is in Table 4.

Figure 4. FWH Write Cycle Waveforms

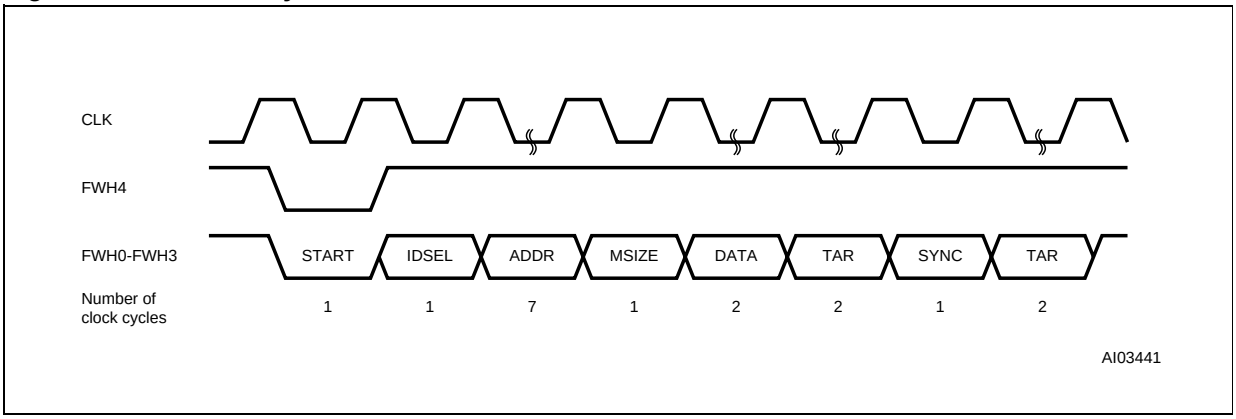


Table 4. FWH Write Cycle Signal Descriptions

Signal	Clock Cycles	FWH0-FWH3	Peripheral I/O	Description
START	1	1110b	I	On the rising edge of CLK with FWH4 Low, the contents of FWH0-FWH3 indicate the start of a FWH Write Cycle.
IDSEL	1	XXXX	I	Indicates which FWH Flash Memory is selected. The value on FWH0-FWH3 is compared to the IDSEL strapping on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed.
ADDR	7	XXXX	I	A 28-bit address phase is transferred starting with the most significant nibble first.
MSIZE	1	0000b	I	Always 0000b (single byte transfer).
DATA	2	XXXX	I	Data transfer is two cycles, starting with the least significant nibble.
TAR	1	1111b	I	The LPC host drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
TAR	1	1111b (float)	O	The FWH Flash Memory takes control of FWH0-FWH3 during this cycle.
SYNC	1	0000b	O	The FWH Flash Memory drives FWH0-FWH3 to 0000b, indicating it has received data or a command.
TAR	1	1111b	O	The FWH Flash Memory drives FWH0-FWH3 to 1111b, indicating a turnaround cycle.
TAR	1	1111b (float)	N/A	The FWH Flash Memory floats its outputs and the LPC host takes control of FWH0-FWH3.

Abort Mechanism

Once valid START, IDSEL, and MSIZE fields are received, the FWH Flash Memory will always assume that the following inputs are valid. In general, the FWH Flash Memory will not indicate that it has received an invalid field. If the FWH Flash Memory receives an invalid MSIZE (i.e. not 0000b), the internal state machine that operates the LPC bus will reset and no operation will be attempted.

The LPC bus provides an abort mechanism. Whenever FWH4 is Low, the FWH will tri-state its outputs and the LPC interface state machine will remain in reset state. Using this protocol, the I/O Controller Hub can abort any cycle by holding FWH4 low for several cycles. Note that the FWH Flash Memory internal operations are independent from the LPC bus interface. The internal FWH Flash Memory state machine will not begin a Flash program or erase operation until it has received the last data nibble from the I/O Controller Hub. These features insure data integrity for the FWH Flash Memory during program and erase operations.

A/A MUX MODE

The M50FW040 Firmware Hub also provides an Address/Address Mux mode (A/A Mux) for out of system programming. This interface is enabled by a strapping option on an input pin. A/A Mux mode is not intended for normal (in-system) operation, rather it is used for bulk programming out of the system and during motherboard manufacturing. More information about A/A Mux mode can be found in the M50FW040 data sheet.

CONCLUSION

The LPC bus interface is ideal for interconnect between onboard peripheral devices. It is faster than the ISA bus for all cycle types. It is more controlled because there are no unknown adapter cards that can cause resource conflicts. Finally, the boot process is simplified by using this fundamental protocol. In addition to Flash, the LPC bus holds promise for even more peripheral content in future PC motherboard, mobile, and server platforms. The new STMicroelectronics M50FW040 Firmware Hub uses the LPC bus to achieve higher bandwidth potential, and reliable data integrity.

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

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Please remember to include your name, company, location, telephone number and fax number.