ATWILC1000-MR110xB

IEEE 802.11 b/g/n Link Controller Module

Description

The ATWILC1000-MR110xB module is a low-power consumption IEEE 802.11 b/g/n IoT (Internet of Things) module, which is specifically optimized for low power IoT applications. This module features small form factor (21.7mm x 14.7mm x 2.1mm) while fully integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive (T/R), switch, power management, and PCB antenna. With advanced security, it is interoperable with various vendors using IEEE 802.11b/g/n Access Points in wireless LAN. The module provides Serial Peripheral Interface (SPI) and Secure Digital Input Output (SDIO) to interface with the host controller.

Note that all references to the ATWILC1000-MR110xB module include all the module devices listed below unless otherwise noted:

- ATWILC1000-MR110PB
- ATWILC1000-MR110UB

Features

- Compliant with IEEE 802.11 b/g/n 20 MHz (1x1) solution
- Supports Single spatial stream in 2.4 GHz ISM band
- Integrated Power Amplifier (PA) and Transmit/Receive (T/R) switch
- Superior sensitivity and range through advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization
- Wi-Fi Direct® and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 and WPA2-Enterprise security
- Superior Medium Access Control (MAC) throughput through hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgement
- On-chip memory management engine to reduce the host load
- SPI and SDIO host interfaces
- Operating temperature ranges from -40°C to +85°C
- Input/Output operating voltage of 1.8V to 3.6V
- Built-in 26 MHz crystal
- Power-save modes:
    – <1µA Power-Down mode typical at 3.3V I/O
    – 380µA Doze mode with chip settings preserved (used for beacon monitoring)
    – On-chip low power Sleep oscillator
    – Fast host wake-up from Doze mode by a pin or the host I/O transaction
- Wi-Fi Alliance® certified for connectivity and optimizations

– ID: WFA65340

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1. Ordering Information and Module Marking

The following table provides the ordering details of the ATWILC1000-MR110xB module.

Table 1-1. Ordering Details

Model Number	Ordering Code	Package	No. of Pins	Description	Regulatory Certification
ATWILC1000-MR110PB	ATWILC1000-MR110PB	21.7x14.7x2.1 mm	28	Certified module with ATWILC1000B-MU chip and PCB antenna	FCC, IC, CE
ATWILC1000-MR110UB	ATWILC1000-MR110UB	21.7x14.7x2.1 mm	28	Certified module with ATWILC1000B-MU chip and uFL connector	FCC

The following figure provides the marking information of the ATWILC1000-MR110xB module.

Figure 1-1. Marking Information
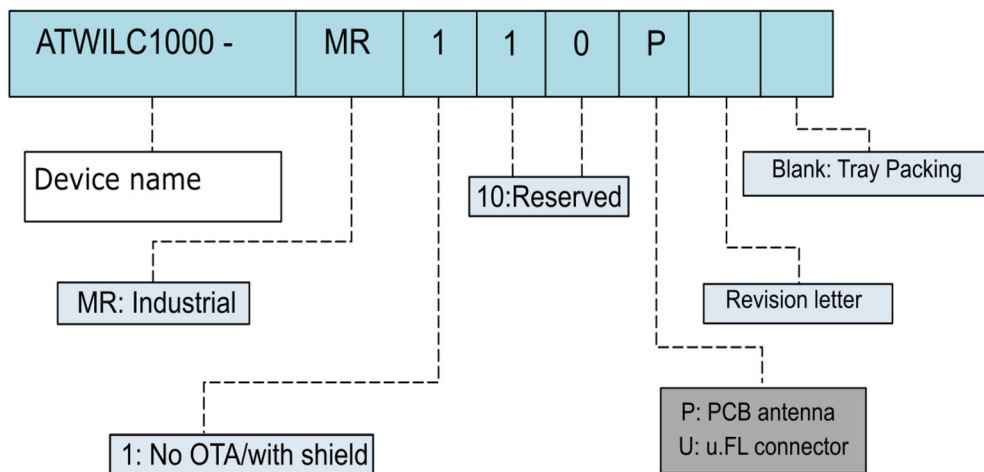
2.   Block Diagram

The following figure provides a basic overview of the ATWILC1000-MR110xB module.

Figure 2-1. ATWILC1000-MR110xB Module Block Diagram
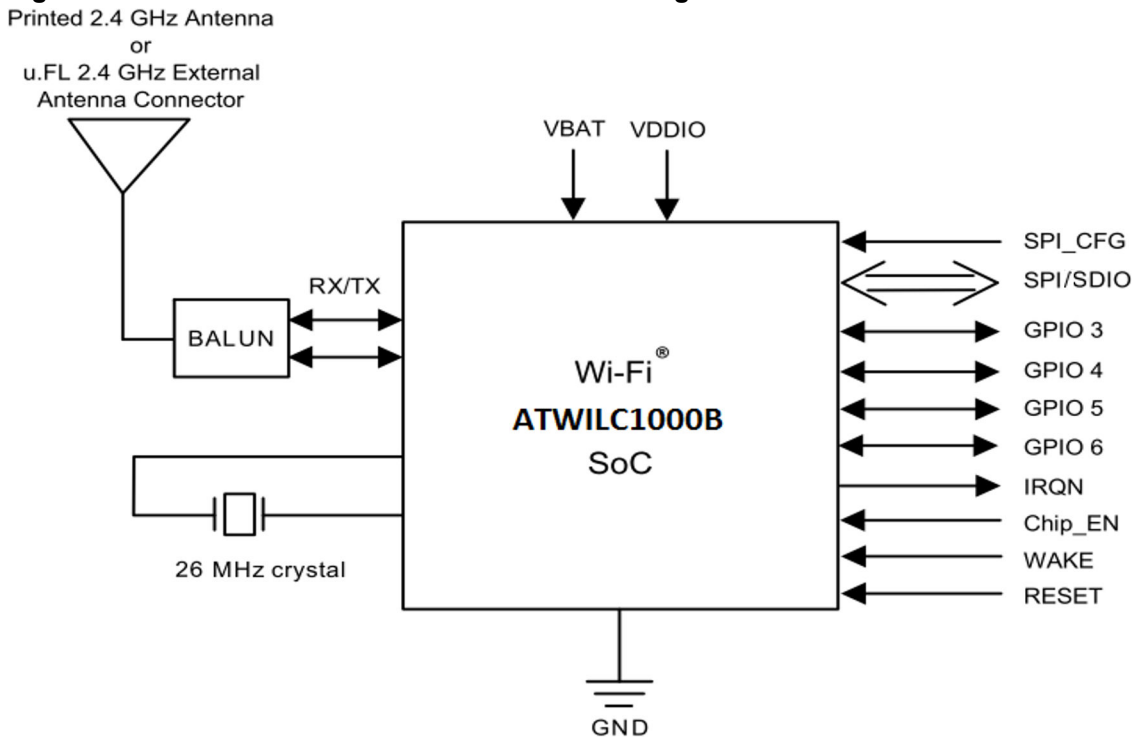
3. Pinout and Package Information

The ATWILC1000-MR110xB package has an exposed paddle that must be connected to the system board ground. The module pin assignment is shown in the following figure.

Figure 3-1. Pin Assignment
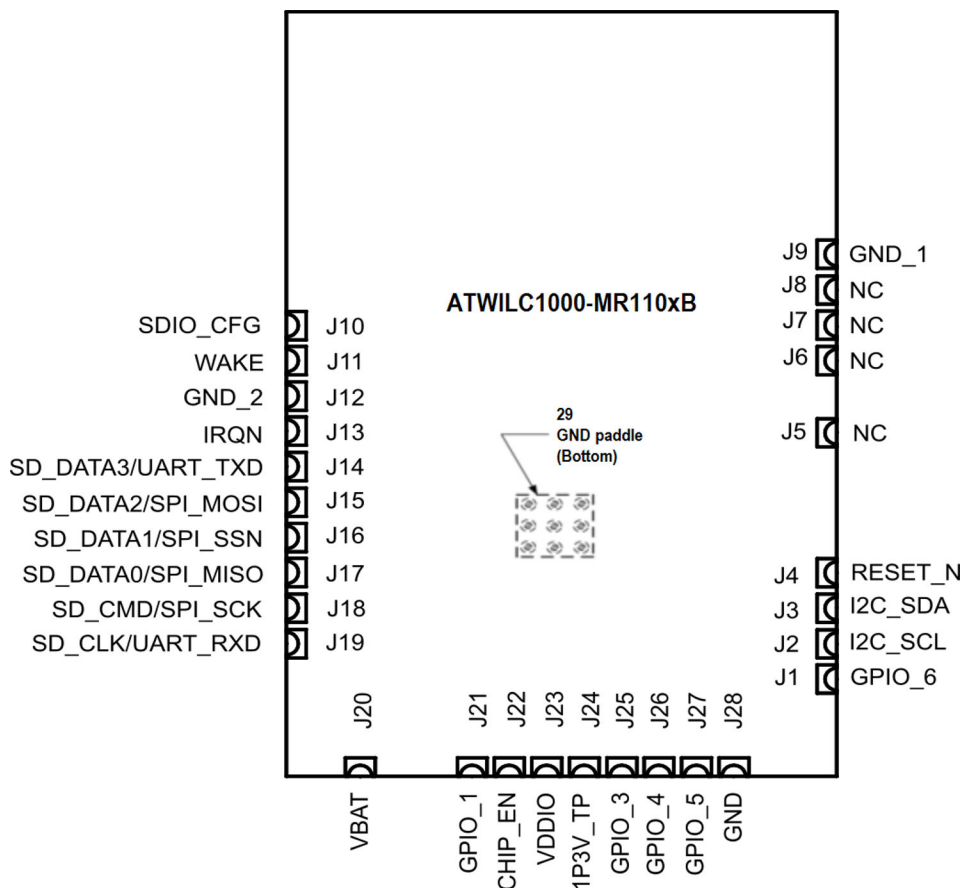
Note: This pin assignment is applicable for both ATWILC1000-MR110PB and ATWILC1000-MR110UB modules.

The following table describes the pin description of this module.

Table 3-1. Pin Details

Pin No.	Name	Type	Description	Programmable Pull up Resistor
1	GPIO_6	I/O	General purpose I/O.	-
2	I^{2}C_SCL	I/O	I^{2}C slave clock. Used only for development debug purposes. It is recommended to add test point for this pin.	-
3	I^{2}C_SDA	I/O	I^{2}C slave data. Used only for development debug purposes. It is recommended to add test point for this pin.	Yes
4	RESET_N	I	Active-low hard reset. When this pin is asserted low, the module is placed in the	Yes

Pin No.	Name	Type	Description	Programmable Pull up Resistor
			reset state. When this pin is asserted high, the module is out of reset and functions normally. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull down resistor to ensure a low level at power-up.	
5	NC	–	No connection	-
6	NC	–	No connection	-
7	NC	–	No connection	-
8	NC	–	No connection	-
9	GND_1	Ground	-	-
10	SDIO_SPI_CFG	I	Connect to VDDIO through a 1MΩ resistor to enable the SPI interface. Connect to ground to enable SDIO interface.	No
11	WAKE	I	Host wake control.	No
12	GND_2	Ground	-	-
13	IRQN	O	The ATWILC1000-MR110xB device interrupt output. Connect to a host interrupt pin.	No
14	SD_DAT3	SDIO=I/O UART=O	SDIO Data Line 3 from the ATWILC1000-MR110xB when module is configured for SDIO.	Yes
15	SD_DAT2/ SPI_RXD	SDIO=I/O SPI=I	SDIO Data Line 2 signal from ATWILC1000-MR110xB when module is configured for SDIO. SPI MOSI (Master Out Slave In) pin when module is configured for SPI.	Yes
16	SD_DAT1/ SPI_SSN	SDIO=I/O SPI=I	SDIO Data Line 1 from ATWILC1000-MR110xB when module is configured for SDIO. Active low SPI slave select from the ATWILC1000 when module is configured for SPI.	Yes
17	SD_DAT0/ SPI_TXD	SDIO=I/O SPI=O	SDIO Data Line 0 from the ATWILC1000-MR110xB when module is configured for SDIO. SPI MISO (Master In Slave Out) pin from ATWILC1000 when module is configured for SPI.	Yes
18	SD_CMD/ SPI_CLK	SDIO=I/O	SDIO CMD line from ATWILC1000-MR110xB when module is configured for	Yes

Pin No.	Name	Type	Description	Programmable Pull up Resistor
		SPI=I	SDIO. SPI Clock from ATWILC1000 when module is configured for SPI.	
19	SD_CLK	SDIO=I UART=I	SDIO clock line for the ATWILC1000-MR110xB when module is configured for SDIO.	Yes
20	VBATT	Power supply	Power supply pin for the DC/DC convertor	Yes
21	GPIO_1	I/O	General purpose I/O	Yes
22	CHIP_EN	I	Module enable. High level enables module, low level places module in power-down mode. Connect to a host Output that defaults low at power-up. If the host output is tri-stated, add a 1MΩ pull down resistor if necessary to ensure a low level at power-up.	No
23	VDDIO	Power supply	I/O power supply. Must match host I/O voltage.	-
24	1P3V_TP	-	1.3V VDD Core Test Point. Decouple with 10uF and 0.01uF to GND	
25	GPIO_3	I/O	General purpose I/O. By default, UART receive input to ATWILC1000-MR110xB. Used only for development debug purposes. It is recommended to add test point for this pin.	Yes
26	GPIO_4	I/O	General purpose I/O.	Yes
27	GPIO_5	I/O	General purpose I/O. By default, UART transmit output from ATWILC1000-MR110xB. Used only for development debug purposes. It is recommended to add test point for this pin.	Yes
28	GND_3	Ground	-	-
29	Paddle	Ground	Exposed paddle GND. This pad must be soldered to system ground	-

The following table provides the ATWILC1000-MR110xB module package dimensions

Table 3-2. ATWILC1000-MR110xB Module Package Information

Parameter	Value	Units
Package Size	21.72 x 14.73	mm
Pad Count	28	-

Parameter	Value	Units
Total Thickness	2.11	mm
Pad Pitch	1.016	
Pad Width	0.82	
Exposed Pad size	3.7 x 3.7	

4. Electrical Specifications

4.1 Absolute Ratings

The absolute maximum ratings for this module are listed in the following table.

Table 4-1. ATWILC1000-MR110xB Module Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	5.0	V

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

4.2 Recommended Operating Conditions

The recommended operating conditions for this module is listed in the following table.

Table 4-2. ATWILC1000-MR110xB Module Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit
VBATT	3.0	3.3	4.2	V
VDDIO	1.8	3.3	3.6	V
Operating temperature	-40		+85	ºC

Note:
1. VBATT should be equal to or greater than VDDIO.
2. The voltage of VDDIO is dependent on system I/O voltage.
3. Test Conditions: -40ºC to +85ºC

4.3 Receiver Performance

The following are typical conditions for radio receiver performance:

VBATT at 3.3 V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6(2437 MHz).

The following table provides the receiver performance characteristics for this module.

Table 4-3. Receiver Performance

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	-	2,412	-	2,472	MHz
Sensitivity 802.11b	1 Mbps DSSS	-	-94	-	dBm
	2 Mbps DSSS	-	-91	-	
	5.5 Mbps DSSS	-	-89	-	
	11 Mbps DSSS	-	-86	-	
Sensitivity 802.11g	6 Mbps OFDM	-	-88	-	dBm
	9 Mbps OFDM	-	-87	-	
	12 Mbps OFDM	-	-86	-	
	18 Mbps OFDM	-	-84	-	
	24 Mbps OFDM	-	-82	-	
	36 Mbps OFDM	-	-78	-	
	48 Mbps OFDM	-	-74	-	
	54 Mbps OFDM	-	-73	-	
Sensitivity 802.11n (BW at 20 MHz)	MCS 0	-	-87	-	dBm
	MCS 1	-	-85	-	
	MCS 2	-	-83	-	
	MCS 3	-	-80	-	
	MCS 4	-	-76	-	
	MCS 5	-	-73	-	
	MCS 6	-	-71	-	
	MCS 7	-	-69	-	
Maximum Receive Signal Level	1-11 Mbps DSSS		0	-	dBm
	6-54 Mbps OFDM		-5	-	
	MCS 0 – 7		-5	-	
Adjacent Channel Rejection	1 Mbps DSSS (30 MHz offset)	-	50	-	dB
	11 Mbps DSSS (25 MHz offset)	-	43	-	
	6 Mbps OFDM (25 MHz offset)	-	40	-	
	54 Mbps OFDM (25 MHz offset)	-	25	-	
	MCS 0 – 20 MHz BW (25 MHz offset)	-	40	-	
	MCS 7 – 20 MHz BW (25 MHz offset)	-	20	-	
Cellular Blocker Immunity	776-794 MHz CDMA	-	-14	-	dBm
	824-849 MHz GSM	-	-10	-	

Parameter	Description	Min.	Typ.	Max.	Unit
	880-915 MHz GSM	-	-10	-	
	1710-1785 MHz GSM	-	-15	-	
	1850-1910 MHz GSM	-	-15	-	
	1850-1910 MHz WCDMA	-	-24	-	
	1920-1980 MHz WCDMA	-	-24	-	

4.4 Transmitter Performance

The following are typical conditions for radio transmitter performance:

VBATT at 3.3 V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6(2437 MHz).

The following table provides the transmitter performance characteristics for this module.

Table 4-4. Transmitter Performance

Parameter	Description	Unit	Minimum	Typical	Maximum
Frequency	-	MHz	2,412	-	2,472
Output Power[1-2], ON_Transmit	802.11b 1Mbps	dBm	-	17.6	-
	802.11b 11Mbps	dBm	-	18.2	-
	802.11g 6Mbps	dBm	-	18.7	-
	802.11g 54Mbps	dBm	-	16.7	-
	802.11n MCS 0	dBm	-	17.3	-
	802.11n MCS 7	dBm	-	13.8	-
Tx Power Accuracy	-	dB	-	±1.5[2]	-
Carrier Suppression	802.11b mode	dBc	-	-19.4	-
	802.11g mode	dBc	-	-27.5	-
	802.11n mode	dBc	-	-21.1	-
Out of Band Transmit Power	76-108	dBm/Hz	-	-125	-
	776-794	dBm/Hz	-	-125	-
	869-960	dBm/Hz	-	-125	-
	925-960	dBm/Hz	-	-125	-
	1570-1580	dBm/Hz	-	-125	-
	1805-1880	dBm/Hz	-	-125	-
	1930-1990	dBm/Hz	-	-125	-
	2110-2170	dBm/Hz	-	-125	-

Parameter	Description	Unit	Minimum	Typical	Maximum
Harmonic Output Power[4]	2nd	dBm/MHz	-	-28	-
	3rd	dBm/MHz	-	-33	-
	4th	dBm/MHz	-	-40	-
	5th	dBm/MHz	-	-28	-

Note:

1. Measured at 802.11 spec compliant EVM/Spectral Mask
2. Measured after RF matching network
3. Operating temperature range is -40°C to +85°C. RF performance is guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. Measured at 11Mbps, DG(Digital Gain)= -7, WLAN Channel 6 (2437 MHz).
5. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
6. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

4.5   Timing Characteristics

4.5.1   SPI Timing

The SPI slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table.

Table 4-5. SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

The red lines in the following figure correspond to clock phase at 0 and the blue lines correspond to clock phase at 1.

Figure 4-1. SPI Slave Clock Polarity and Clock Phase Timing
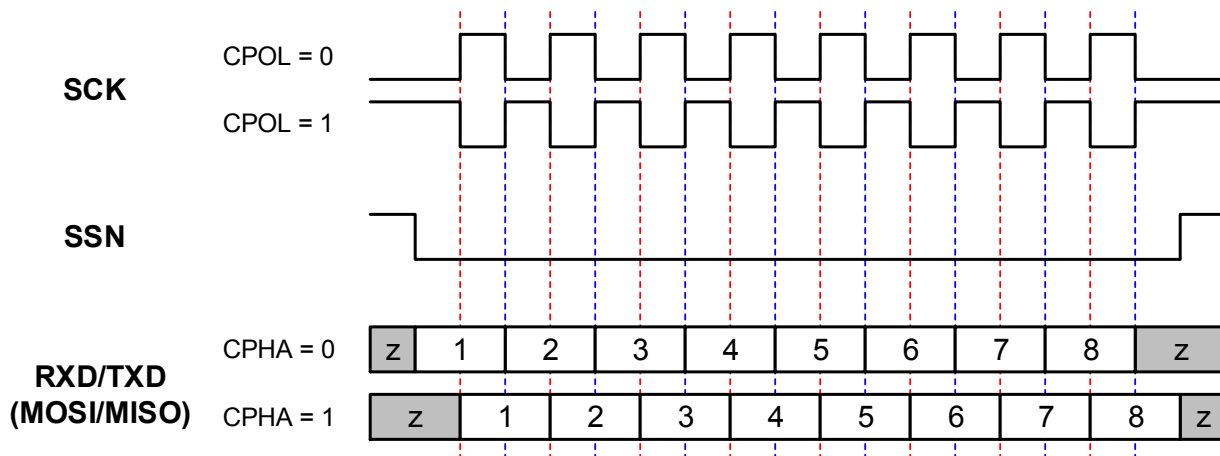
The SPI timing is shown in the following figure.

Figure 4-2. SPI Timing Diagram (SPI MODE CPOL=0, CPHA=0)
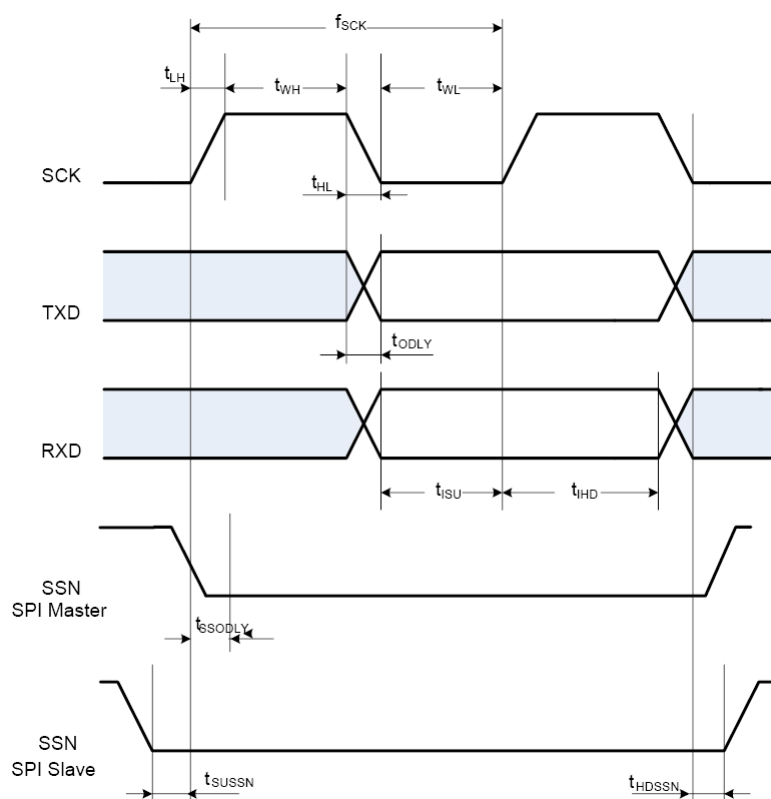
The SPI timing parameters are provided in the following table.

Table 4-6. SPI Slave Timing Parameters[1]

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency[2]	f_{SCK}	-	48	MHz
Clock Low Pulse Width	t_{WL}	4	-	ns
Clock High Pulse Width	t_{WH}	5	-	

Parameter	Symbol	Min.	Max.	Units
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay[3]	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD Input Setup Time	t_{ISU}	1	-	
RXD Input Hold Time	t_{IHD}	5	-	
SSN Input Setup Time	t_{SUSSN}	3	-	
SSN Input Hold Time	t_{HDSSN}	5.5	-	

Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15pF output loading.

4.5.2 SDIO Timing

The SDIO Slave interface timing is shown in following figure.

Figure 4-3. SDIO Timing Diagram
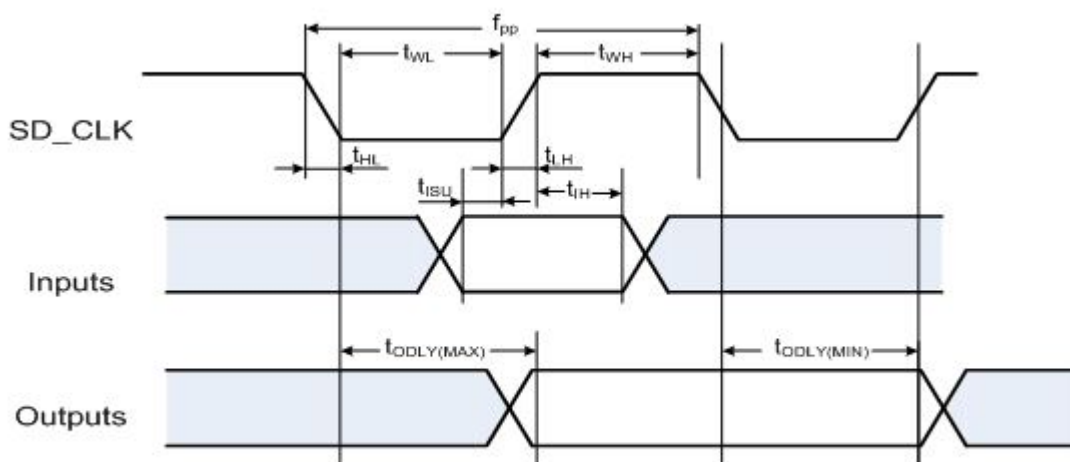
Slave timing parameters are provided in the following table.

Table 4-7. SDIO Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock Input Frequency[1]	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	9	-	ns

Parameter	Symbol	Min	Max	Units
Clock High Pulse Width	t_{WH}	4.5	-	
Clock Rise Time	t_{LH}	0	5	
Clock Fall Time	t_{HL}	0	5	
Input Setup Time	t_{ISU}	6	-	
Input Hold Time	t_{IH}	4	-	
Output Delay[2]	t_{ODLY}	3	11	

1.   Maximum clock frequency specified is limited by the SDIO Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
2.   Timing based on 15pF output loading.

4.5.3 I^2C Timing

The following figure illustrates I^2C Slave timing.

Figure 4-4. I^2C Timing Diagram
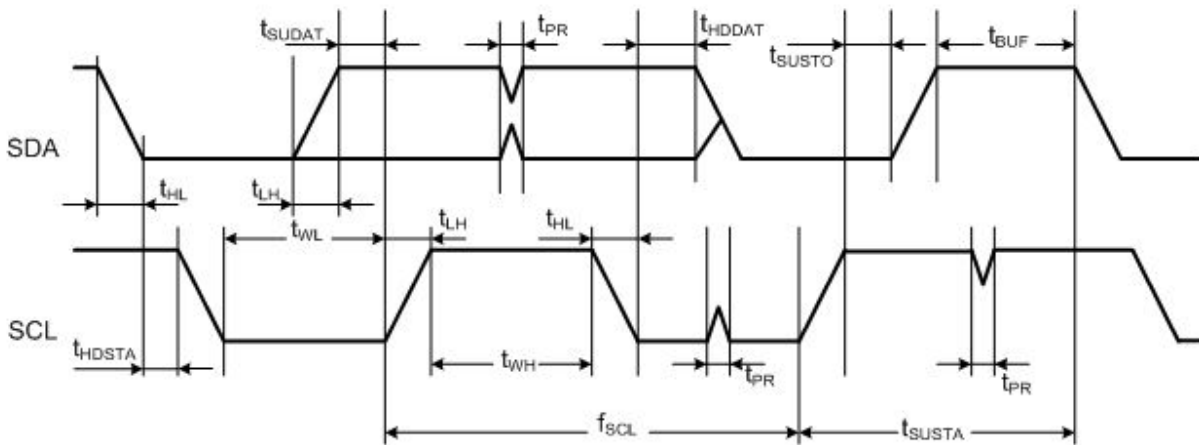
The following table provides I^2C Slave timing parameters.

Table 4-8. I2C Timing Parameters

Parameter	Symbol	Min	Max	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHZ	-
SCL Low Pulse Width	t_{WL}	1.3	-	µs	-
SCL High Pulse Width	t_{WH}	0.6	-	µs	-
SCL, SDA Fall Time	t_{HL}	-	300	ns	-

Parameter	Symbol	Min	Max	Units	Remarks
SCL, SDA Rise Time	t_{LH}	-	300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6	-	µs	-
START Hold Time	t_{HDSTA}	0.6	-	µs	-
SDA Setup Time	t_{SUDAT}	100	-	ns	-
SDA Hold Time	t_{HDDAT}	0	-	ns	Slave and Master Default
		40	-	ns	Master Programming Option
STOP Setup time	t_{SUSTO}	0.6	-	µs	-
Bus Free Time Between STOP and START	t_{BUF}	1.3	-	µs	-
Glitch Pulse Reject	t_{PR}	0	50	ns	-

5.   Power Management

The ATWILC1000-MR110xB module has several device states:

- • On states:
    - – ON_Transmit – device actively transmits an 802.11 signal. Highest output power and nominal current consumption.
    - – ON_Receive – device actively receives an 802.11 signal. Lowest sensitivity and nominal current consumption.
    - – ON_Doze – device is powered on but it does not actively transmit or receive the data.
    - – Power_Down – device core supply is powered off.

The following pins are used to switch between the ON and Power_Down states:

- • CHIP_EN – this pin (pin 22) enables or disables the DC/DC converter.
- • VDDIO – I/O supply voltage from external supply.

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power down sequence mentioned in Power-Up/Down Sequence. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see Restrictions for Power States).

5.1   Current Consumption in Various Device States

The following table provides this module's current consumption in various device states.

Table 5-1. Current Consumption

Device State	Code Rate	Output Power (dBm)	Current Consumption[1]	
			I_{VBATT}	I_{VDDIO}
ON_Transmit	802.11b 1Mbps	17.6	266 mA	22 mA
	802.11b 11Mbps	18.5	239 mA	22 mA
	802.11g 6Mbps	18.6	249 mA	22 mA
	802.11g 54Mbps	16.9	173 mA	22 mA
	802.11n MCS 0	17.7	253 mA	22 mA
	802.11n MCS 7	14.0	164 mA	22 mA
ON_Receive	802.11b 1Mbps	N/A	63 mA	22 mA
	802.11b 11Mbps	N/A	63 mA	22 mA
	802.11g 6Mbps	N/A	63 mA	22 mA
	802.11g 54Mbps	N/A	63 mA	22 mA
	802.11n MCS 0	N/A	63 mA	22 mA
	802.11n MCS 7	N/A	63 mA	22 mA

Device State	Code Rate	Output Power (dBm)	Current Consumption[1]	
ON_Doze	N/A	N/A	380µA	<10µA
Power_Down	N/A	N/A	1.25 uA[2]	

Note:

1. The power consumption values are measured when VBAT is 3.3V and VDDIO is 3.3V at 25°C.
2. Current consumption mentioned for these states is the sum of current consumed in VDDIO and VBAT voltage rails.

5.2   Restrictions for Power States

When no power is supplied to the device, the DC/DC Converter output and VDDIO are both turned off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Sleep mode or power-down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

5.3   Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWILC1000-MR110xB module.

Figure 5-1. Power-Up/Down Sequence
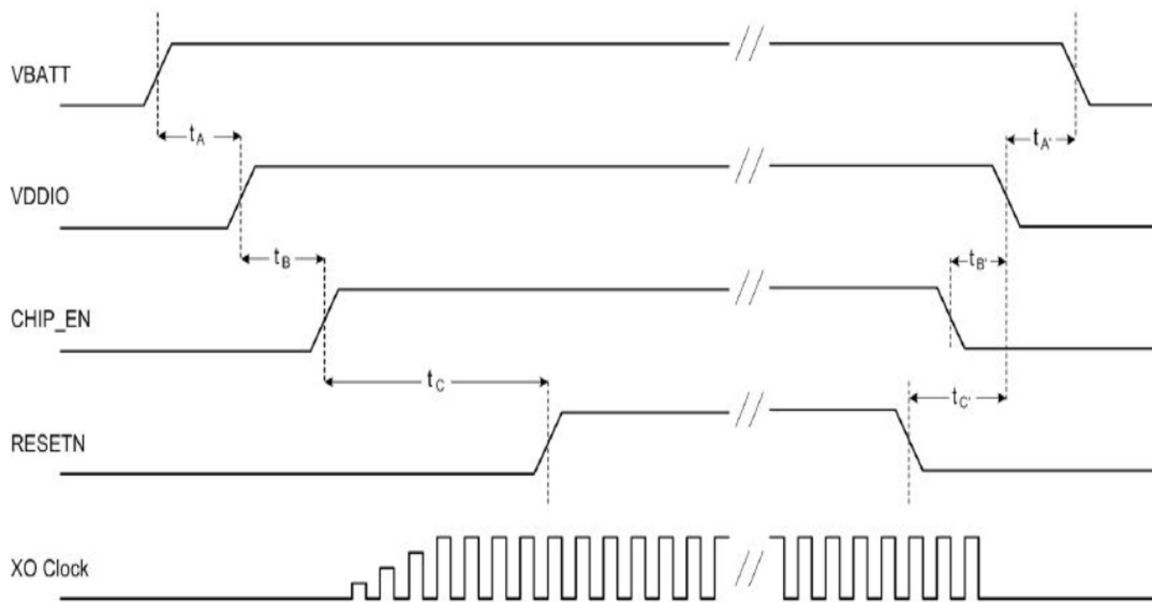
The following table provides power-up/down sequence timing parameters.

Table 5-2.   Power-Up/Down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0	-	ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.
t_B	0	-	ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.
t_C	5	-	ms	CHIP_EN rise to RESETN rise	This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.
$t_{A'}$	0	-	ms	VDDIO fall to VBAT fall	VBAT and VDDIO fall simultaneously or connected together. VBAT must not fall before VDDIO.
$t_{B'}$	0	-	ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.
$t_{C'}$	0	-	ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.

5.4   Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 5-3. Digital I/O Pin Behavior in Different Device States

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96 kOhm)
Power_Down: core supply OFF	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply and hard reset ON	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply ON, device out of reset and not programmed	High	High	High	Disabled (Hi-Z)	Enabled	Enabled
On_Doze/ On_Transmit/	High	High	High	Programmed by firmware for each pin: enabled or disabled	Opposite of Output Driver state	Programmed by firmware for each pin: enabled or disabled

Device State	VDDIO	CHIP_EN	RESETN	Output Driver	Input Driver	Pull Up/Down Resistor (96 kOhm)
On_Receive: core supply ON, device programmed by firmware						

6. CPU and Memory Subsystems

6.1 Processor

This ATWILC1000-MR110xB module has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions including but not limited to association, authentication, power management, security key management, and MSDU aggregation/deaggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

6.2 Memory Subsystem

The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC that allows the APS3 core to perform various data management tasks on the Tx and Rx data packets.

6.3 Nonvolatile Memory (eFuse)

This ATWILC1000-MR110xB module has 768 bits of nonvolatile eFuse memory that is read by the CPU after device reset. This nonvolatile One-Time-Programmable (OTP) memory is used to store customer specific parameters, such as MAC address; various calibration information, such as Tx power, crystal frequency offset etc; and other software-specific configuration parameters. The eFuse is partitioned into six 128 bit banks. Each bank has the same bit map, mentioned in the following figure. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general purpose software dependent bits. Each bank is programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of TX gain correction and Frequency offset if they are used and programmed in the Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the Invalid bit in the Bank 0. This will allow the firmware to use the MAC address from Bank 1.

By default, all the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules are programmed with the MAC address and the Frequency offset bits of Bank 0.

Figure 6-1. eFuse Bit Map
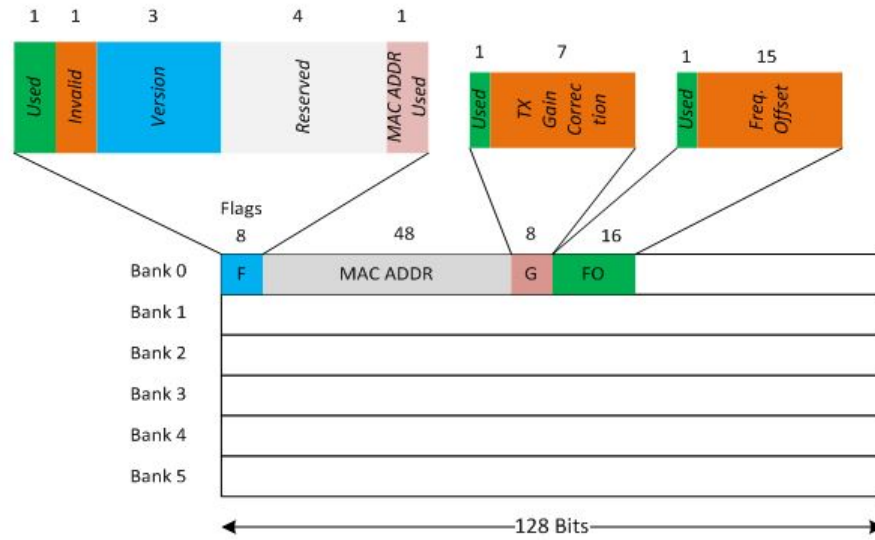
7. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY), and the radio.

7.1 MAC

7.1.1 Description

This module is designed to operate at low power, while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement data path functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES and WPA2 Enterprise security requirements.

Control functions, which have real time requirements, are implemented using hardwired control logic modules. These logic modules offer real time response while maintaining configurability through the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon Tx control, interframe spacing, and so on), protocol timer module (responsible for the Network Access vector, back-off timing, timing synchronization function, and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication), and Tx/Rx control Finite State Machine (FSM) (coordinate data movement between PHY and MAC interface, cipher engine, and the Direct Memory Acces (DMA) interface to the Tx/Rx FIFOs).

Following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real time requirements. Examples are authentication and association.
- Functions that require flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

7.1.2 Features

The ATWILC1000-MR110xB IEEE 802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
    - Transmission and reception of aggregated MPDUs (A-MPDU)
    - Transmission and reception of aggregated MSDUs (A-MSDU)
    - Immediate block acknowledgment
    - Reduced Interframe Spacing (RIFS)
- Supports IEEE 802.11i and WFA security with key management

- – WEP 64/128
- – WPA-TKIP
- – 128-bit WPA2 CCMP (AES)
- – WPA2 Enterprise
- Advanced power management
  - – Standard IEEE 802.11 Power save mode
  - – Wi-Fi alliance WMM-PS (U-APSD)
- RTS-CTS and CTS self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports concurrent mode of operation
- Supports Independent Basic Service Set (IBSS)

7.2 PHY

The ATWILC1000-MR110xB module WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

Features

The IEEE 802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20 MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11 Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, and 54 Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20 MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
- IEEE 802.11n mixed mode operation
- Per packet Tx power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery and frame detection

7.2.1 Features

The IEEE 802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20 MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11 Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12,18, 24, 36, 48, and 54 Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20 MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
- IEEE 802.11n mixed mode operation
- Per packet Tx power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery and frame detection

7.3 Radio

This section describes the properties and characteristics of the ATWILC1000- MR110xB and Wi-Fi radio transmit and receive performance capabilities of the device. The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is guaranteed for room temperature of 25°C with a derating of 2-3dB at boundary conditions.

Measurements were taken under typical conditions: VBATT at 3.3V; VDDIO at 3.3V ,and temperature at +25ºC.

Table 7-1. Features and Properties

Feature	Description
Module Part Number	ATWILC1000-MR110xB
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host Interface	SPI, SDIO
Dimension	L x W x H: 21.7 x 14.7 x 2.1 (typical) mm
Frequency range	2.412 GHz ~ 2.472 GHz (2.4 GHz ISM band)
Number of channels	11 for North America, 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM/64-QAM,16-QAM, QPSK, BPSK
Data rate	802.11b: 1, 2, 5.5, 11 Mbps 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data rate (20 MHz ,short GI,400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2 Mbps
Operating temperature[1]	-40°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating humidity 10% to 95% non-condensing Storage humidity 5% to 95% non-condensing

Note:

1. RF performance is guaranteed at room temperature of 25°C with a 2-3db change at boundary conditions.

8.   External Interfaces

This section describes the various host and debug interfaces of the ATWILC1000-MR110xB module.

8.1   Interfacing with the Host Microcontroller

This section describes how to interface ATWILC1000-MR110xB module with the host microcontroller. The interface comprises of a slave SPI/SDIO and additional control signals, as shown in the figure. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 8-1. Interfacing with the Host Microcontroller

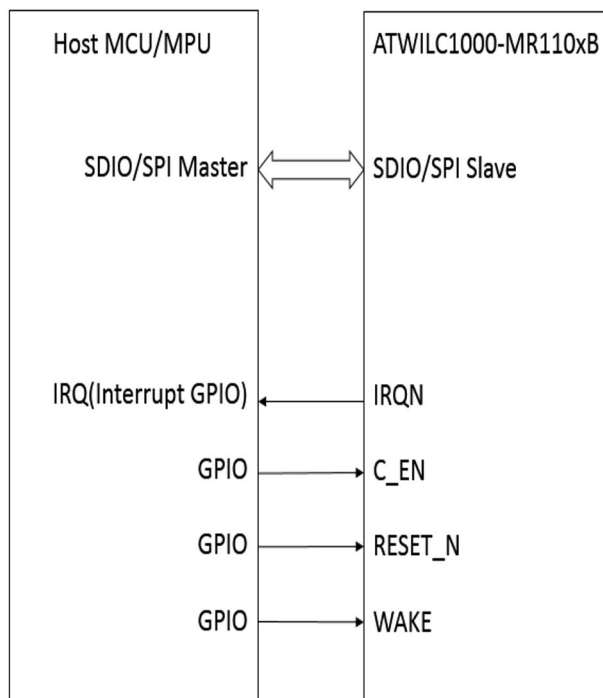**Table 8-1. Host Microcontroller Interface Pins**

Module Pin	Function[1]
4	RESET_N
11	WAKE
13	IRQ_N
22	CHIP_EN
16	SPI_SSN/SD_DATA1
15	SPI_MOSI/SD_DATA2
17	SPI_MISO/SD_DATA0
18	SPI_SCK/SD_CMD

Module Pin	Function[1]
14	SD_DATA3
19	SD_CLK

Note:
1. Logic input for module pin SDIO_SPI_CFG(10) determines whether SDIO or SPI slave interface is enabled. Connect SDIO_SPI_CFG to VDDIO through a 1MΩ resistor to enable the SPI interface. Connect SDIO_SPI_CFG to ground to enable SDIO interface.
2. It is recommended to place test points for pins I2C_SDA(3), I2C_SCL(2), GPIO_3(25) and GPIO_5(27) in the design.

8.2   SPI Slave Interface

The SPI slave interface can be enabled by connecting the SDIO_SPI_CFG pin to VDDIO. This SPI interface is used to exchange the control and 802.11 data. The SPI is a full duplex slave-synchronous serial interface that is available following reset when pin 10 (SDIO_SPI_CFG) is connected to VDDIO.

The SPI interface pin mapping configuration is provided in the following table.

Table 8-2. SPI Interface Pin Mapping

Pin #	SPI Function
10	SDIO_SPI_CFG: Must be connected to VDDIO
16	SSN: Active-Low Slave Select
15	MOSI: Serial Data Receive
18	SCK: Serial Clock
17	MISO: Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial master and other serial slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip and also initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of this module have internal programmable pull up resistors. These resistors are programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while this module is in the low power sleep state, current will flow from the VDDIO supply through the pull up resistors, increasing the current consumption of the module.

8.3   SDIO Slave Interface

The SDIO interface is enabled by connecting the SDIO_SPI_CFG pin to ground. This SDIO interface is used to exchange the control and 802.11 data.. The SDIO interface is available after reset when pin 10 (SDIO_SPI_CFG) is connected to ground.

This SDIO is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50 MHz. The host uses this interface to read and write from any register within the chip and also configures this module for DMA data transfer.

The SDIO interface pin mapping configuration is provided in the following table.

Table 8-3. ATWILC1000 SDIO Interface Pin Mapping

Pin #	SDIO Function
10	SDIO_SPI_CFG: Must be connected to ground
14	DAT3: Data 3
15	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

The SDIO card is detected when the it is inserted into an SDIO host. During the normal initialization and interrogation of the card by the host, the card identifies itself as an SDIO device. The host software obtains the card information in a tuple (linked list) format and determines if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it is allowed to power-up fully and start the I/O function(s) built into the card.

The SD memory card communication is based on an advanced 9-pin interface (clock, command, four data and three power lines) designed to operate at maximum operating frequency of 50 MHz.

8.3.1   Features

- Compliant with SDIO card specification version 2.0
- Host clock rate variable between 0 and 50 MHz
- Supports 1-bit/4-bit SD bus modes
- Allows card to interrupt host
- Responds to direct read/write (IO52) and extended read/write (IO53) transactions
- Supports suspend/resume operation

8.4   UART Debug Interface

This module has a Universal Asynchronous Receiver/Transmitter (UART) interface on J25(RxD) and J27(TxD) pins. This interface should be used only for debugging purposes. The UART is compatible with the RS-232 standard, where ATWILC1000-MR110xB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWILC1000-MR110xB is mentioned below:

- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has Rx and Tx FIFOs, which ensures reliable high speed reception and low software overhead transmission. FIFO size is 4x8 for both Rx and Tx direction. The UART has status registers that show the

number of received characters available in the FIFO and various error conditions; in addition, it has the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 8-2. Example of UART RX or TX Packet
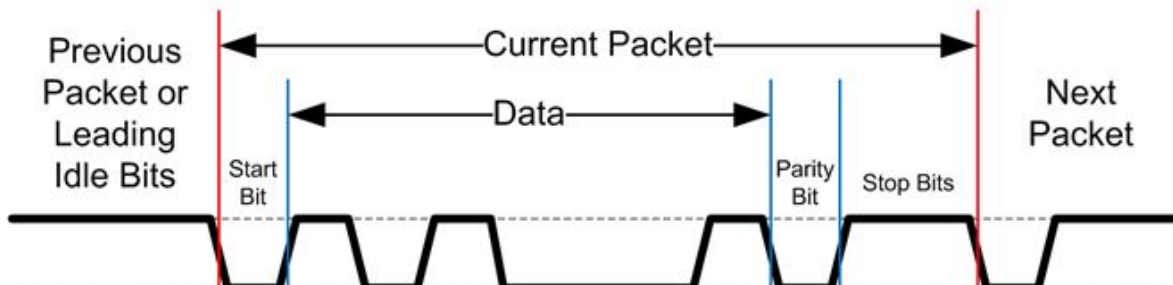
8.5   I^{2}C Slave Interface

This module provides an I^{2}C bus slave that allows for easy debugging of the ATWILC1000-MR110xB devices. It supports I^{2}C bus Version 2.1 – 2000.

The I^{2}C interface is used only for debug. This interface is a two-wire serial interface consisting of a serial data line (SDA, Pin 17) and a serial clock (SCL, Pin 18). It responds to seven bit address value 0x60. This module I^{2}C interface operates in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The I^{2}C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only when the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire AND functions on the bus. The devices on the bus are limited to the 400pF capacitance. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled "The I2C -Bus Specification, Version 2.1."

9.   Notes on Interfacing with the ATWILC1000-MR110xB

Programmable Pull up Resistors

The ATWILC1000-MR110xB module provides programmable pull up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which causes excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device must leave these pull up resistors enabled, so that the pin will not float. The default state at power-up is for the pull up resistor to be enabled; however, any pin that is used must have the pull up resistor disabled. The reason for this is that if any pins are driven to a low level while the device is in the low power sleep state, current flows from the VDDIO supply through the pull up resistors, increasing the current consumption of the module. Since the value of the pull up resistor is approximately 100 kOhm, the current through any pull up resistor that is being driven low is VDDIO/100K. For VDDIO = 3.3V, the current is approximately 33 µA. The pins that are used and have programmable the pull up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

10. Application Reference Design

This section provides reference schematic for ATWILC1000-MR110xB module with SPI and SDIO host interfaces.

Figure 10-1. ATWILC1000-MR110xB Reference Schetmatic - SDIO Host Interface
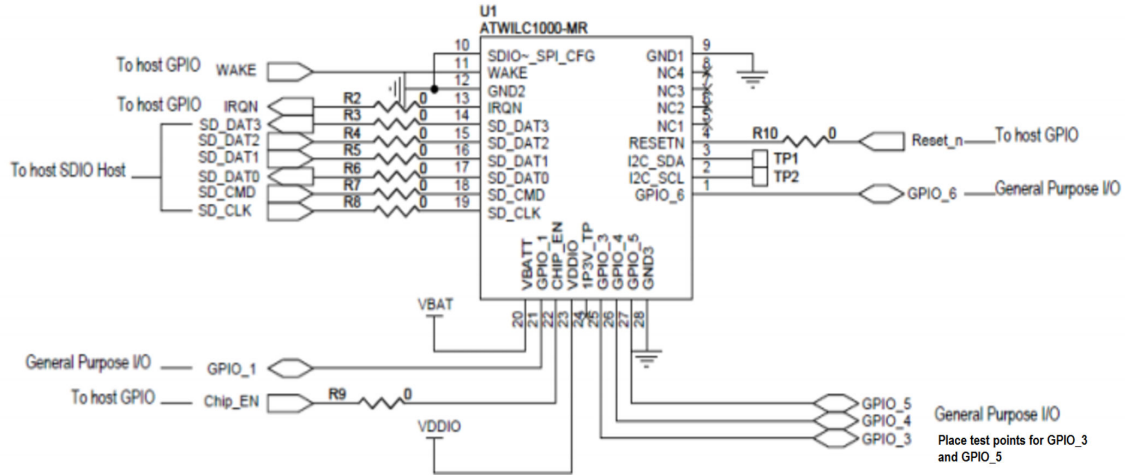
Table 10-1. ATWILC1000-MR110xB reference Schematic - SDIO Host Interface - Bill of Materials

Item	Qty.	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	9	R2, R3, R4,R5, R6, R7, R8, R9, R10	0 R	RESISTOR,Thick Film, 0 ohm, 0402	Yageo	RC0402JR-070RL	0402
2	1	U1	ATWILC1000-MR110xB	Wi-Fi Module	Microchip	ATWILC1000-MR110xB	

Figure 10-2. ATWILC1000-MR110xB Reference Schetmatic - SPI Host Interface
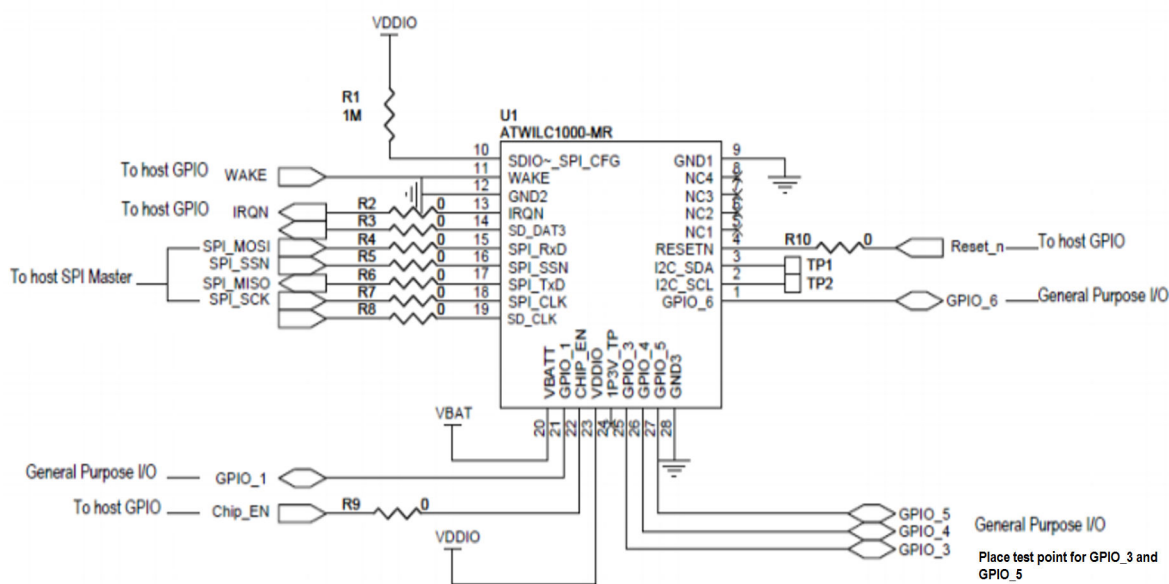
Table 10-2. ATWILC1000-MR110xB reference Schematic - SPI Host Interface - Bill of Materials

Item	Qty.	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	R1	1 M	RESISTOR ,Thick Film, 1 M ohm, 0402	Yageo	RC0100FR-071ML	0402
2	9	R2, R3, R4,R5, R6, R7, R8, R9, R10	0 R	RESISTOR ,Thick Film, 0 ohm, 0402	Yageo	RC0402JR-070RL	0402
3	1	U1	ATWILC1000-MR110xB	Wi-Fi Module	Microchip	ATWILC1000-MR110xB	

11.   Module Outline Drawings

The ATWILC1000-MR110PB module package details are outlined in the following figure. Dimensions are in mm.

Figure 11-1. Module Drawings – ATWILC1000-MR110PB - Top, Bottom and Side Views

MODULE TOP VIEW

MODULE SIDE VIEW

MODULE BOTTOM VIEW
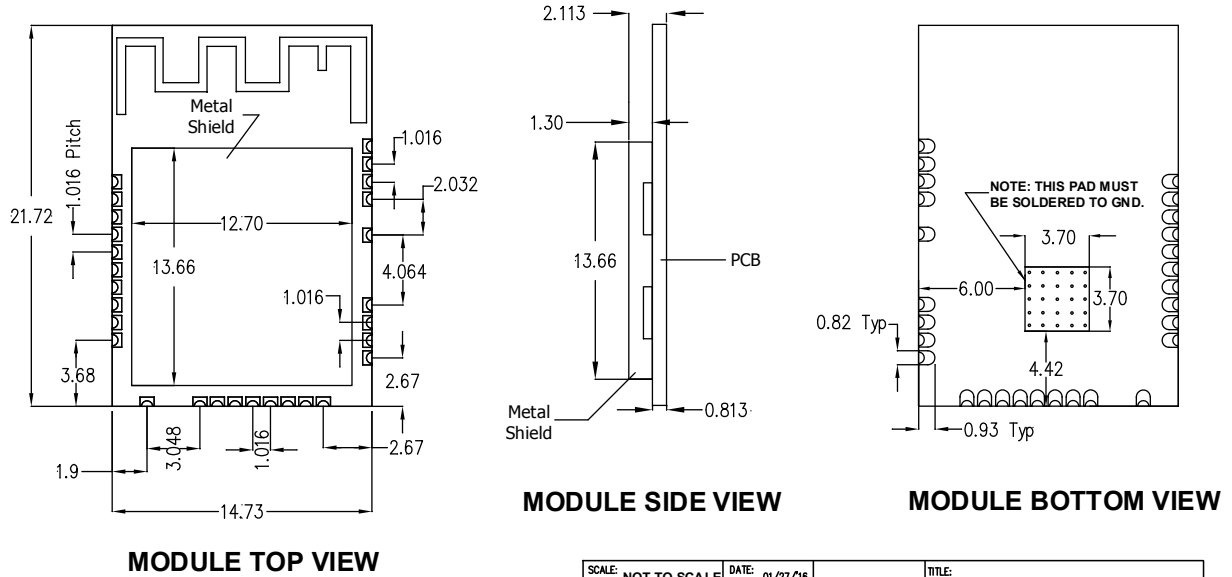
SCALE: NOT TO SCALE	DATE: 01/27/'16	TITLE:
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	WIFI MODULE PRINTED ANTENNA WITH LOW PROFILE SHIELD
PROJECTION UNLESS SPECIFIED		

The ATWILC1000-MR110UB module package details are outlined in the following figure. Dimensions are in mm.

Figure 11-2. Module Drawings – ATWILC1000-MR110UB - Top, Bottom and Side Views

MODULE TOP VIEW

MODULE SIDE VIEW

MODULE BOTTOM VIEW
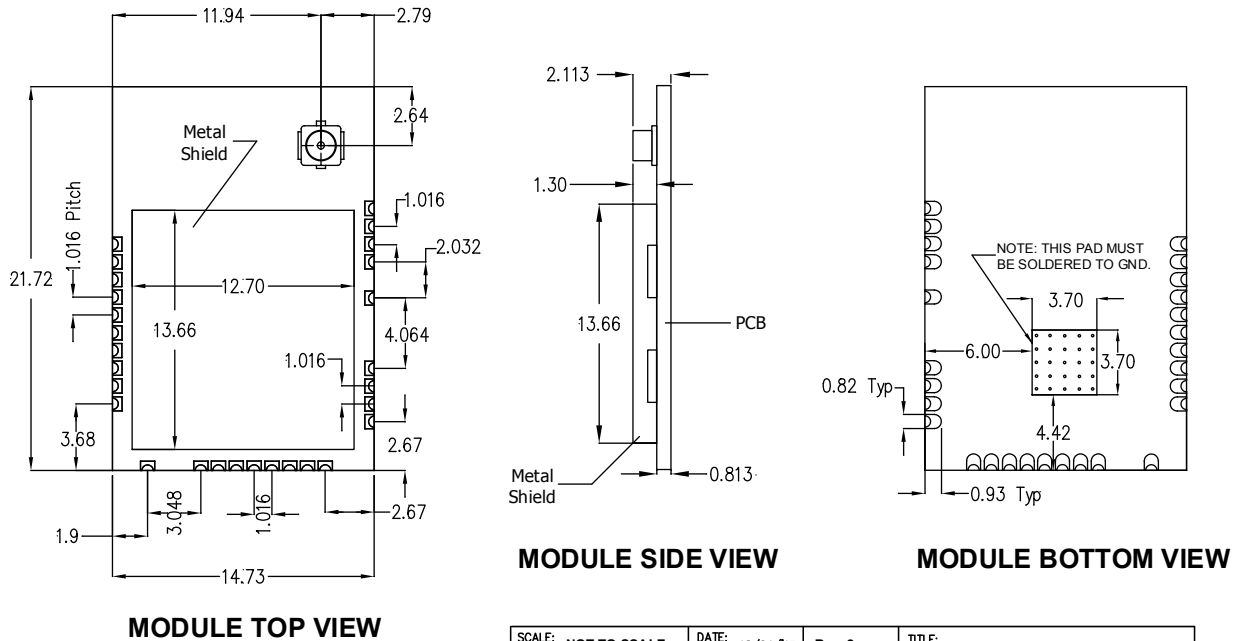
SCALE:	NOT TO SCALE	DATE:	12/04/'15	Rev. 2	TITLE:		
DIMENSIONAL UNIT:	MM	UNTOLERANCED DIMENSIONS			WIFI MODULE uFL ANTENNA WITH LOW PROFILE SHIELD		
PROJECTION UNLESS SPECIFIED							

This section provides the outline drawing for the recommended footprint for the ATWILC1000-MR110xB module. It is imperative that the center Ground Pad is provided, with an array of GND vias to provide a good ground and act as thermal sink for the ATWILC1000-MR110xB module.

Figure 11-3. Recommended Solder Pad Footprint

NOTE: THIS PAD MUST BE TIED TO GND.
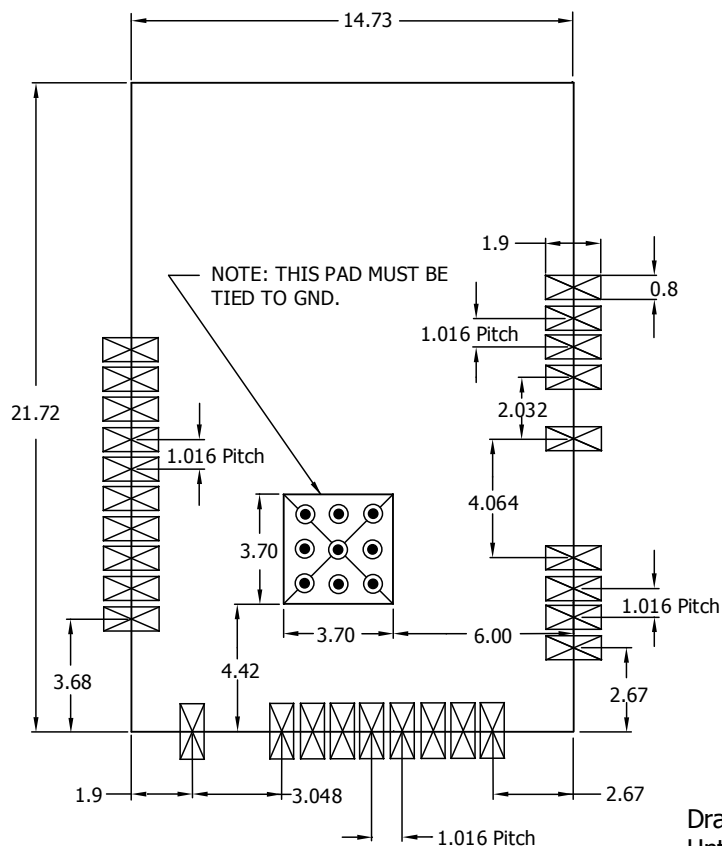
SOLDER PAD FOOTPRINT

Drawing not to scale.
Untoleranced dimensions.
Units=mm.

12.   Design Consideration

This section provides the guidelines on placement and routing to achieve the best performance.

12.1   ATWILC1000-MR110PB Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The module must be placed on host board, The printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not stick out over the edge of the host board. The antenna is designed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board. Figure 12-2 shows the best, poor and worst case module placements in host board.

- If the module is placed at the edge of the host board, a minimum 22mm by 5 mm area directly under the antenna must be clear of all metal on all layers of the board. "In-land" placement is acceptable; however, deepness of keep-out area must grove to: module edge to host board edge plus 5 mm.
  Note: Do not place the module in the middle of the host board or far away from the host board edge.

- Follow the module placement, keepout, host PCB cutout recommendation as shown in Figure 12-1
  - Avoid routing any traces in the highlighted region on the top layer of the host board which will be directly below the module area.
  - Follow the electrical keepout layer recommendation as shown in Figure 12-1. There should be no copper in all layers of the host board in this region. Avoid placing any components (like mechanical spacers, bumpon etc) in the recommended electrical keepout area.
  - Place GND polygon pour below the module with the recommended boundary in the top layer of the host board as shown in Figure 12-1. Do not have any breaks in this GND plane.
  - Place sufficient GND vias in the highlighted area below the module for better RF performance.
  - It is recommended to have a 3x3 grid of GND vias solidly connecting the exposed GND paddle of the module to the inner layer ground plane. This will act as a good ground and thermal conduction for the ATWILC1000-MR110PB module. The GND vias should have a minimum via hole size of 0.3mm.
  - Follow the mechanical boundary of the host PCB as shown in the Figure 12-1

- Keep the large metal objects away from antenna to avoid electromagnetic field blocking.
- Do not enclose the antenna within a metal shield.
- Keep any components which may radiate noise or signals within the 2.4 GHz – 2.5 GHz frequency band away from the antenna and if possible, shield those components. Any noise radiated from the host board in this frequency band will degrade the sensitivity of the module.
- Make sure the width of the traces routed to GND, VDDIO and VBAT rails are sufficiently larger for handling the peak Tx current consumption.

Figure 12-1. ATWILC1000-MR110PB Placement Reference
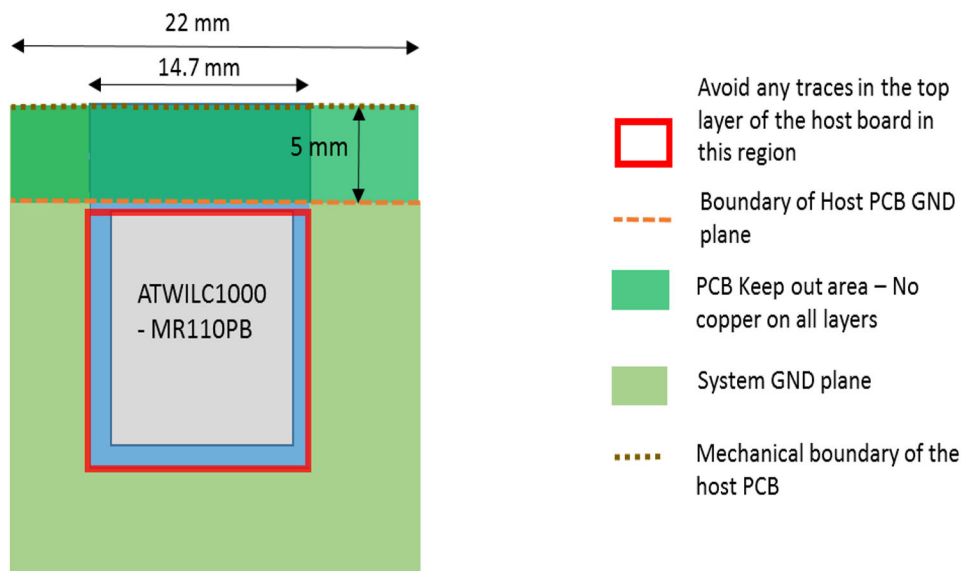
Figure 12-2. ATWILC1000-MR110PB Placement Example
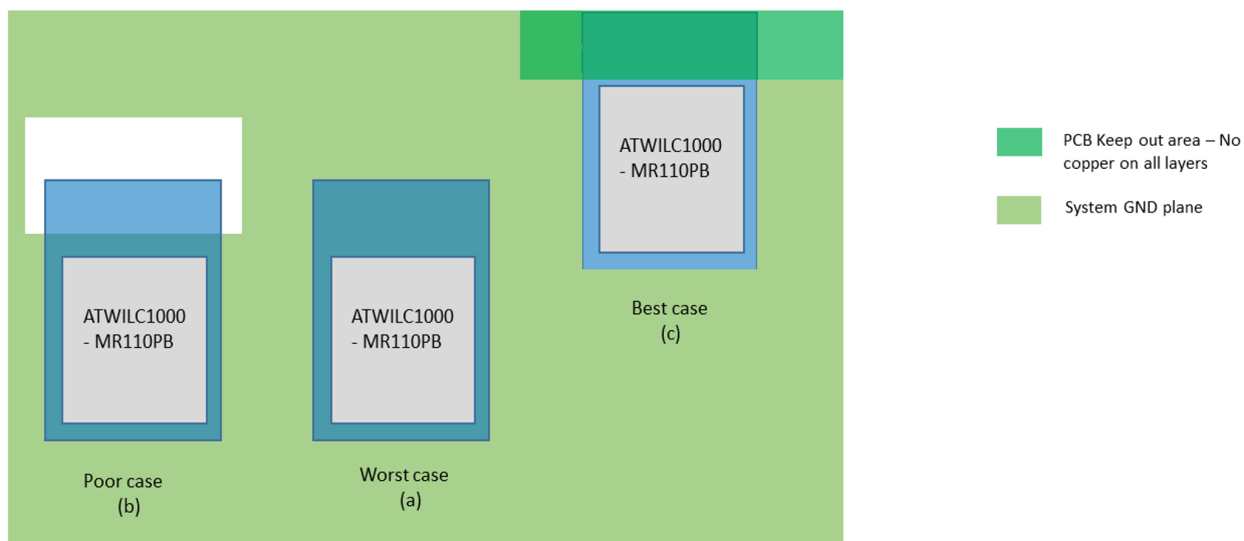
12.2 Printed PCB Antenna Performance of ATWILC1000-MR110PB

The printed PCB antenna on the ATWILC1000-MR110PB is a meandered Inverted F Antenna (IFA). The antenna is fed via matching network, which is matched for the module installed on 1.5mm thick main board. Main board thickness deviation by ±1mm changes RX/TX performance by ±1dB maximum referring to RX/TX performance with default antenna matching network and installed on 1.5mm thick main board.

Measured antenna gain is -0.3dBi.

Antenna Radiation Pattern

Following figures illustrate the antenna radiation pattern. During the measurement, the printed antenna is placed in the XZ plane with Y axis being perpendicular to the module and pointing to the back of the module.

Figure 12-3. Antenna Radiation Pattern when Phi = 0 degree
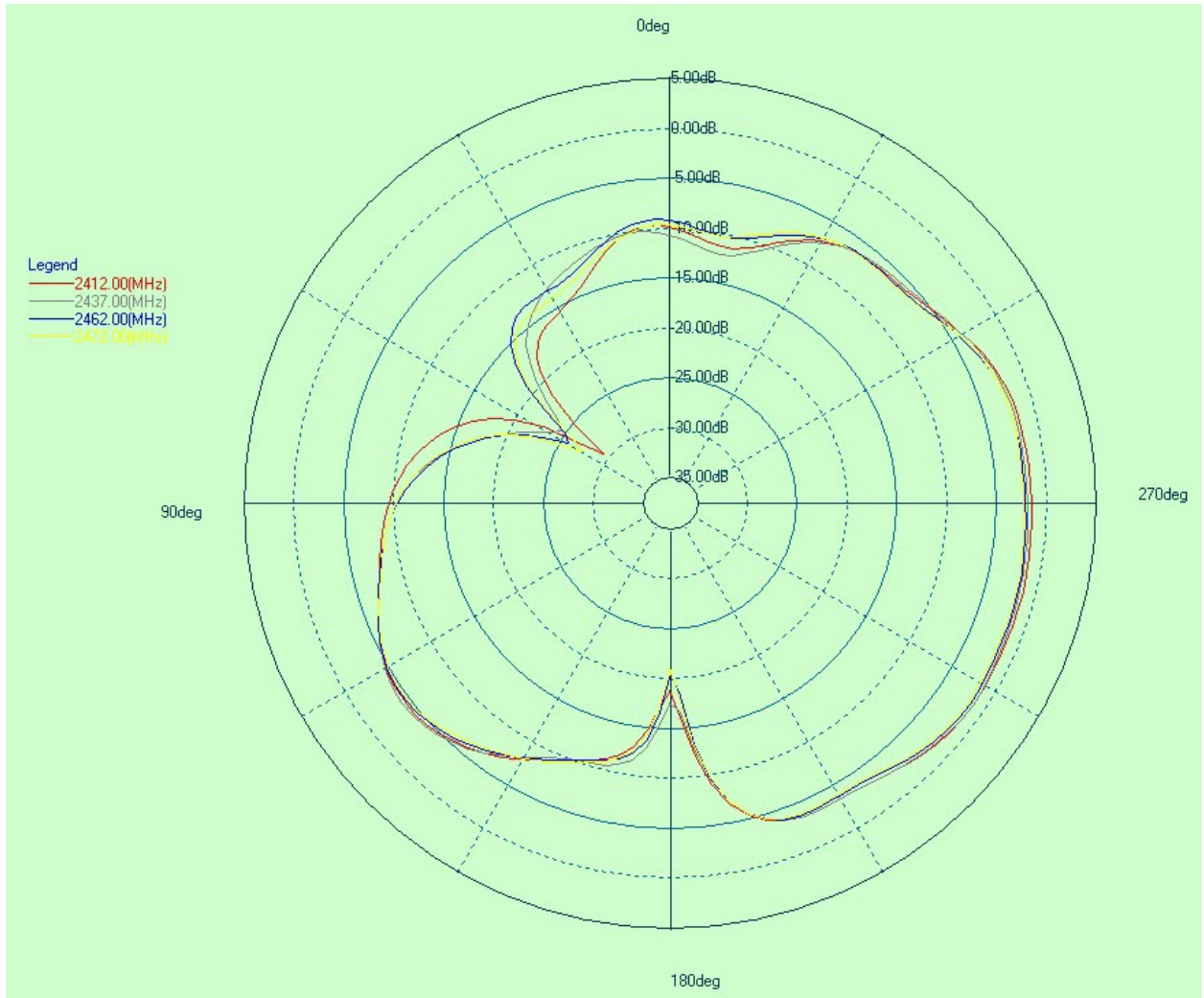
Figure 12-4. Antenna Radiation Pattern when Phi = 90 degree
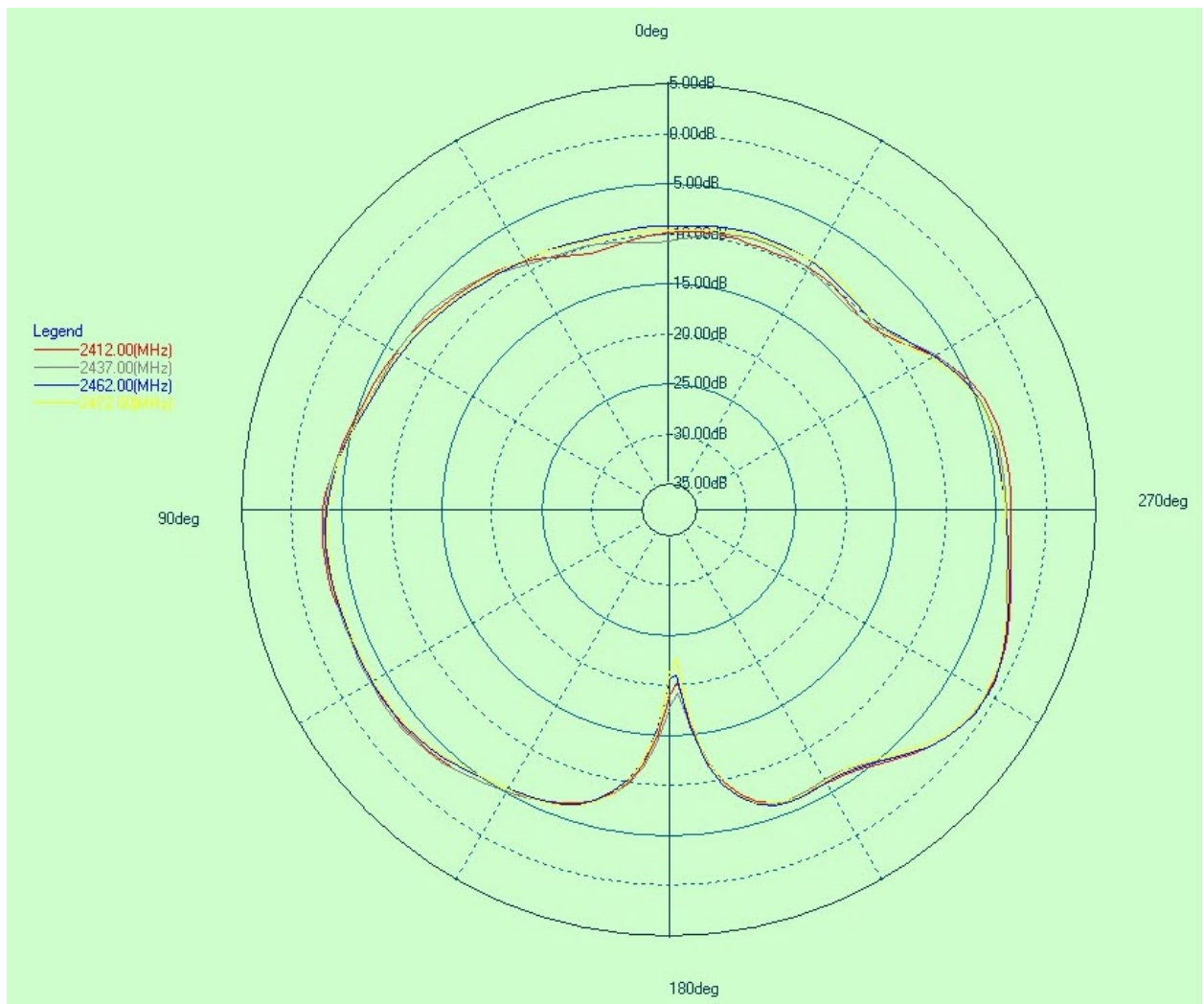
Figure 12-5. Antenna Radiation Pattern when Theta = 90 degree
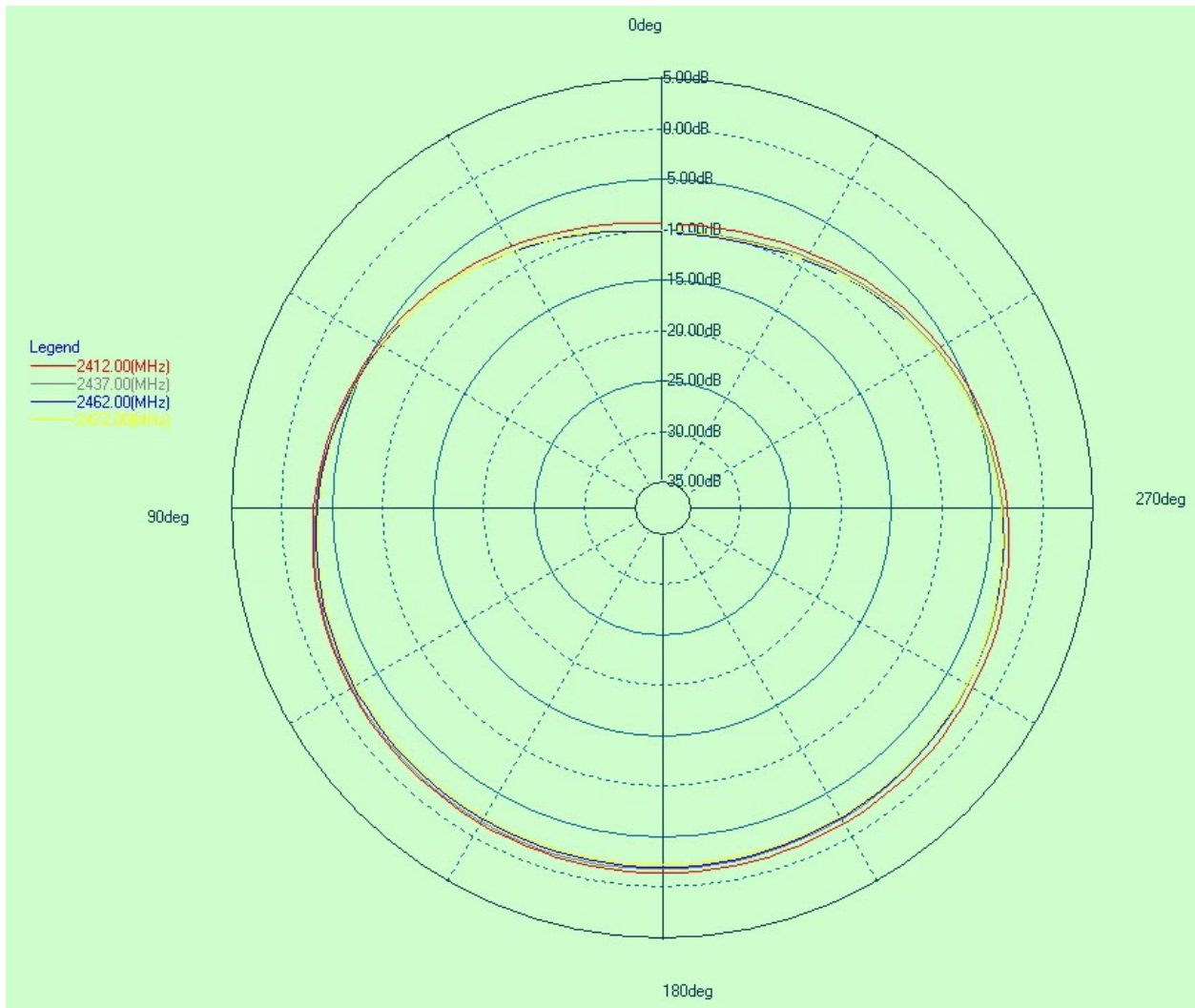
12.3.1   Recommended External Antenna for ATWILC1000-MR110UB

PCB Antenna (Part number: W3525B039) along with a 10cm length RF cable assembly (u.FL to SMA) has been used for the certification of ATWILC1000-MR110UB. It is recommended to use the same or similar external antenna in design.

13.   Reflow Profile Information

This section provides the guidelines for the reflow process to get the module soldered to the customer's design.

13.1   Storage Condition

13.1.1   Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

13.1.2   Moisture Barrier Bag Open

Humidity indicator cards must be blue, indicating that the humidity is <30%.

13.2   Solder Paste

SnAgCu eutectic solder with melting temperature of 217°C is most commonly used for lead-free solder reflow application. This alloy is widely accepted in the semiconductor industry due to its low cost, relatively low melting temperature, and good thermal fatigue resistance. Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.

13.3   Stencil Design

The recommended stencil is laser-cut, stainless-steel type with thickness of 100 µm to 130 µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25 µm larger than the top is utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

13.4   Printing Process

The printing process requires no significant changes compared to Sn/Pb solder. Any guidelines recommended by the paste manufacturers to accommodate paste specific characteristics should be followed. Post-print inspection and paste volume measurement is very critical to ensure good print quality and uniform paste.

13.5   Baking Conditions

This module is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours as long as the devices are held at ≤ 30°C/60% RH or stored at < 10% RH.

The module requires baking before mounting if:
- The sealed bag has been open for more than 168 hours
- The humidity indicator card reads more than 10%
- SIPs need to be baked for eight hours at 125°C

13.6 Soldering and Reflow Condition

Optimization of the reflow process is the most critical factor considered for lead-free soldering. The development of an optimal profile must account the paste characteristics, the size of the board, the density of the components, the mix of the larger and smaller components, and the peak temperature requirements of the components. An optimized reflow process is the key to ensuring a successful lead-free assembly and achieves high yield and long-term solder joint reliability.

Temperature Profiling

Temperature profiling must be performed for all new board designs by attaching thermocouples at the solder joints, on the top surface of the larger components, and at multiple locations of the boards. This is to ensure that all components are heated to a temperature above the minimum reflow temperatures and the smaller components do not exceed the maximum temperature limit. The SnAgCu solder alloy melts at ~217°C, so the reflow temperature peak at joint level must be 15 to 20°C higher than melting temperature. The targeted solder joint temperature for the SnAgCu solder must be ~235°C. For larger or sophisticated boards with a large mix of components, it is also important to ensure that the temperature difference across the board is less than 10 degrees to minimize board warpage. The maximum temperature at the component body must not exceed the MSL3 qualification specification.

13.6.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process.

1. Some recommended pastes include:
    –   NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu
    –   SENJU N705-GRN3360-K2-V Type 3, no clean paste
2. Allowable reflow soldering iterations:
    –   Three times based on the following reflow soldering profile (refer following Figure).
3. Temperature profile:
    –   Reflow soldering shall be done according to the following temperature profile (refer to the following figure).
    –   Peak temperature: 250°C.

Figure 13-1. Solder Reflow Profile
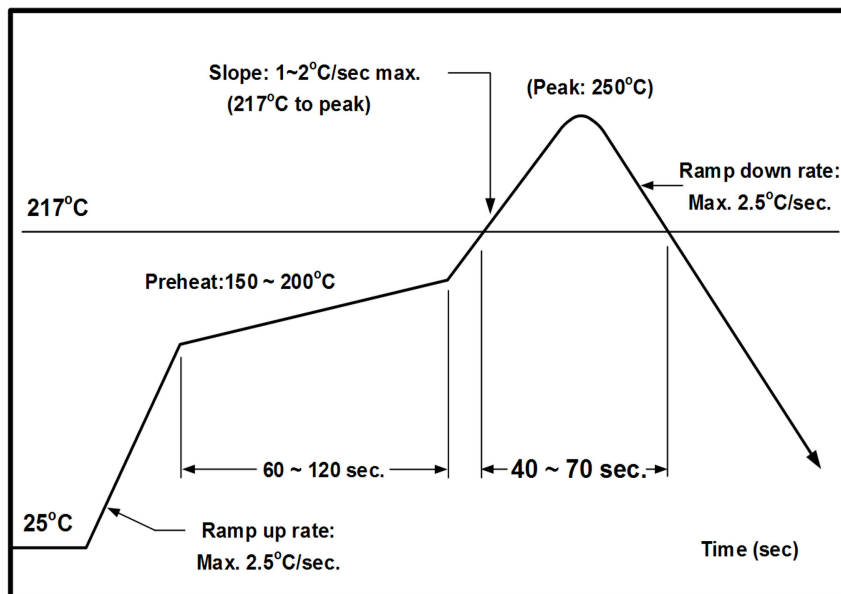
Cleaning

The exposed ground paddle helps to self-align the module, avoiding pad misalignment. The use of no-clean solder pastes is recommended. Full drying of no-clean paste fluxes must be ensured as a result of the reflow process. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window as recommended by the solder paste vendor. It is believed that uncured flux residues could lead to corrosion and/or shorting in accelerated testing and possibly the field.

Rework

Rework is to remove the mounted SIP package and replace with a new unit. It is recommended that once an ATWILC1000-MR110xB module has been removed it should never be reused. During the rework process, the mounted module and PCB are heated partially, and the module is removed. It is recommended to heat-proof the proximity of the mounted parts and junctions and use the best nozzle for rework that is suited to the module size.

14. Module Assembly Considerations

The ATWILC1000-MR110xB modules are assembled with an EMI Shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions like IPA and similar solvents can be used to clean the ATWILC1000-MR110xB module; however, cleaning solutions that contain acid should never be used on the module.

The ATWILC1000-MR110xB modules are manufactured without any conformal coating applied. It is the customer's responsibility if a conformal coating is specified and applied to the ATWILC1000- MR110xB module.

15. Regulatory Approval

Regulatory approvals received:

ATWILC1000-MR110PB

- United States/FCC ID: 2ADHKATWILC1000
- Canada/ISED
    - IC: 20266-ATWILC1000
    - HVIN: ATWILC1000-MR110PB
- Europe - CE

ATWILC1000-MR110UB

- United States/FCC ID: 2ADHKATWILC1000U

15.1 United States

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C "Intentional Radiators" single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification or Declaration of Conformity) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

15.1.1 Labeling and User Information Requirements

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have been labeled with their own FCC ID numbers. If the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording as follows:

For the ATWILC1000-MR110PB:

Contains Transmitter Module FCC ID: 2ADHKATWILC1000 **or**

Contains FCC ID: 2ADHKATWILC1000

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For the ATWILC1000-MR110UB:

Contains Transmitter Module FCC ID: 2ADHKATWILC1000U **or**

Contains FCC ID: 2ADHKATWILC1000U

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

A user's manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm

15.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

In the end product, the antenna(s) used with this transmitter must be installed to provide a separation distance of at least 6.5 cm from all persons and must not be co-located or operation in conjunction with any other antenna or transmitter. User and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying the RF exposure compliance.

15.1.3 Approved Antenna Types

To maintain modular approval in the United States, only the antenna types that have been tested shall be used. It is permissible to use a different antenna, provided the same antenna type and antenna gain (equal to or less than) is used. An antenna type comprises antennas having similar in-band and out-of-band radiation patterns.

Testing the ATWILC1000-MR110UB module was performed with the antenna types listed in Table 12-1.

15.1.4 Helpful Websites

Federal Communications Commission (FCC): http://www.fcc.gov

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB): https://apps.fcc.gov/oetcf/kdb/index.cfm

15.2 Canada

The ATWILC1000-MR110PB module has been certified for use in Canada under Innova- tion, Science and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specifi- cation (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

15.2.1 Labeling and User Information Requirements

Label Requirements (from RSP-100 Issue 11, Section 3): The host device shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the words "Contains", or similar wording expressing the same meaning, as follows:

For the ATWILC1000-MR110PB:

Contains IC: 20266-ATWILC1000

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

> **This device complies with Industry Canada license exempt RSS standard(s). Operation is subject to the following two conditions:**
>
> **(1) This device may not cause interference, and**
>
> **(2) This device must accept any interference, including interference that may cause undesired operation of the device.**
>
> **Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:**
>
> **(1) l'appareil ne doit pas produire de brouillage, et**
>
> **(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.**

Guidelines on Transmitter Antenna for License Exempt Radio Apparatus:

> **Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.**
>
> **Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour**

l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établisse-ment d'une communication satisfaisante.

15.2.2   RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure that the antenna has a separation distance of at least 6.5 cm from all persons or compliance must be demonstrated according to the ISED SAR procedures.

15.2.3   Canada_Helpful Websites

Innovation, Science and Economic Development Canada: http://www.ic.gc.ca/

15.3   Europe

The ATWILC1000-MR110PB module is Radio Equipment Directive (RED) assessed radio module that is CE marked and have been manufactured and tested with the intention of being integrated into a final product.

The ATWILC1000-MR110PB module has been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2), and are summarized in Table 15-1.

The ETSI provides guidance on modular devices in "*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/20 3367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the testing listed in Table 15-1, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified.

When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

15.3.1   Labeling and User Information Requirements

The label on the final product which contains the ATWILC1000-MR110PB module must follow CE marking requirements.

Table 15-1. European Compliance Testing - ATWILC1000-MR110PB

Certification	Standards	Article	Laboratory	Report Number	Date
Safety	EN60950-1:2006/A11:2009/ A1:2010/ A12:2011/A2:2013	[3.1(a)]	TUV Rheinland,	10061532 001	11 Aug 2017

Certification	Standards	Article	Laboratory	Report Number	Date
Health	EN300 328 v2.1.1 EN62311:2008		Taiwan	50092557 001	11 Aug 2017
EMC	EN 301 489-1 V2.1.1 EN 301 489-1 V2.2.0	[3.1(b)]		10060032 001	11 Aug 2017
	EN 301 489-17 V3.1.1 EN 301 489-17 V3.2.0				
Radio	EN300 328 v2.1.1	(3.2)		50092557 001	11 Aug 2017

15.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1 Non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in Table 15-1 was performed using the integral PCB antenna.

15.3.3 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATWILC1000-MR110PB is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following webpage: http://www.microchip.com/design-centers/wireless-connectivity

15.3.4 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/.

Additional helpful web sites are:
- Radio Equipment Directive (2014/53/EU): https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_en
- European Conference of Postal and Telecommunications Administrations (CEPT): http://www.cept.org
- European Telecommunications Standards Institute (ETSI): http://www.etsi.org
- The Radio Equipment Directive Compliance Association (REDCA): http://www.redca.eu/

16.   Reference Documentation

The following table provides the set of collateral documents to ease integration and device ramp.

Table 16-1. Reference documents

Title	Content
Wi-Fi Link Controller Linux user Guide	Getting started package, which includes: Quick start guide, Hardware limitations and notes, and software quick start guidelines.
Wi-Fi Link Controller Linux Porting Guide	This user guide describes how to port the ATWILC1000 and ATWILC3000 Linux drivers to another platform and contains all the required modifications for driver porting.

Note:

For a complete listing of development support tools and documentation, visit http://www.microchip.com/wwwproducts/en/ATWILC1000 or refer to the customer support section on options to the nearest Microchip field representative.

17. Document Revision History

Rev B - 10/2017

Section	Changes
MAC Features	Editorial updates

Rev A - 08/2017

Section	Changes
Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42503 revision C. • ISBN number added. • Updated module reference to ATWILC1000-MR110xB throughout the document. • Removed reference to Bluetooth coexistence • Added WFA certification details • Updated block diagram Figure 2-1 • Updated pin description in Table 3-1 • Updated VDDIO absolute maximum volatge rating in Table 4-1 and added caution footnote • Added operating temperature to Table 4-2 • Moved Transmitter Performance, Receiver Performance and Timing Characteristics under Electrical Specifications • Updated description in Nonvolatile Memory (eFuse) • Revised the Transmitter Performance and Receiver Performance • Updated Application Reference Design • Added Design Consideration • Updated Reference Documentation

Rev C - 11/2016

Section	Changes
Document	• Updated the device pinout drawing Figure 3-1 to make it easier to read • Added section 11.5 regarding PCBA coatings • Updated Marking diagram in Figure 1-1

Section	Changes
	• Revised values for Transmit Power and added notes in Table 4-4 • Added Pins and Agencies to Ordering Information in Table 1-1 • Added section ATWILC1000-MR110UB Placement and Routing Guidelines Types for ATWILC1000-MR110UB • Added Certification Notices • Added Regulatory Approval • Updated Description to indicate both the MR110PB and MR110UB are covered • Removed "With seamless roaming capabilities" from description • Revised features to only support SPI and SDIO hosts. • Removed references to WAPI • Removed UART • Moved Solder Pad drawing to be with POD drawings as in Figure 11-1 • Minor edits

Rev B - 5/2016

Section	Changes
Document	• Revised POD drawings in Module Outline Drawings • Revised Footprint drawing in Module Outline Drawings • Removed Module schematics and BOM's • Added Reflow profile Reflow Profile Information • Updated SDIO timing content in SDIO Slave Timing • Added footnotes to recommended operating ratings in Recommended Operating Conditions • Updated SPI timing content in SPI Slave Timing

Rev A - 8/2015

Section	Changes
Document	Updated due to changes from ATWILC100A(42380D) to ATWILC1000B:

Section	Changes
	• Updated power numbers and description, added high-power and low-power modes • Updated radio performance numbers • Fixed typos in SPI interface timing • Added hardware accelerators in feature list (security and checksum) • Increased instruction RAM size from 128KB to 160KB • Improved and corrected description of Coexistence interface • Miscellaneous minor updates and corrections

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