Document Number: A2T20H330W24N
Rev. 0, 9/2016

RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 55 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1880 to 2025 MHz.

1880–2025 MHz

- Typical Doherty single–carrier W–CDMA performance: V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.1 Vdc, P_{out} = 55 W Avg., input signal PAR = 9.9 dB @ 0.01% probability on CCDF.

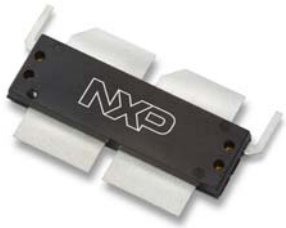
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1880 MHz	15.6	49.6	7.8	–31.2
1960 MHz	16.3	50.3	7.8	–32.1
2025 MHz	15.3	47.4	7.6	–33.1

Features

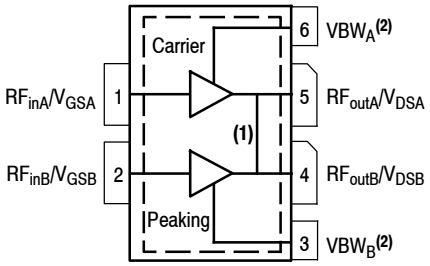
- Advanced high performance in–package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate–source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2T20H330W24NR6

1880–2025 MHz, 55 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



OM–1230–4L2L
PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 55 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.1 Vdc, f = 1960 MHz	$R_{\theta JC}$	0.26	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	0.8	1.2	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 700 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.3	2.6	3.1	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 180 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.8 Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

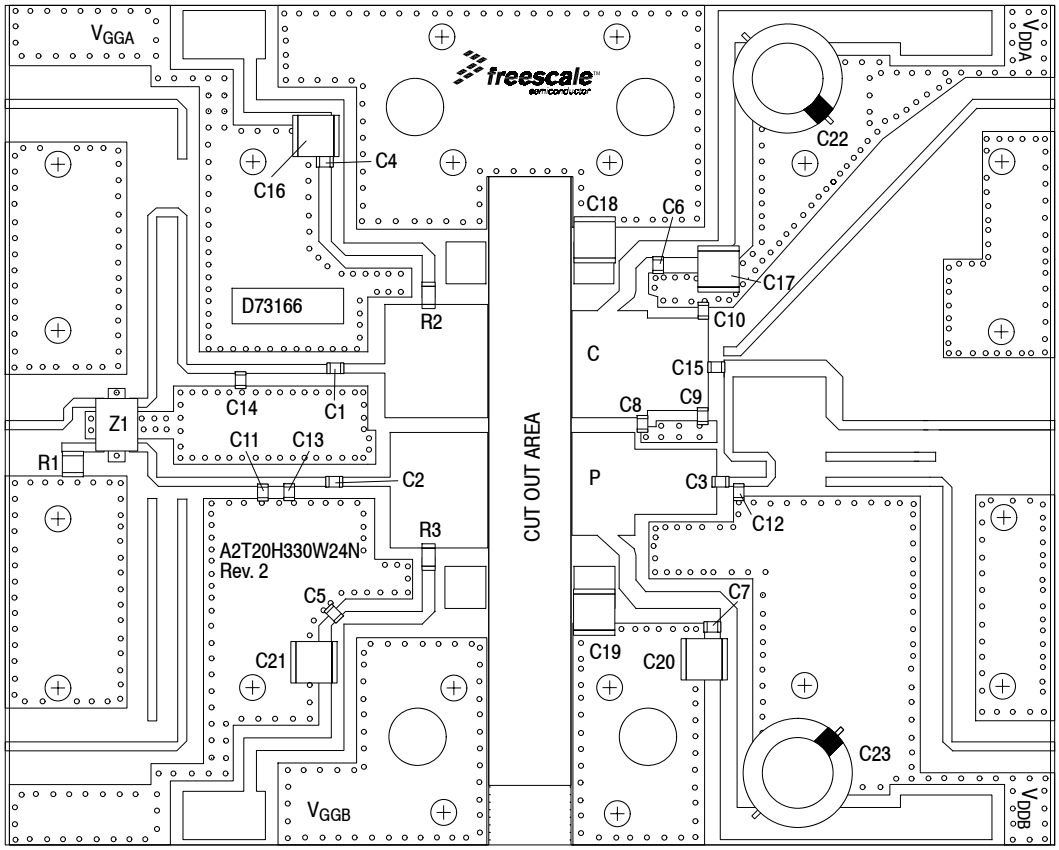
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2,3] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.1 Vdc, P_{out} = 55 W Avg., f = 1880 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.8	15.9	17.8	dB
Drain Efficiency	η_D	46.7	49.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.4	7.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	–32.8	–28.7	dBc
Load Mismatch [3] (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 700 mA, V_{GSB} = 0.1 Vdc, f = 1960 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 5:1 at 28 Vdc, 191 W Pulsed CW Output Power (0 dB Input Overdrive from 191 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance [3] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.1 Vdc, 1880–2025 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	229	—	W
P_{out} @ 3 dB Compression Point [4]	P3dB	—	383	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1880–2025 MHz bandwidth)	Φ	—	–13	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	130	—	MHz
Gain Flatness in 145 MHz Bandwidth @ P_{out} = 55 W Avg.	G_F	—	0.8	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.001	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T20H330W24NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L2L

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. A2T20H330W24NR6 Test Circuit Component Layout

Table 7. A2T20H330W24NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7	8.2 pF Chip Capacitors	ATC600F8R2JT250XT	ATC
C8, C9, C10, C11	0.3 pF Chip Capacitors	ATC600F0R3JT250XT	ATC
C12	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C13	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
C14	1.1 pF Chip Capacitor	ATC600F1R1BT250XT	ATC
C15	7.5 pF Chip Capacitor	ATC600F7R5BT250XT	ATC
C16, C17, C18, C19, C20, C21	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C22, C23	220 μF, 50 V Electrolytic Capacitors	227CKS050M	Illinois Capacitor
R1	50 Ω, 10 W Chip Resistor	C10A50Z4	Anaren
R2, R3	2.7 Ω, 1/4 W Chip Resistors	CRCW12062R70FKEA	Vishay
Z1	1800–2200 MHz Band, 90°, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D73166	MTL

TYPICAL CHARACTERISTICS — 1880–2025 MHz

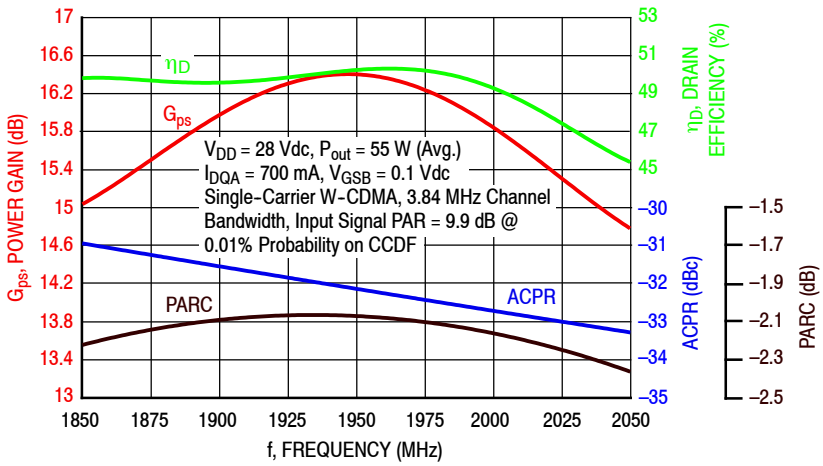


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 55 Watts Avg.

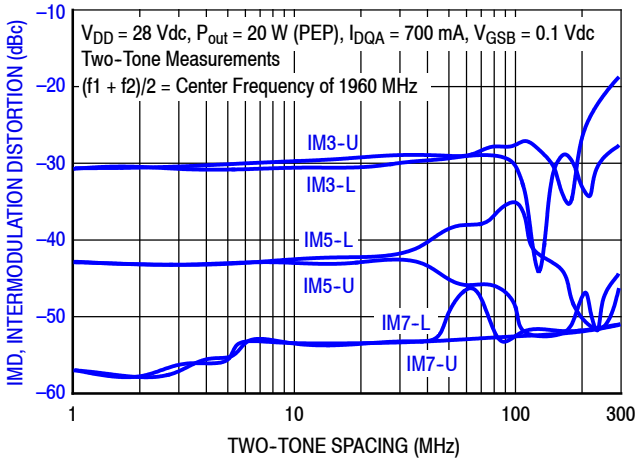


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

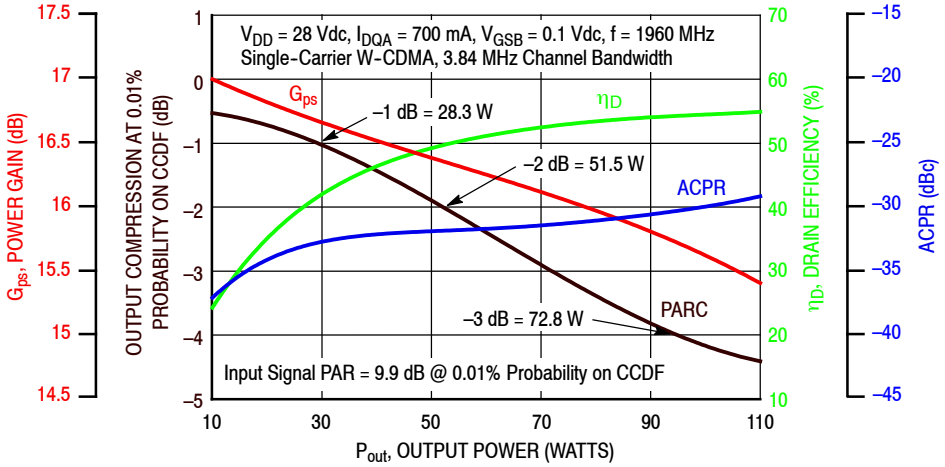


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1880–2025 MHz

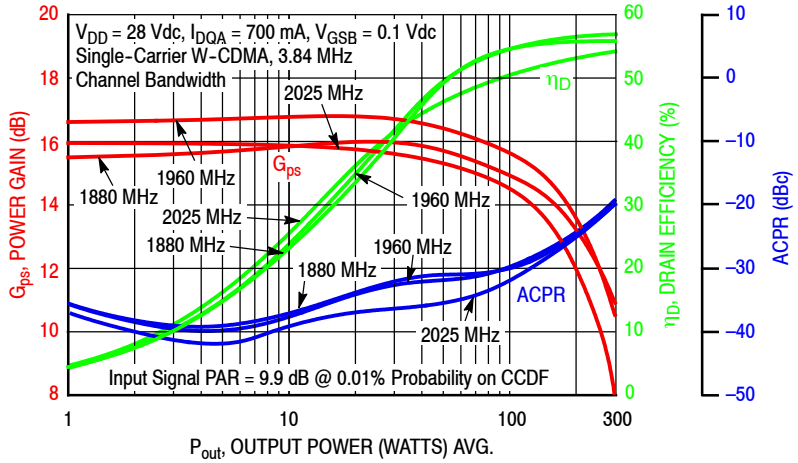


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

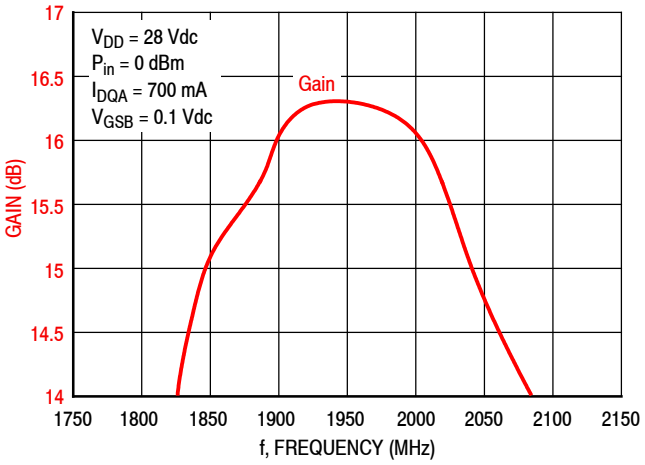


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 697 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	0.90 – j3.49	1.03 + j3.46	1.10 – j2.83	19.6	51.9	155	56.9	–15
1960	2.03 – j4.74	1.94 + j4.58	1.13 – j2.91	19.5	51.9	156	56.8	–15
2025	4.03 – j6.34	4.09 + j5.83	1.14 – j2.94	19.5	51.8	152	55.2	–15

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	0.90 – j3.49	0.95 + j3.53	1.06 – j2.94	17.3	52.7	186	58.1	–19
1960	2.03 – j4.74	1.85 + j4.74	1.13 – j3.04	17.2	52.7	185	58.1	–18
2025	4.03 – j6.34	4.10 + j6.23	1.15 – j3.06	17.2	52.6	181	56.7	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 697 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	0.90 – j3.49	1.15 + j3.85	3.07 – j1.83	23.0	49.0	79	68.3	–17
1960	2.03 – j4.74	2.50 + j4.99	2.76 – j1.68	22.6	49.0	80	67.7	–17
2025	4.03 – j6.34	5.09 + j6.21	1.91 – j1.94	22.2	50.1	102	65.0	–18

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	0.90 – j3.49	1.20 + j3.90	3.07 – j1.83	21.0	49.9	97	71.4	–25
1960	2.03 – j4.74	2.55 + j5.10	2.76 – j1.68	20.6	49.9	99	69.9	–24
2025	4.03 – j6.34	6.23 + j6.35	2.04 – j1.25	21.2	49.5	89	67.6	–27

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

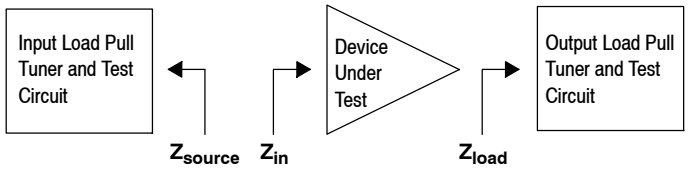


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.16 – j3.95	0.87 + j4.11	1.55 – j2.98	14.7	53.4	217	55.2	–32
1960	2.19 – j5.24	1.69 + j5.51	1.64 – j2.91	14.7	53.5	223	57.5	–31
2025	4.51 – j6.98	3.76 + j7.58	1.58 – j2.84	14.7	53.4	221	56.2	–32

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.16 – j3.95	0.87 + j4.26	1.61 – j3.06	12.7	54.1	258	57.9	–38
1960	2.19 – j5.24	1.80 + j5.80	1.67 – j3.08	12.6	54.2	263	58.5	–38
2025	4.51 – j6.98	4.29 + j8.08	1.66 – j3.03	12.6	54.1	258	57.1	–39

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

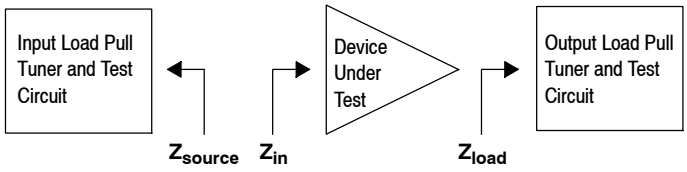
Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 1.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.16 – j3.95	0.81 + j4.10	3.98 – j2.80	15.5	51.9	154	66.6	–37
1960	2.19 – j5.24	1.52 + j5.46	3.44 – j1.48	15.5	51.8	150	67.4	–37
2025	4.51 – j6.98	3.36 + j7.55	2.72 – j1.22	15.5	51.8	150	66.5	–38

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.16 – j3.95	0.84 + j4.26	3.68 – j3.07	13.5	52.7	186	66.1	–44
1960	2.19 – j5.24	1.69 + j5.79	3.33 – j2.09	13.4	52.8	191	66.7	–44
2025	4.51 – j6.98	4.01 + j8.11	2.83 – j1.67	13.5	52.7	188	65.9	–46

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1960 MHz

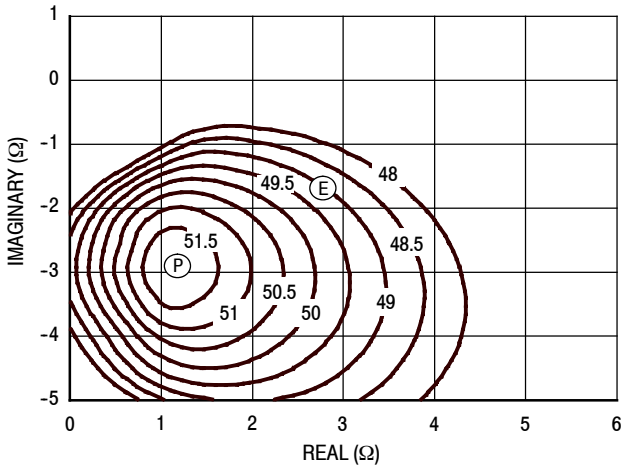


Figure 8. P1dB Load Pull Output Power Contours (dBm)

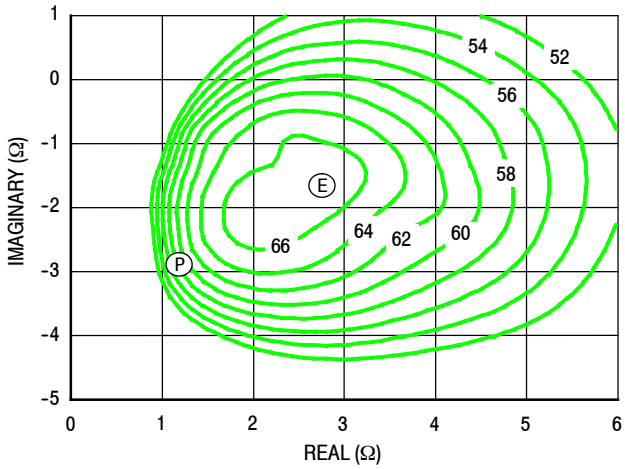


Figure 9. P1dB Load Pull Efficiency Contours (%)

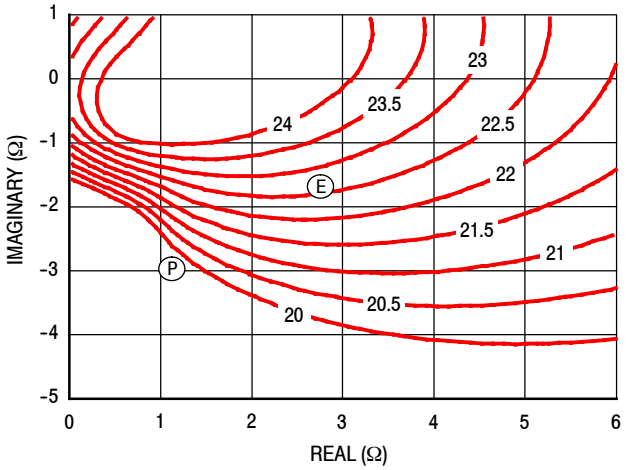


Figure 10. P1dB Load Pull Gain Contours (dB)

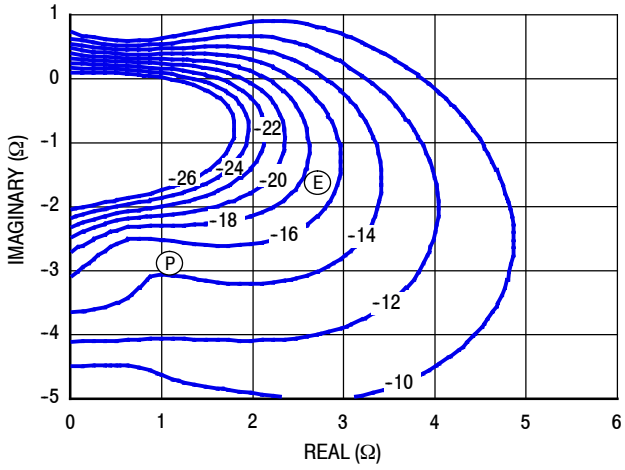


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1960 MHz

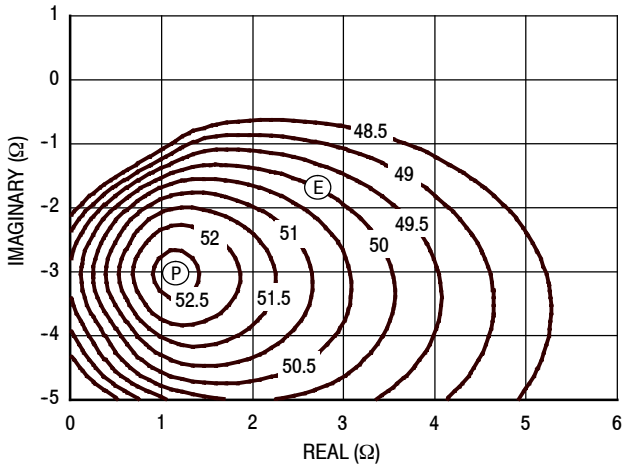


Figure 12. P3dB Load Pull Output Power Contours (dBm)

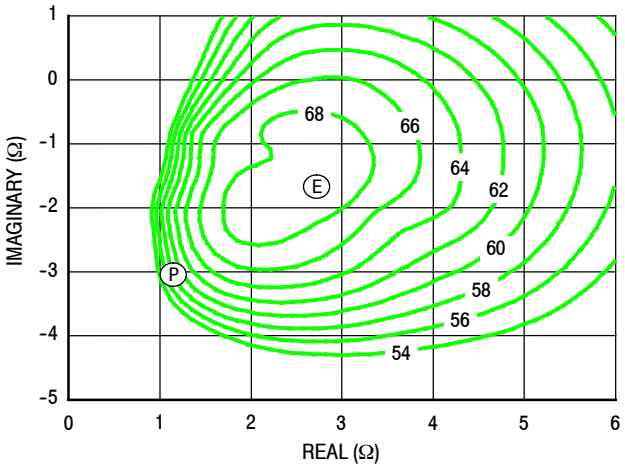


Figure 13. P3dB Load Pull Efficiency Contours (%)

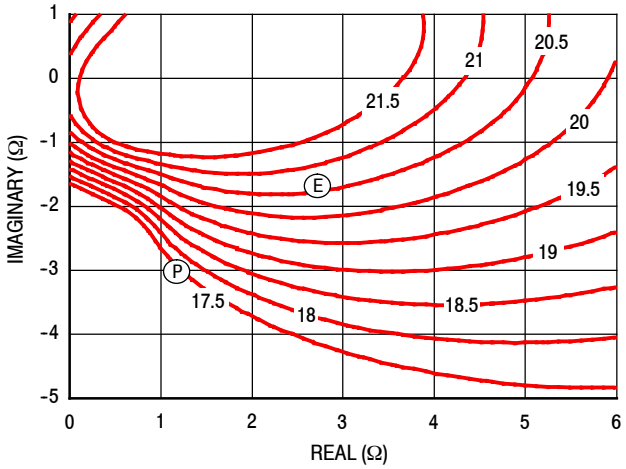


Figure 14. P3dB Load Pull Gain Contours (dB)

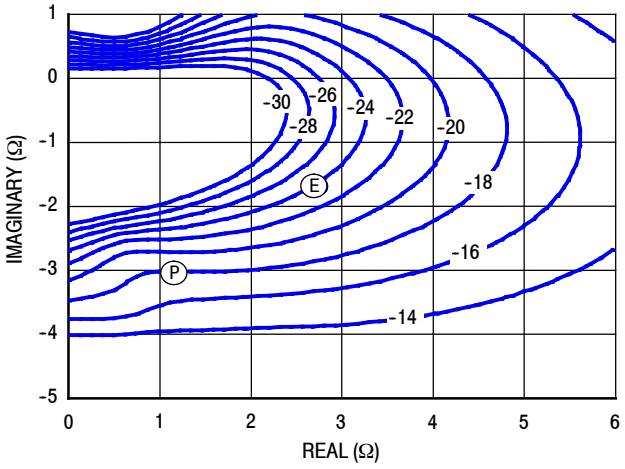


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1960 MHz

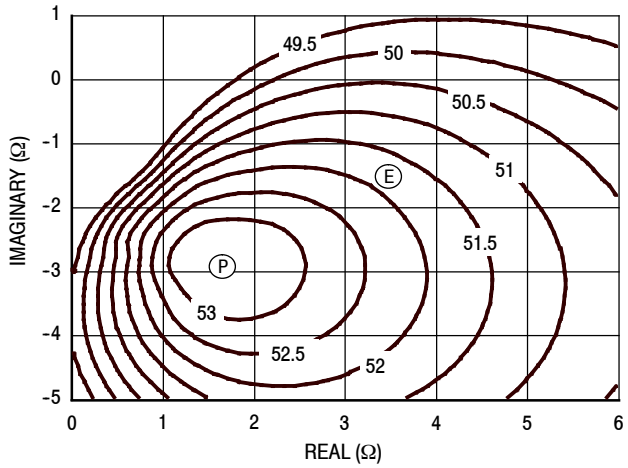


Figure 16. P1dB Load Pull Output Power Contours (dBm)

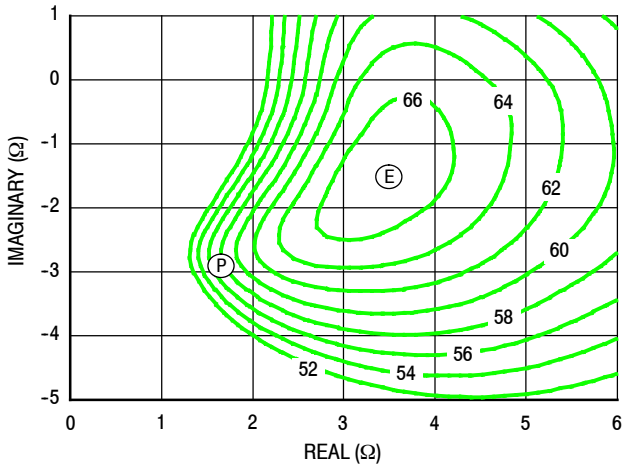


Figure 17. P1dB Load Pull Efficiency Contours (%)

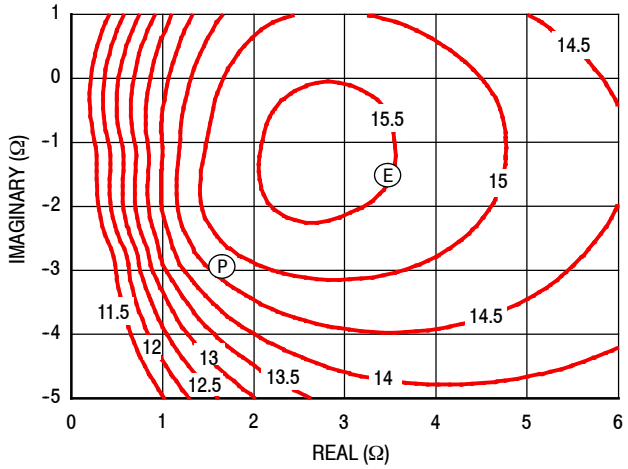


Figure 18. P1dB Load Pull Gain Contours (dB)

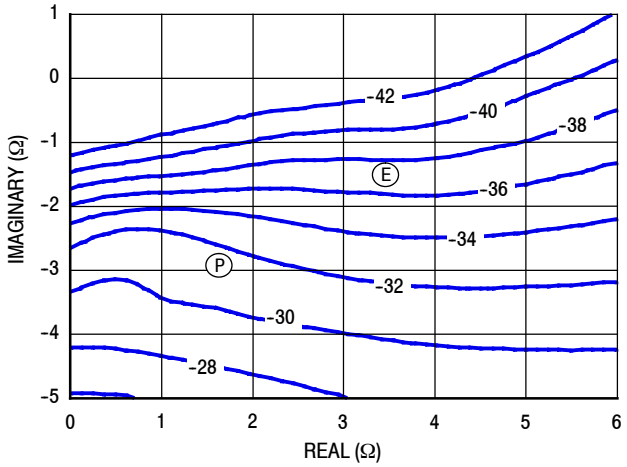


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1960 MHz

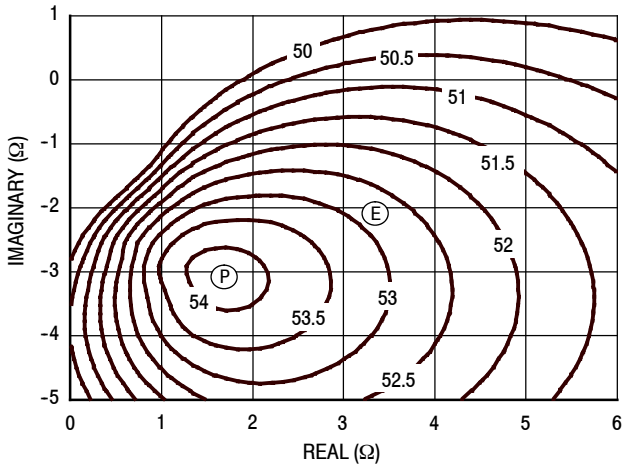


Figure 20. P3dB Load Pull Output Power Contours (dBm)

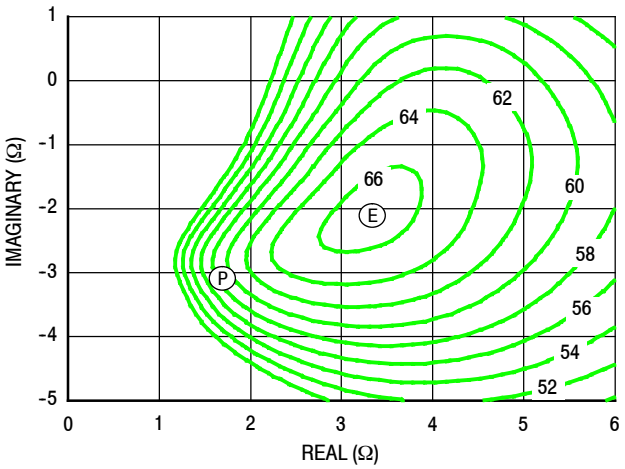


Figure 21. P3dB Load Pull Efficiency Contours (%)

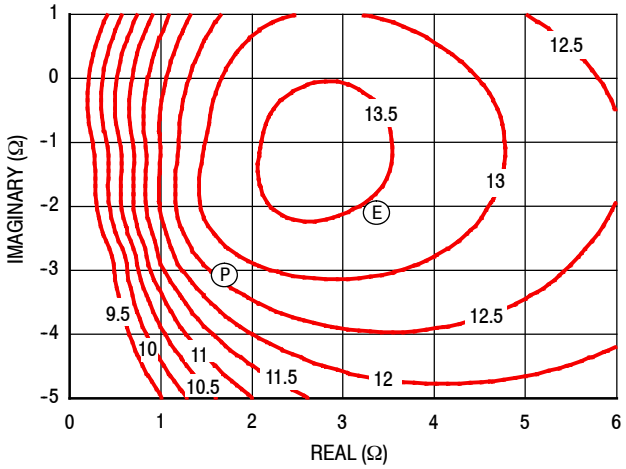


Figure 22. P3dB Load Pull Gain Contours (dB)

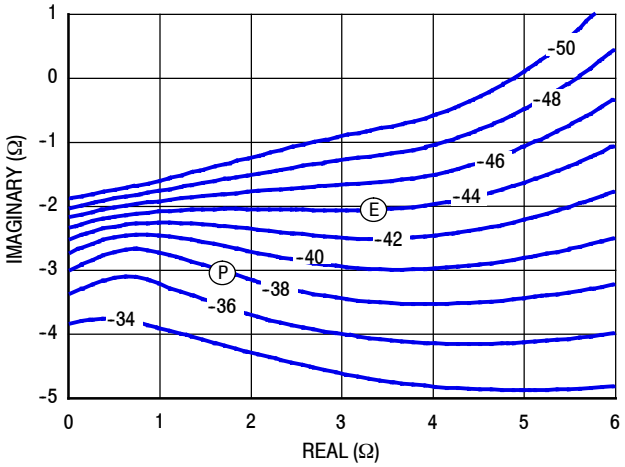


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

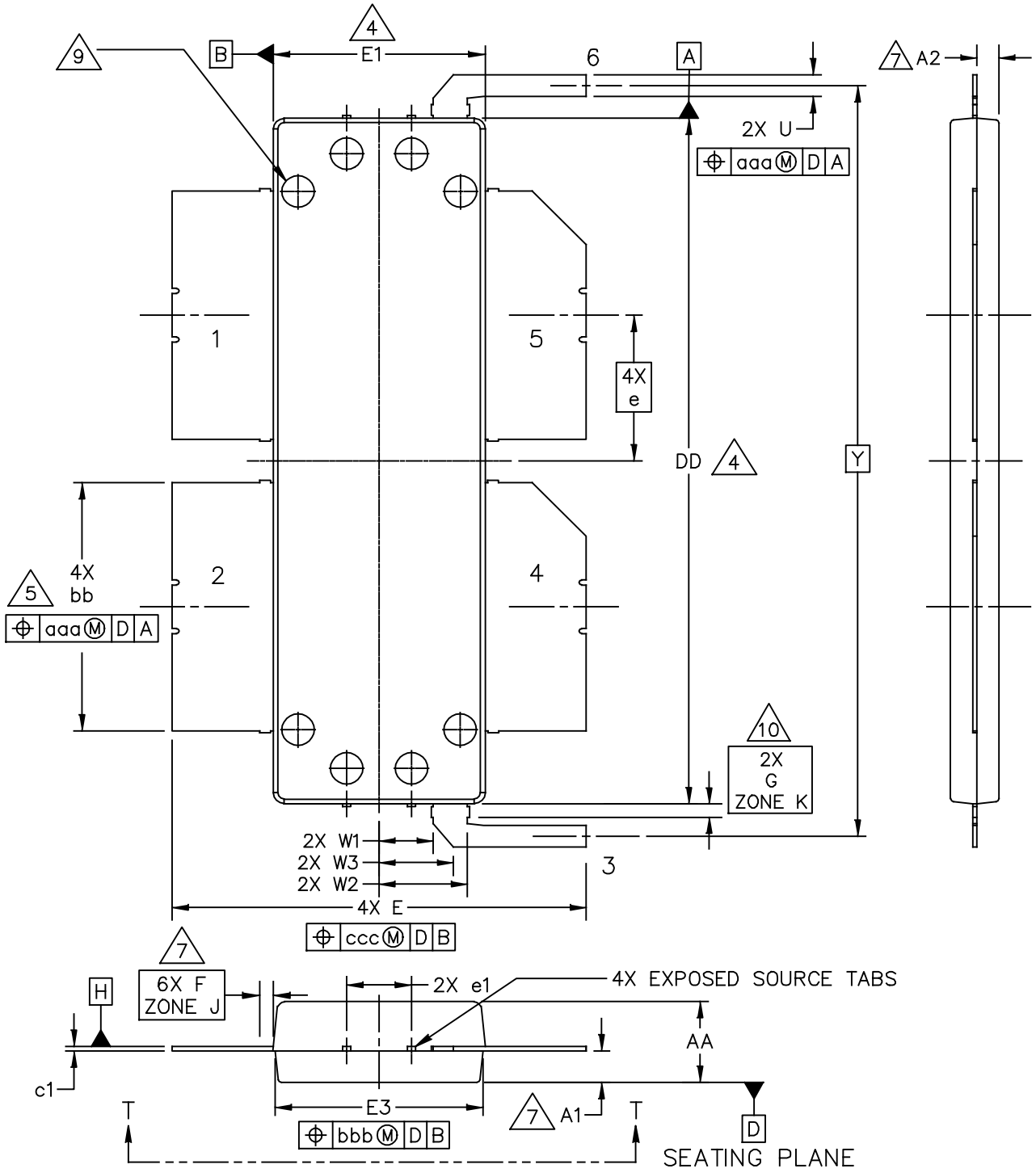
Gain

Drain Efficiency

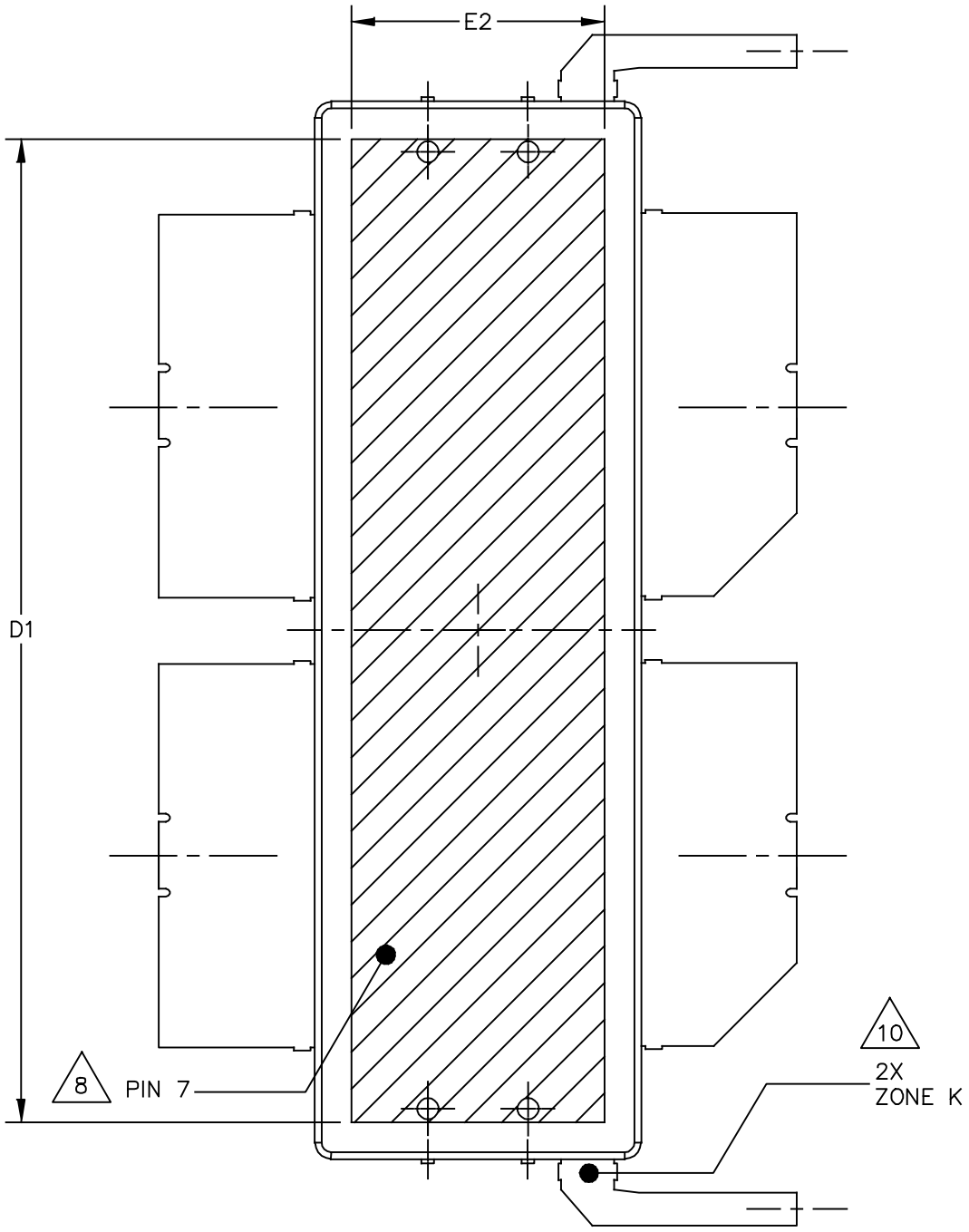
Linearity

Output Power

PACKAGE DIMENSIONS



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM−1230−4L2L	DOCUMENT NO: 98ASA00787D	REV: A
	STANDARD: NON−JEDEC	
	SOT1819−1	17 FEB 2016



BOTTOM VIEW
VIEW T–T

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM–1230–4L2L	DOCUMENT NO: 98ASA00787D	REV: A
	STANDARD: NON–JEDEC	
	SOT1819–1	17 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS A1 AND A2 APPLY WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1, 2, 4 AND 5. A2 APPLIES TO PINS 3 AND 6.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. ZONE K REPRESENTS NON–SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	0.148	.152	3.76	3.86	W1	.095	.105	2.41	2.67
A1	.059	.065	1.50	1.65	W2	.158	.168	4.01	4.27
A2	.056	.068	1.42	1.73	W3	.132	.142	3.35	3.61
DD	1.267	1.273	32.18	32.33	U	.037	.043	0.94	1.09
D1	1.180	----	29.97	----	Y	1.390 BSC		35.31 BSC	
E	.762	.770	19.35	19.56	bb	.457	.463	11.61	11.76
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.270 BSC		6.86 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
					ccc	.010		0.25	

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA00787D	REV: A
OM–1230–4L2L	STANDARD: NON–JEDEC	
	SOT1819–1	17 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2016	• Initial release of data sheet

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number: A2T20H330W24N
Rev. 0, 9/2016