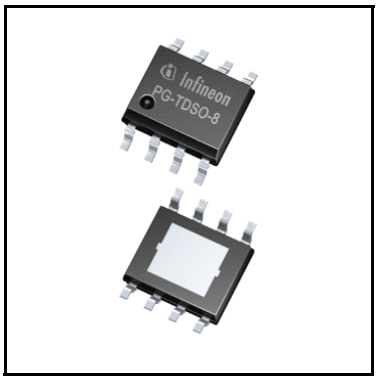
HITFET - BTS3080EJ

Smart Low-Side Power Switch



1 Overview

Basic Features

- Single channel device
- Very low output leakage current in OFF state
- Electrostatic discharge protection (ESD)
- Embedded protection functions (see below)
- ELV compliant package
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits

Description

The BTS3080EJ is a 80 mΩ single channel Smart Low-Side Power Switch with in a PG-TDSO8-31 package providing embedded protective functions. The power transistor is built by an N-channel vertical power MOSFET.
The device is monolithically integrated. The BTS3080EJ is automotive qualified and is optimized for 12 V automotive applications.

Type	Package	Marking
BTS3080EJ	PG-TDSO8-31	S3080EJ

Table 1 Product Summary

Operating voltage range	V_{OUT}	0 .. 31 V
Maximum load voltage	$V_{BAT(LD)}$	40 V
Maximum input voltage	V_{IN}	5.5 V
Maximum On-State resistance at T_J = 150°C,V_{IN} = 5 V	$R_{DS(ON)}$	160 mΩ
Nominal load current	$I_{L(NOM)}$	3 A
Minimum current limitation	$I_{L(LIM)}$	10 A
Maximum OFF state load current at $T_J \leq$ 85°C	$I_{L(OFF)}$	2 µA

Overview

Diagnostic Functions

- open-drain status output

Protection Functions

- Over temperature shut-down with automatic-restart
- Active clamp over voltage protection
- Current limitation

Detailed Description

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by maximum clamping energy and maximum current capabilities.

The BTS3080EJ offers ESD protection on the IN pin which refers to the Source pin (Ground).

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions. The temperature information is given by a temperature sensor in the power MOSFET.

The BTS3080EJ has an auto-restart thermal shut-down function. The device will turn on again, if input is still high, after the measured temperature has dropped below the thermal hysteresis.

The over voltage protection can be activated during load dump or inductive turn off conditions. The power MOSFET is limiting the drain-source voltage, if it rises above the $V_{OUT(CLAMP)}$.

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2 Block Diagram

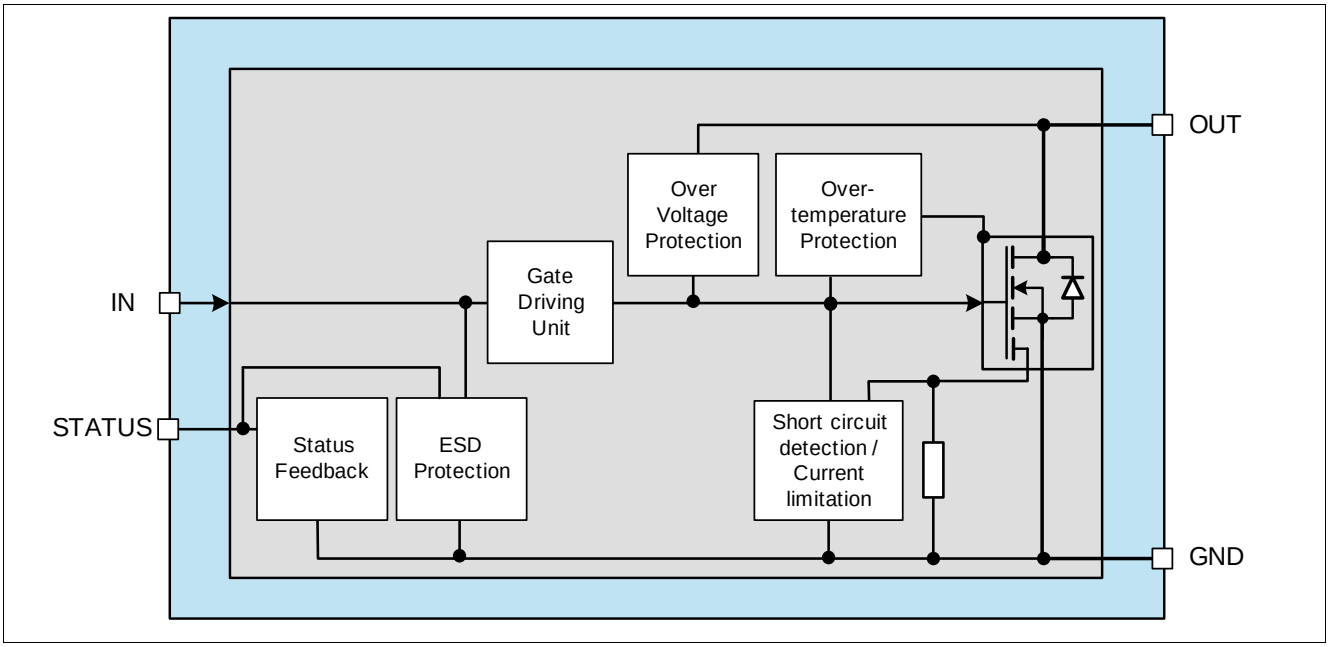

Figure 1 Block Diagram

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance PG-TDSO8-31

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	4.1	–	K/W	1) 2)	P_4.3.5
Junction to Ambient (2s2p)	$R_{thJA(2s2p)}$	–	37	–	K/W	1) 3)	P_4.3.11
Junction to Ambient (1s0p+600 mm^2 Cu)	$R_{thJA(1s0p)}$	–	48	–	K/W	1) 4)	P_4.3.17
Junction to Ambient (1s0p+300 mm^2 Cu)	$R_{thJA(1s0p)}$	–	58	–	K/W	1) 5)	P_4.3.23

1) Not subject to production test, specified by design

2) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).
T_A = 85°C. Device is loaded with 1 W power.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board;
The product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer.
T_A = 85°C, Device is loaded with 1 W power.

4) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board;
The product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600 mm^2 and 70 µm thickness. T_A = 85°C, Device is loaded with 1 W power.

5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board;
The product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 300 mm^2 and 70 µm thickness. T_A = 85°C, Device is loaded with 1 W power.

4.3.1 PCB set up

The following PCB set up was implemented to determine the transient thermal impedance[1)]

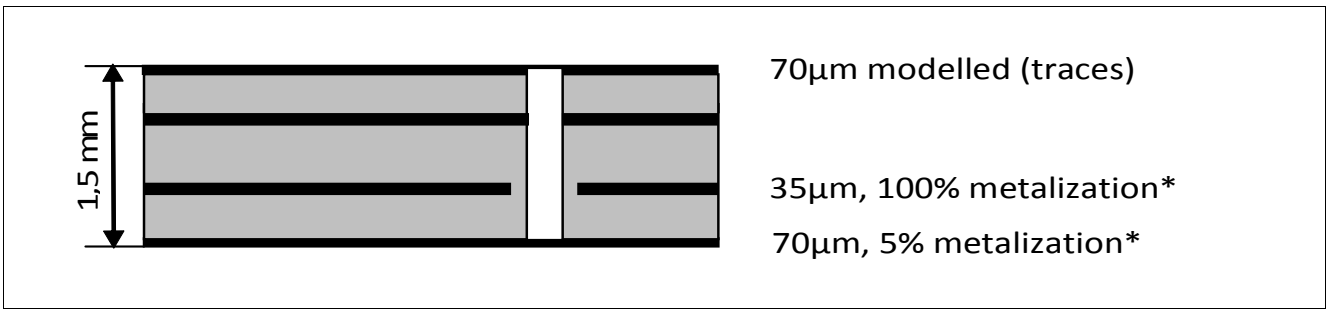

Figure 4 Cross section JEDEC2s2p

1) (*) means percentual Cu metalization on each layer

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Output voltage	V_{OUT}	–	–	40	V	internally clamped	P_4.1.1
Battery voltage for short circuit protection	$V_{BAT(SC)}$	–	–	31	V	I = 0 or 5 m R_{SC} = 20 mΩ + R_{Cable} R_{Cable} = l * 16 mΩ/m L_{SC} = 5 µH + L_{Cable} L_{Cable} = l * 1 µH/m V_{IN} = 5 V	P_4.1.2
Battery voltage for load dump protection	$V_{BAT(LD)}$	–	–	40	V	[2)] R_I = 2 Ω R_L = 4.5 Ω t_D = 400 ms suppressed pulse	P_4.1.4
Input Pin							
Input Voltage	V_{IN}	-0.3	–	5.5	V	–	P_4.1.7
Input current in inverse condition on OUT to GND)	I_{IN}	–	–	2	mA	[3)] V_{OUT} < -0.3 V	P_4.1.10
Status Pin							
Status Voltage	V_{STATUS}	-0.3	–	5.5	V	–	P_4.1.11
Status current	I_{STATUS}	–	–	5	mA	-0.3 V < V_{STATUS} < 5.5 V	P_4.1.12
Status current in inverse current condition on STATUS	I_{STATUS_L}	-1	–	–	mA	V_{STATUS} < -0.3 V	P_4.1.13
Power Stage							
Load current	$\lvert I_L \rvert$	–	–	$I_{L(LIM)}$	A	–	P_4.1.14
Energies							
Unclamped single inductive energy single pulse	E_{AS}	–	–	35	mJ	$I_{L(0)}$ = $I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 150°C	P_4.1.20
Unclamped repetitive inductive energy pulse with 10k	$E_{AR(10k)}$	–	–	38	mJ	$I_{L(0)}$ = $I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 105°C	P_4.1.32

Table 2 Absolute Maximum Ratings [1)] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Unclamped repetitive inductive energy pulse with 100k cycles	$E_{AR(100k)}$	–	–	30	mJ	$I_{L(0)} = I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 105 °C	P_4.1.38
Unclamped repetitive inductive energy pulse with 1M	$E_{AR(1M)}$	–	–	24	mJ	$I_{L(0)} = I_{L(NOM)}$ V_{BAT} = 13.5 V $T_{J(0)}$ = 105 °C	P_4.1.44
Temperatures							
Operating temperature	T_J	-40	–	+150	°C	–	P_4.1.52
Storage temperature	T_{STG}	-55	–	+150	°C	–	P_4.1.53
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-3	–	3	kV	HBM[4)]	P_4.1.54
ESD susceptibility OUT-pin to GND	V_{ESD}	-10	–	10	kV	HBM[5)]	P_4.1.55
ESD susceptibility	V_{ESD}	-1	–	1	kV	CDM[6)]	P_4.1.56
ESD susceptibility non-corner pins	V_{ESD}	-1	–	1	kV	CDM[7)]	P_4.1.57

1) Not subject to production test, specified by design.

2) $V_{BAT(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1;
R_i is the internal resistance of the load dump test pulse generator;
t_D is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.

3) Maximum allowed value. Consider also inverse input current in inverse condition $I_{IN(-VOUT)}$ in Chapter 9

4) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

5) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

6) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

7) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance PG-TDSO8-31

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Junction to Ambient (2s2p)	$R_{thJA(2s2p)}$	–	37	–	K/W	1) 3)	P_4.3.11
Junction to Ambient (1s0p+600 mm^2 Cu)	$R_{thJA(1s0p)}$	–	48	–	K/W	1) 4)	P_4.3.17
Junction to Ambient (1s0p+300 mm^2 Cu)	$R_{thJA(1s0p)}$	–	58	–	K/W	1) 5)	P_4.3.23

1) Not subject to production test, specified by design

2) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).
T_A = 85°C. Device is loaded with 1 W power.

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board;
The product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the ex posed pad contacted the first inner copper layer.
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5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board;
The product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 300 mm^2 and 70 µm thickness. T_A = 85°C, Device is loaded with 1 W power.

4.3.1 PCB set up

The following PCB set up was implemented to determine the transient thermal impedance[1)]

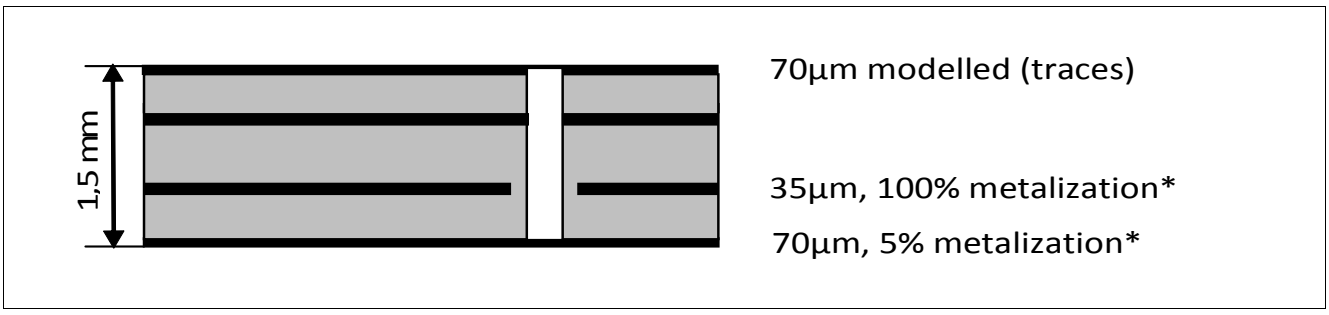


Figure 4 Cross section JEDEC2s2p

1) (*) means percentual Cu metalization on each layer

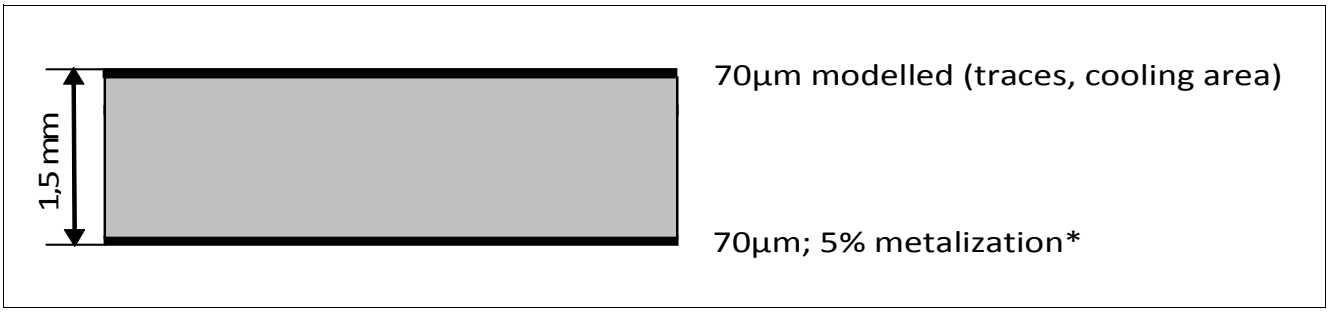


Figure 5 Cross section JEDEC1s0p

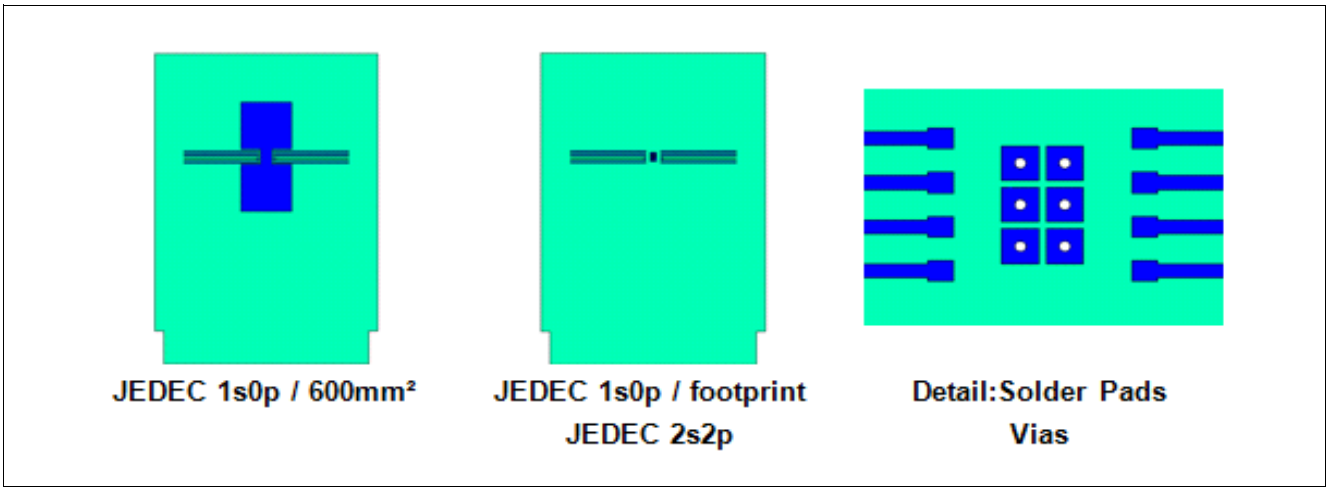


Figure 6 PCB layout

4.3.2 Transient Thermal Impedance

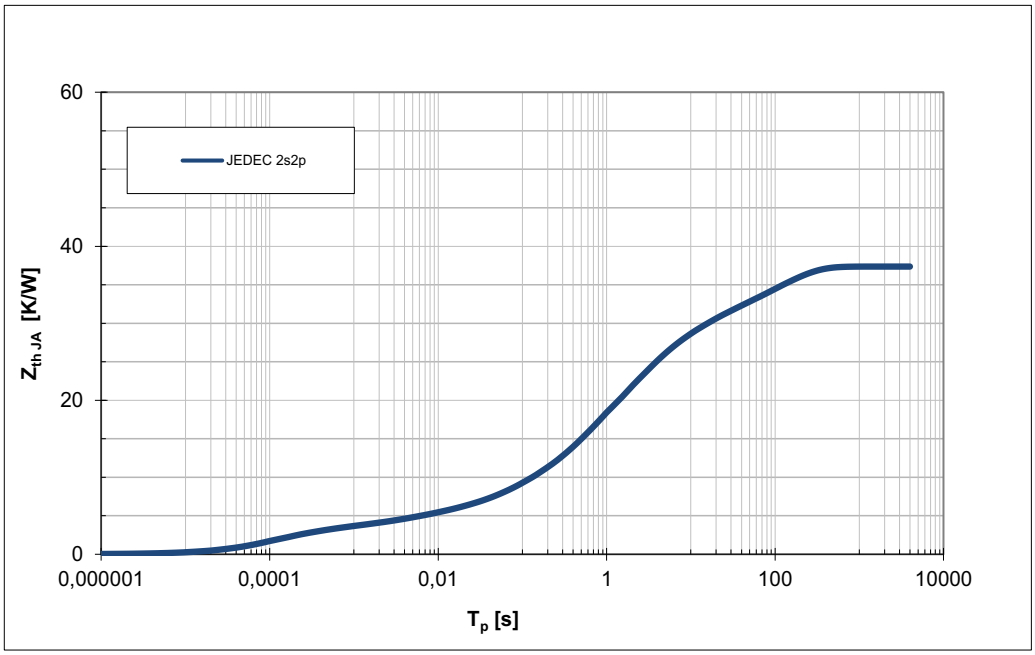


Figure 7 Typical transient thermal impedance $Z_{thJA} = f(t_p)$, $T_A = 85°C$
Value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Device is dissipating 1 W power.

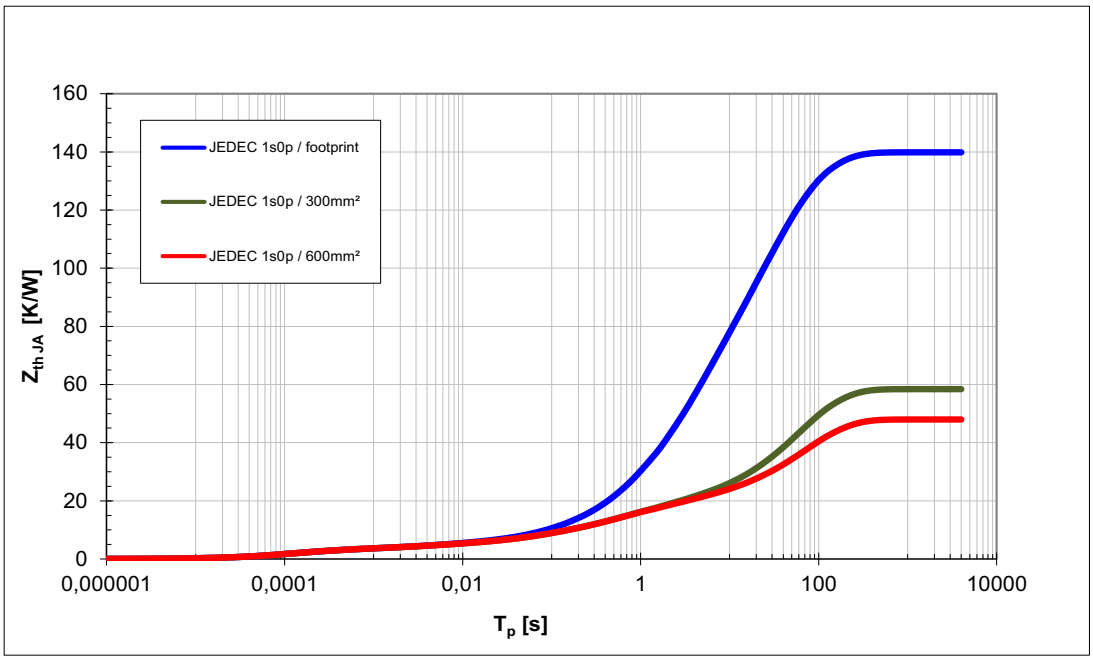


Figure 8 Typical transient thermal impedance $Z_{thJA} = f(t_p)$, Ta = 85°C
Value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. Device is dissipating 1 W power.

5 Power Stage

5.1 Output On-state Resistance

The on-state resistance depends on the junction temperature T_J. The Figure below show this dependencies in terms of temperature and voltage for the typical on-state resistance $R_{DS(ON)}$. The behavior in reverse polarity is described in**"Reverse Current capability" on Page 16**

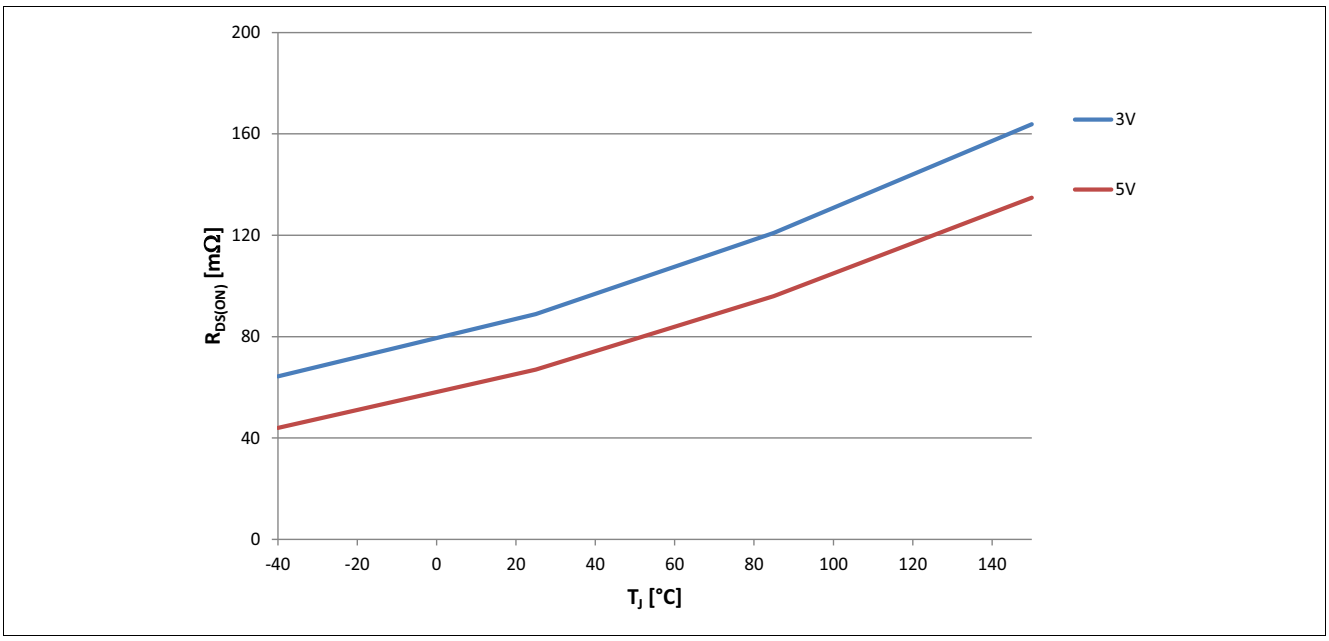


Figure 9 Typical On-State Resistance, $R_{DS(ON)} = f(T_J)$, $V_{IN} = 3$ V; $V_{IN} = 5$ V

5.2 Resistive Load Output Timing

Figure 10 shows the typical timing when switching a resistive load.

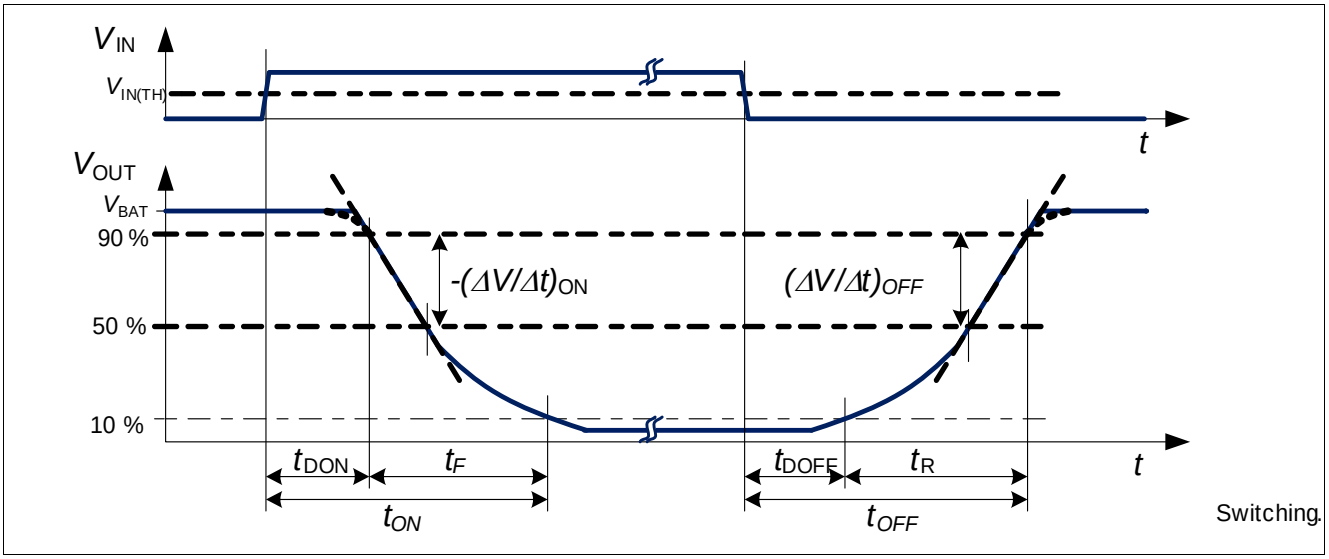


Figure 10 Definition of Power Output Timing for Resistive Load

5.3 Inductive Load

5.3.1 Output Clamping

When switching off inductive loads with low side switches, the Drain-Source voltage V_{OUT} rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at $V_{OUT(CLAMP)}$. During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See **Figure 11** and **Figure 12** for more details.

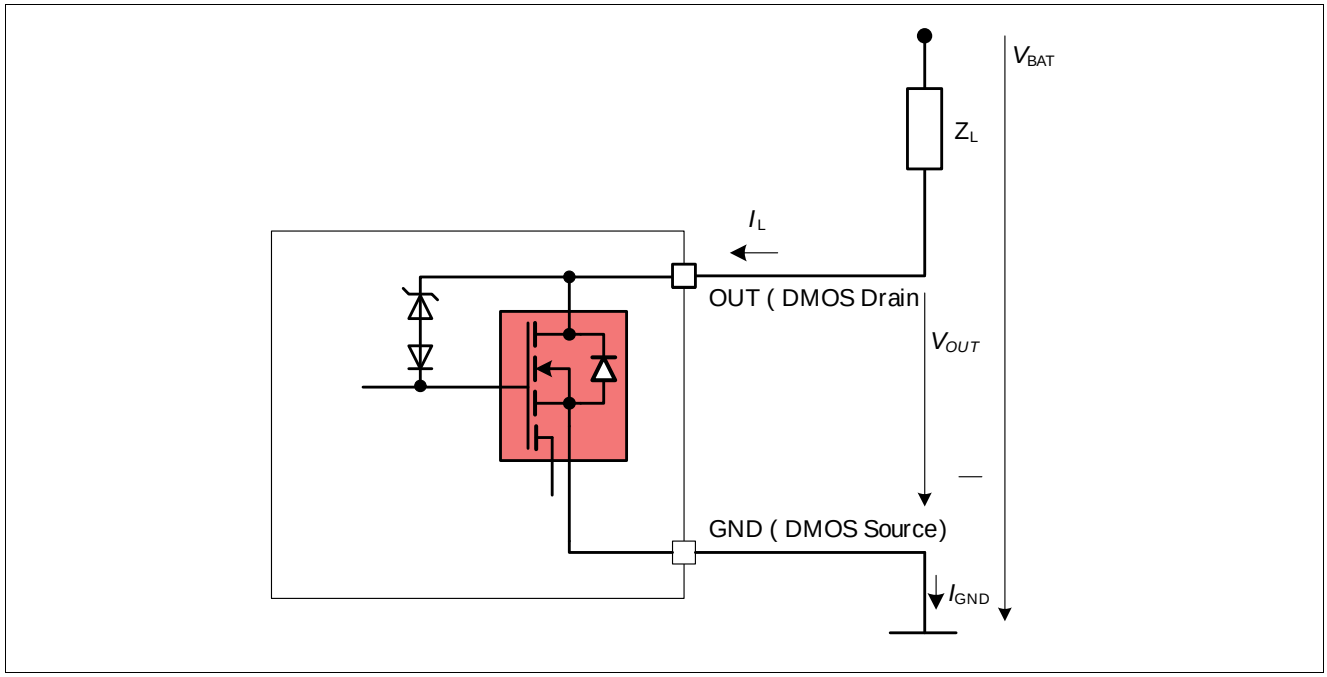


Figure 11 Output Clamp Circuitry

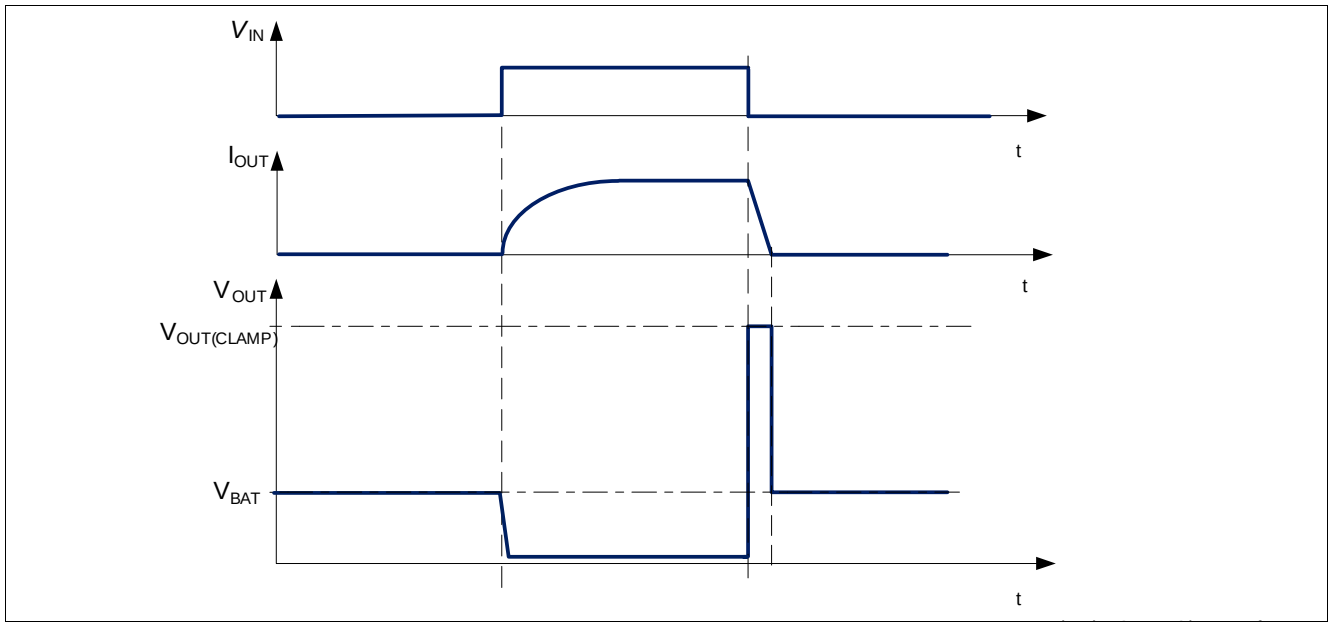


Figure 12 Switching an Inductive Load

5.3.1.1 Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS3080EJ.
This energy can be calculated by the following equation:

$$E = V_{OUT(CLAMP)} \times \left[\frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_{BAT} - V_{OUT(CLAMP)}}\right) + I_L \right] \times \frac{L}{R_L} \quad (5.1)$$

Following equation simplifies under assumption of $R_L = 0$

$$E = \frac{1}{2} L I_L^{\,2} \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}}\right) \quad (5.2)$$

For maximum single avalanche energy please also refer to EAS value in **“Energies” on Page 8**

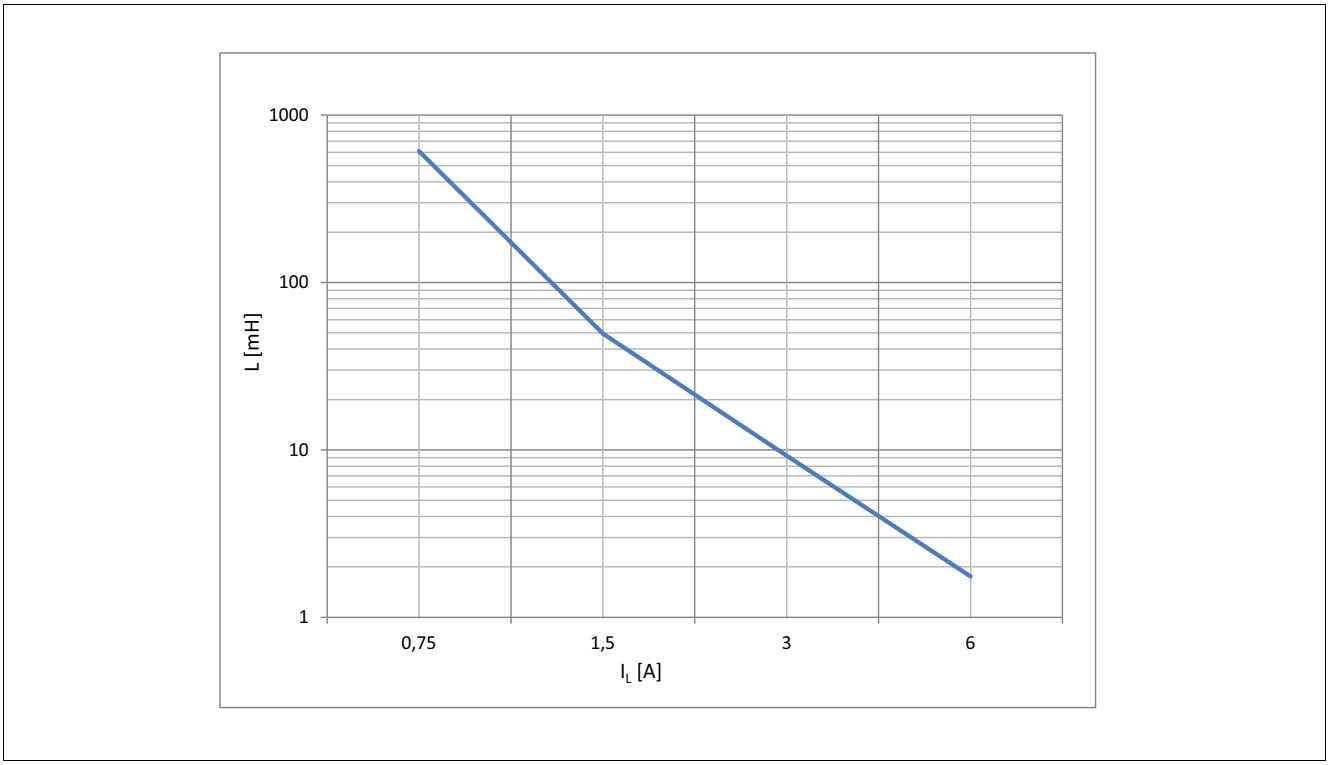


Figure 13 Maximum load inductance for single pulse
$L = f(I_L)$, $T_{J(0)} = T_{J,\,start} = 150°C$, $V_{BAT} = 13.5\ V$

5.4 Reverse Current capability

A reverse battery situation means the OUT pin is pulled below GND potentials to $-V_{BAT}$ via the load Z_L.

In this situation the load is driven by a current through the intrinsic body diode of the BTS3080EJ. During Reverse Battery all protection functions like current limitation, over temperature shut down and over voltage clamping are not available.

The device is dissipating a power loss which is defined by the driven current and the voltage drop on the DMOS reverse body diode "-V_{OUT}".

5.5 Inverse Current capability

An inverse current situation means the OUT pin is pulled below GND potential by a current flowing from GND to OUT (for example in half-bridge configuration and inductive load using freewheeling via the low side path).

In this situation the load is driven by a current through the intrinsic body diode (device off) of the BTS3080EJ. During Inverse operation all protection functions like current limitation, over temperature shut down and over voltage clamping are not available.

The device is dissipating a power loss which is defined by the driven current and the voltage drop on the DMOS reverse body diode "-V_{OUT}".

Input current behavior during inverse condition on Output

Please note that during inverse current on drain an increased input current can flow ($I_{IN(-VOUT)}$). To limit this current it is needed to place a resistor (R_{IN}) in line with the input, also to prevent the microcontroller I/O pins from latching up in this case. The value of this resistor is a compromise of input voltage level in normal operation and maximum allowed device input current I_{IN} or I/O current (for example of microcontroller).

$$R_{IN\,(\min)} = \frac{V_{OHuC\ (\max)}}{I_{IN\,(\max)}} \tag{5.3}$$

with $I_{IN(max)}$ = 2 mA (see also **"Absolute Maximum Ratings" on Page 8**) allow for the device;
$V_{OH\mu C(max)}$ maximum high level voltage of the control signal (microcontroller I/O)
and assuming -V_{OUT} = 1.1 V (worst case) in inverse condition on the output

If inverse current occurs while the STATUS is active (LOW), the STATUS will be reset (HIGH) after the inverse current disappears.

5.6 Characteristics

Please see **"Power Stage" on Page 14** for electrical characteristic table.

6 Protection Functions

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operation. Protection functions are not designed for continuous repetitive operation.

6.1 Over Voltage Clamping on OUTput

The BTS3080EJ is equipped with a voltage clamp circuitry that keeps the drain-source (output to GND) voltage V_{DS} at a certain level $V_{OUT(CLAMP)}$. The over voltage clamping is overruling the other protection functions. Power dissipation has to be limited to not exceed the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. Please see also **Chapter 5.3.1** for more details.

6.2 Thermal Protection

The device is protected against over temperature due to overload and / or bad cooling conditions. To ensure this a temperature sensor is located in the power MOSFET.

The BTS3080EJ has a thermal protection function with automatic restart. After the device has switched off due to over temperature the device will stay off until the junction temperature has dropped down below the thermal hysteresis **“Thermal Protection” on Page 18**.

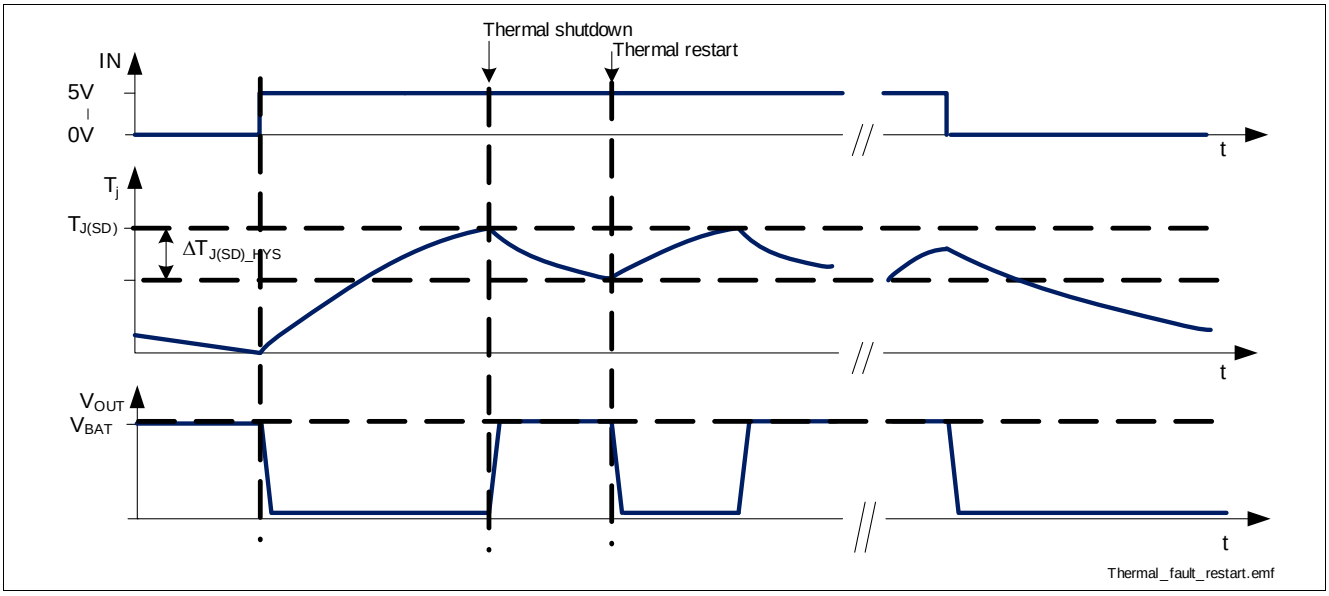


Figure 14 Thermal protective switch OFF scenario with thermal restart

The device also features a digital feedback on the dedicated status pin. This feedback is latched and can be read out easily by the microcontroller. Please see **“Diagnostics” on Page 21** for details on this feedback.

6.3 Short Circuit Protection / Current limitation

The condition short circuit is an overload condition to the device. If the load current reaches the limitation value of $I_{L(LIM)}$ the device limits the current and therefore will start heating up. When the thermal shutdown temperature is reached, the device turns off.

The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

If input is still high the device will turn on again after the measured temperature has dropped below the thermal hysteresis.

Figure 15 shows this simplified behavior.

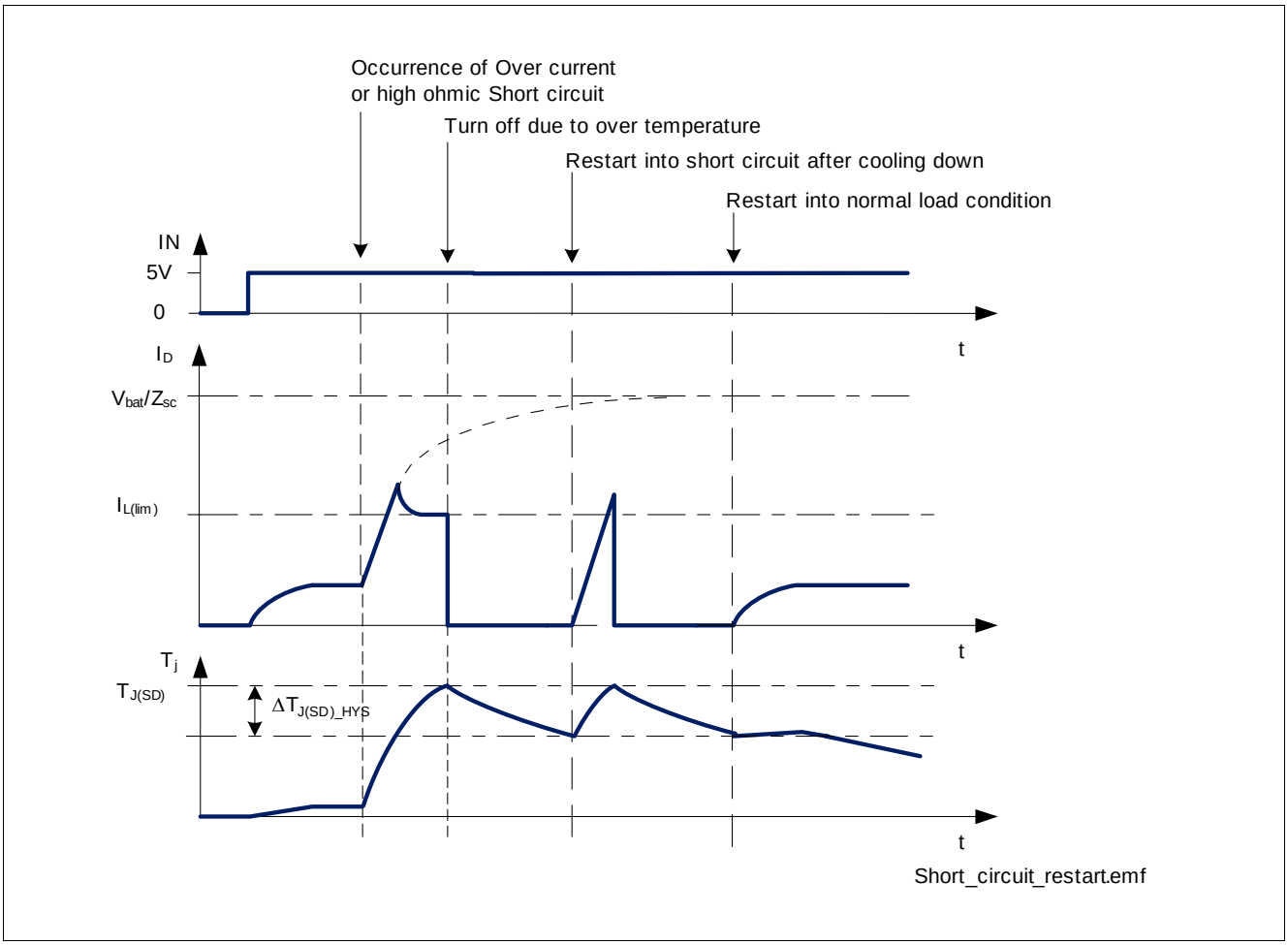


Figure 15 Short circuit protection via current limitation and over temperature switch off with auto-restart

6.4 Characteristics

Please see **"Protection Functions" on Page 18** for electrical characteristic table.

7 Input Stage

7.1 Input Circuit

Figure 16 shows the input circuit of the BTS3080EJ. In case of open or floating input pin the device will automatically switch off and remain off. An ESD Zener structure protects the input circuit against ESD pulses.

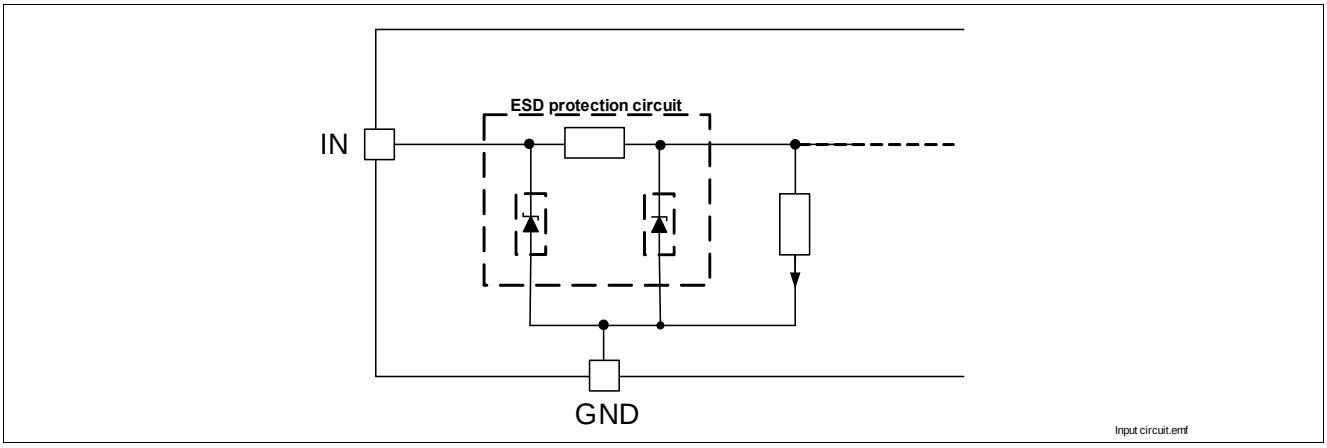


Figure 16 Simplified Input circuitry

7.2 Characteristics

Please see **“Input Stage” on Page 25** for electrical characteristic table.

8 Diagnostics

The BTS3080EJ provides a latching digital status signal via an open drain style feedback on the STATUS pin.

In case of a detected over temperature condition, the device pulls the STATUS pin down to GND (pin) by an internal pull-down intend to signal a low level to the micro controller. This pull-down signal stays active also during thermal restart until the input pin is pulled-down below the input threshold.

In normal operation the status needs to be externally pulled up to a 3 V/5 V supply to signal a high level.

Figure 17 shows this simplified behavior.

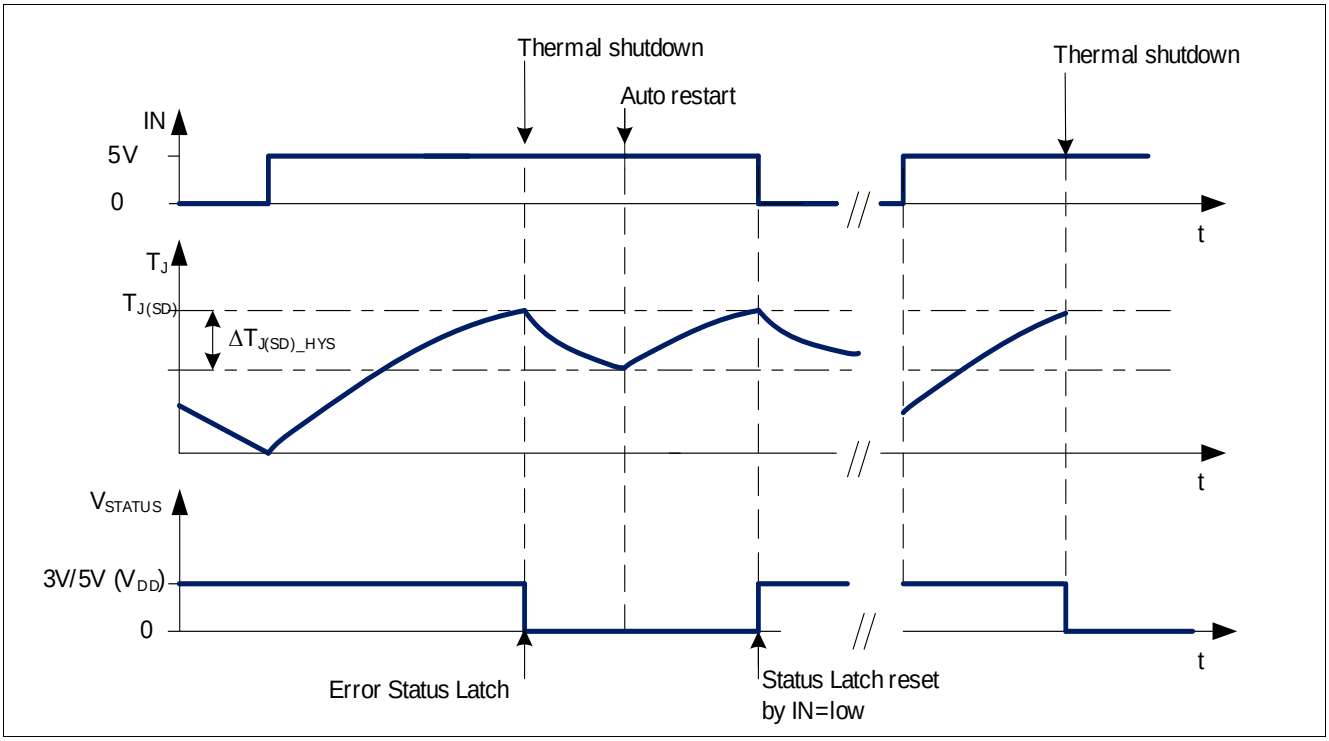


Figure 17 Short circuit protection via current limitation and over temperature switch off with auto-restart and signaling via STATUS pin

9 Electrical Characteristics

9.1 Power Stage

Please see Chapter **"Power Stage" on Page 14** for parameter description and further details.

Table 5 Electrical Characteristics: Power Stage

T_j = -40°C to +150°C, V_{BAT} =6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Stage							
On-State resistance at hot temperature (150°C)	$R_{DS(ON)\_150}$	–	134	160	mΩ	T_J = 150°C; V_{IN} = 5 V; I_L = $I_{L(NOM)}$	P_9.1.5
On-State resistance at ambient temperature (25°C)	$R_{DS(ON)\_25}$	–	69	–	mΩ	T_J = 25°C; V_{IN} = 5 V; I_L = $I_{L(NOM)}$	P_9.1.11
Nominal load current	$I_{L(NOM)}$	–	3	–	A	[1] T_J < 150°C; T_A = 85°C V_{IN} = 5 V	P_9.1.41
OFF state load current, Output leakage current	$I_{L(OFF)\_85}$	–	–	0.6	µA	[2] V_{BAT} = 13.5 V; V_{IN} = 0 V; T_J ≤ 85°C	P_9.1.47
OFF state load current, Output leakage current	$I_{L(OFF)\_150}$	–	0.5	2	µA	V_{BAT} = 18 V; V_{IN} = 0 V; T_J = 150°C	P_9.1.53
Reverse body diode forward voltage	$-V_{OUT}$	–	0.8	1.1	V	I_L = $-I_{L(NOM)}$; V_{IN} = 0 V	P_9.1.67

Table 5 Electrical Characteristics: Power Stage (cont'd)

T_j = -40°C to +150°C, V_{BAT} =6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Dynamic characteristics - switching timessingle pulseV_{BAT} = 13.5 V, R_L = 4.7Ω; for definition details see Figure 10 "Definition of Power Output Timing for Resistive Load" on Page 14							
Turn-on time	t_{ON}	35	75	115	µs	3) V_{IN} = 0 V to 5 V; V_{OUT} = 10% V_{BAT}	P_9.1.68
Turn-off time	t_{OFF}	70	135	210	µs	4) V_{IN} = 5 V to 0 V; V_{OUT} = 90% V_{BAT}	P_9.1.69
Turn-on delay time	t_{DON}	5	15	25	µs	V_{IN} = 0 V to 5 V; V_{OUT} = 90% V_{BAT}	P_9.1.70
Turn-off delay time	t_{DOFF}	40	75	120	µs	V_{IN} = 5 V to 0 V; V_{OUT} = 10% V_{BAT}	P_9.1.71
Fall time, Falling output voltage (turn-on)	t_F	30	60	90	µs	V_{IN} = 0 V to 5 V; V_{OUT} = 90% V_{BAT} to V_{OUT} = 10% V_{BAT}	P_9.1.72
Rise time, Rising output voltage	t_R	30	60	90	µs	V_{IN} = 5 V to 0 V; V_{OUT} = 10% V_{BAT} to V_{OUT} = 90% V_{BAT}	P_9.1.73
Turn-on Slew rate	$-(\Delta V/\Delta t)_{ON}$	0.22	0.45	0.65	V/µs	5) V_{OUT} = 90% V_{BAT} to V_{OUT} = 50% V_{BAT}	P_9.1.74
Turn-off Slew rate	$(\Delta V/\Delta t)_{OFF}$	0.22	0.45	0.65	V/µs	6) V_{OUT} = 50% V_{BAT} to V_{OUT} = 90% V_{BAT}	P_9.1.75

1) Not subject to production test, calculated by R_{thJA} (JEDEC 2s2p, PCB) and $R_{DS(ON)}$
2) Not subject to production test, specified by design;
3) Not subject to production test, calculated with delay time ON and fall time
4) Not subject to production test, calculated with delay time OFF and rise time
5) Not subject to production test, calculated slew rate between 90% and 50% V_{OUT}
6) Not subject to production test, calculated slew rate between 50% and 90% V_{OUT}

9.2 Protection

Please see Chapter **"Protection Functions" on Page 18** for parameter description and further details.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

Table 6 Electrical Characteristics: Protection

T_j = -40°C to +150°C, V_{BAT} =6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Protection							
Thermal shut down junction temperature	$T_{J(SD)}$	150	175	–	°C	1) 3 V < V_{IN} < 5.5 V	P_9.2.1
Thermal hysteresis	ΔT_{J_HYS}	–	15	–	K	1)	P_9.2.3
Minimum status latch reset time	t_{RESET}	50	–	–	µs	1) 2) V_{IN} < *0.8 V;*	P_9.2.8
Overvoltage Protection							
Drain clamp voltage	$V_{OUT(CLAMP)}$	40	45	–	V	V_{IN} = 0 V; I_L = 6 mA	P_9.2.13
Current limitation (see also Figure 15)							
Current limitation	$I_{L(LIM)}$	10	15	20	A	V_{IN} = 5 V	P_9.2.19

1) Not subject to production test, specified by design.
2) Minimum time needed to reset the STATUS latch feedback signal

9.3 Input Stage

Please see Chapter **"Input Stage" on Page 20** for description and further details.

Table 7 Electrical Characteristics: Input

T_j = -40°C to +150°C, V_{BAT} =6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input							
Input Current, normal ON state	$I_{IN(ON)}$	–	82	120	µA	V_{IN} = 5.0 V;	P_9.3.1
Input Current, protection mode	$I_{IN(PROT)}$	–	165	220	µA	V_{IN} = 5.0 V;	P_9.3.7
Input current, inverse condition on OUT to GND	$I_{IN(-VOUT)}$	–	15	–	mA	1) 2) V_{OUT} < -0.3 V; -0.3 V ≤ V_{IN} <5.5 V	P_9.3.9
Input pull down current	I_{IN-GND}	10	–	–	µA	3) V_{IN} = $V_{IN(TH)}$	P_9.3.10
Input Voltage on-threshold	$V_{IN(TH)}$	0.8	2.3	3	V	I_L =0.6 mA; Power DMOS active	P_9.3.11

1) Not subject to production test, specified by design
2) Input current must not exceed the maximum ratings in Chapter 4, P_4.1.10
3) Not subject to production test, specified by design

9.4 Diagnostics (STATUS Pin)

Please see Chapter **"Diagnostics" on Page 21** for description and further details.

Table 8 Electrical Characteristics: Diagnostics

T_j = -40°C to +150°C, V_{BAT} =6 V to 18 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Status pin voltage drop	$V_{STATUS(ON)}$	–	–	0.65	V	I_{STATUS} = 1 mA; latched fault; 3 V≤ V_{IN} < 5.5 V	P_9.4.1
Status pin leakage current (85°C)	$I_{STATUS(OFF)\_85}$	–	1.5	6	µA	1) V_{STATUS} ≤ 5.5 V; T_J ≤ 85°C; 3 V≤ V_{IN} < 5.5 V	P_9.4.2
Status pin leakage current (150°C)	$I_{STATUS(OFF)\_150}$	–	6	12	µA	V_{STATUS} ≤ 5.0 V; T_J = 150°C; 3 V≤ V_{IN} < 5.5 V	P_9.4.3

1) Not subject to production test, specified by design.

10 Characterization Results

Typical performance characteristics.

10.1 Power Stage

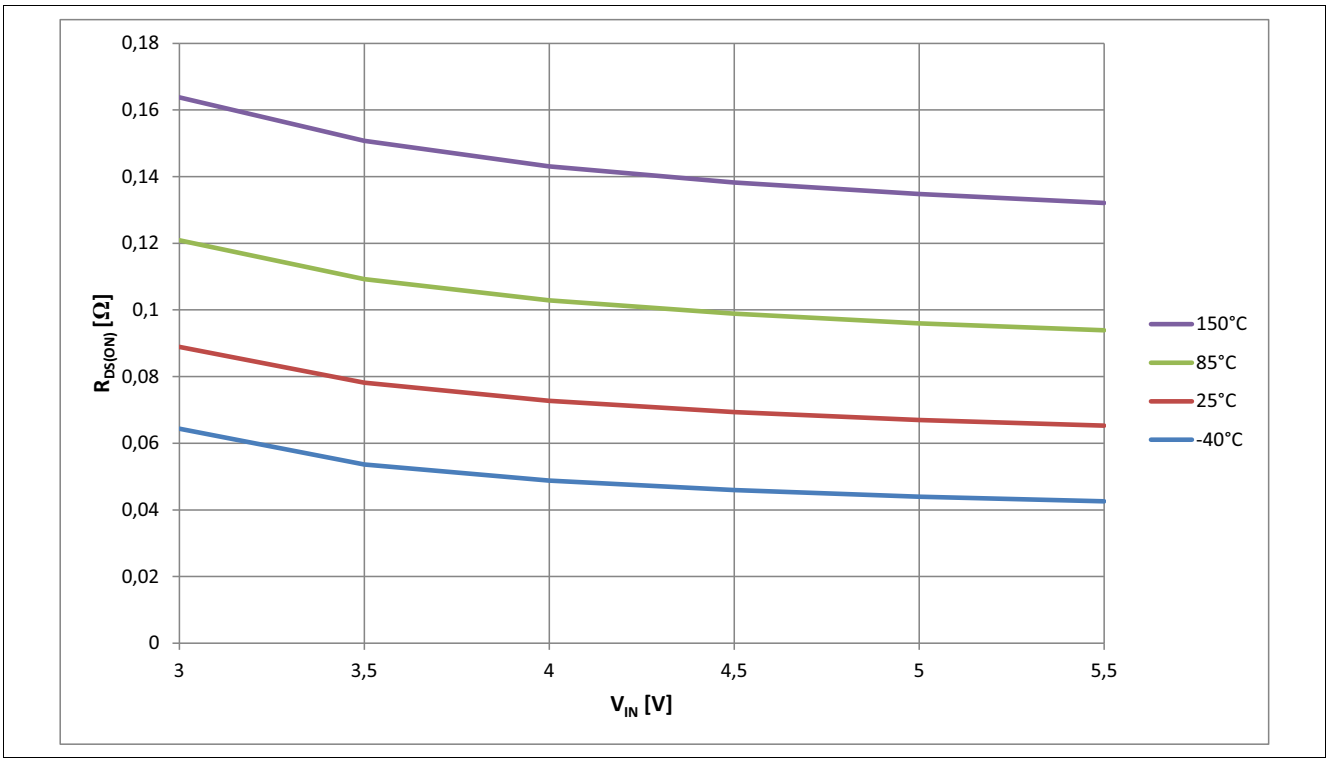


Figure 18 typical $R_{DS(ON)}$ vs. V_{IN} @ T_J = -40 … 150°C, I_L = $I_{L(NOM)}$

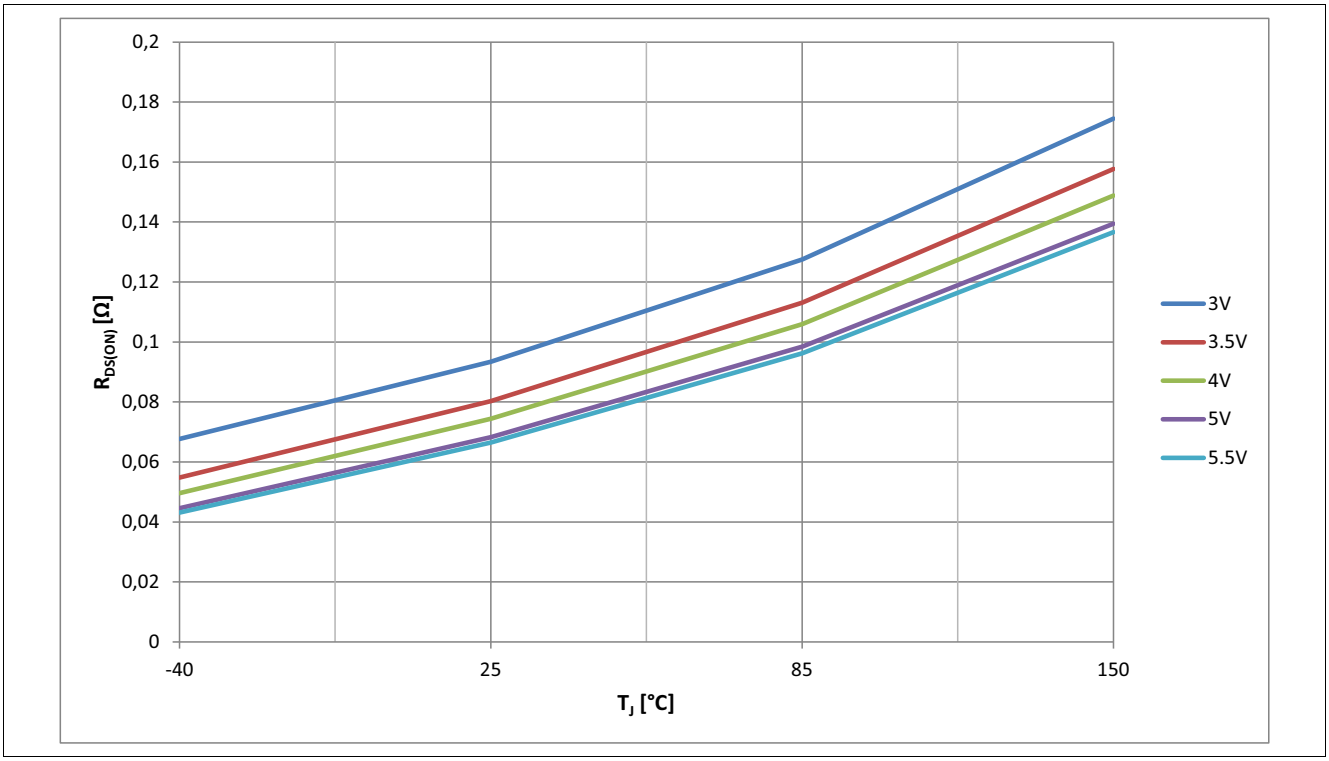


Figure 19 Typical $R_{DS(ON)}$ vs. T_J @ V_{IN} = 3 … 5.5 V; I_L = $I_{L(NOM)}$

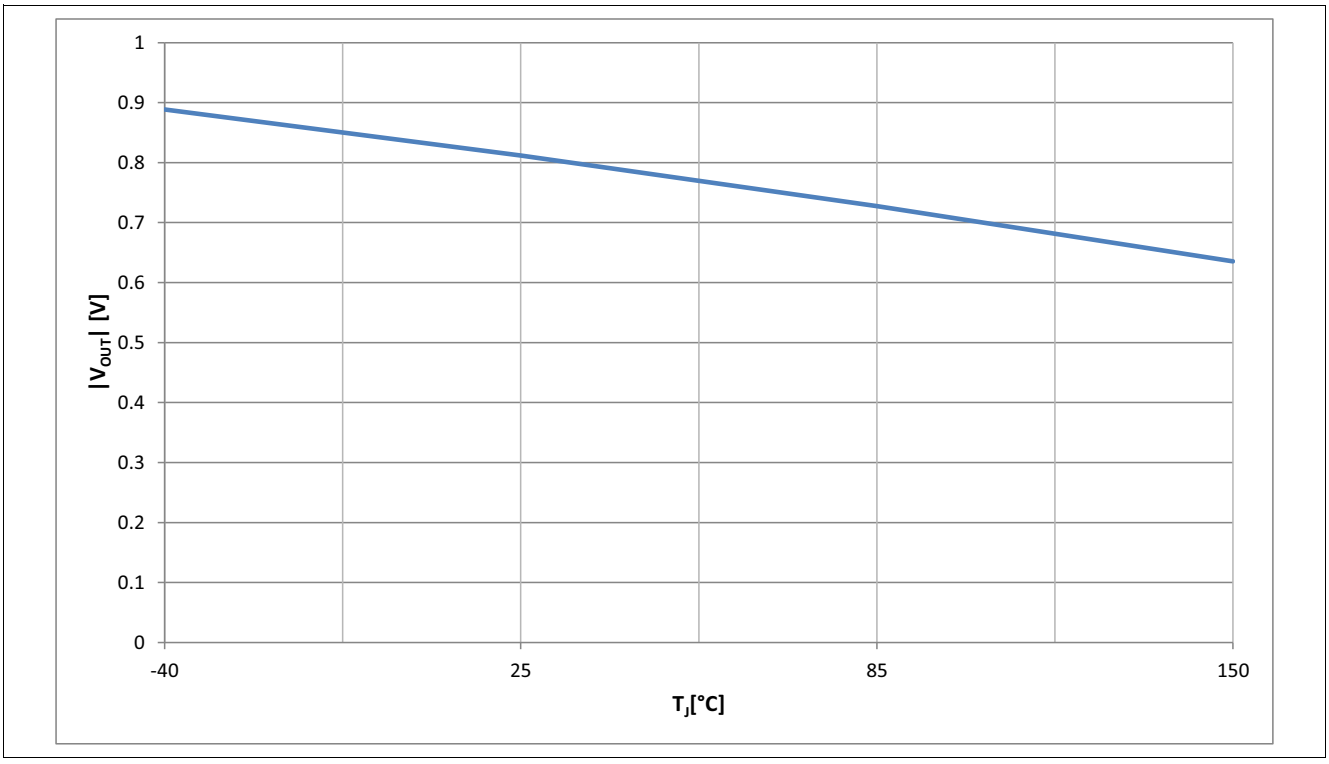


Figure 20 Typical Reverse Diode $|V_{OUT}|$ vs. T_J @ I_L = -$I_{L(NOM)}$

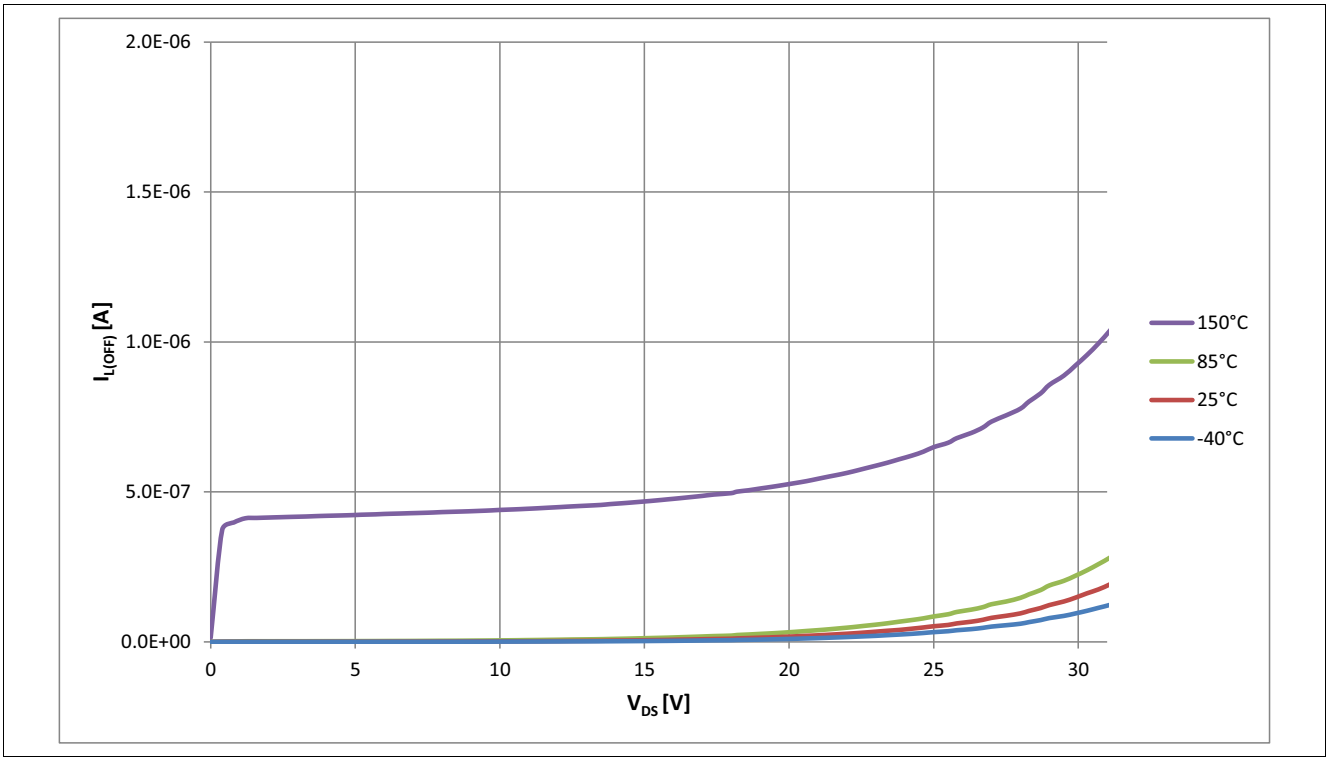


Figure 21 Typical $I_{L(OFF)}$ vs. V_{DS} @ T_J = -40 … 150°C, V_{IN} = 0 V

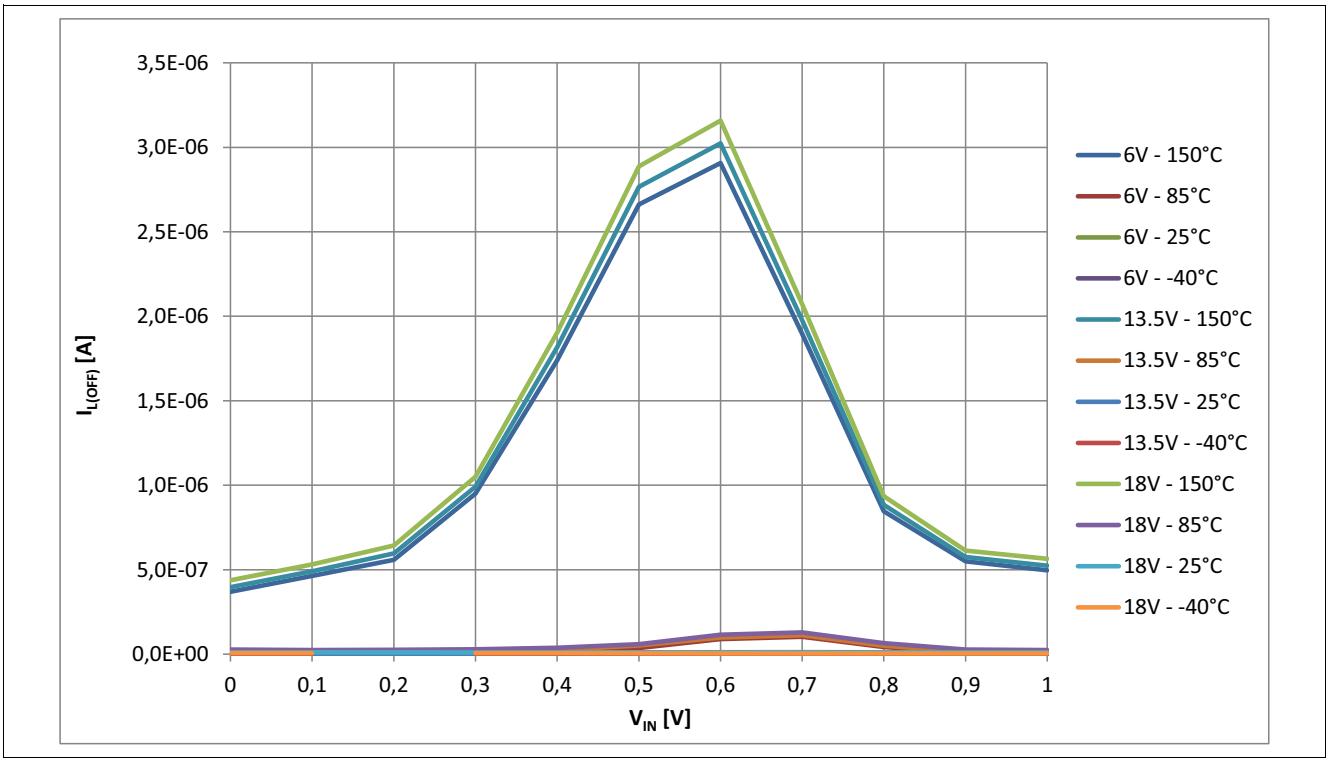


Figure 22 Typical $I_{L(OFF)}$ vs. V_{IN} @ T_J = -40 … 150°C, V_{BAT} = 6 … 18 V

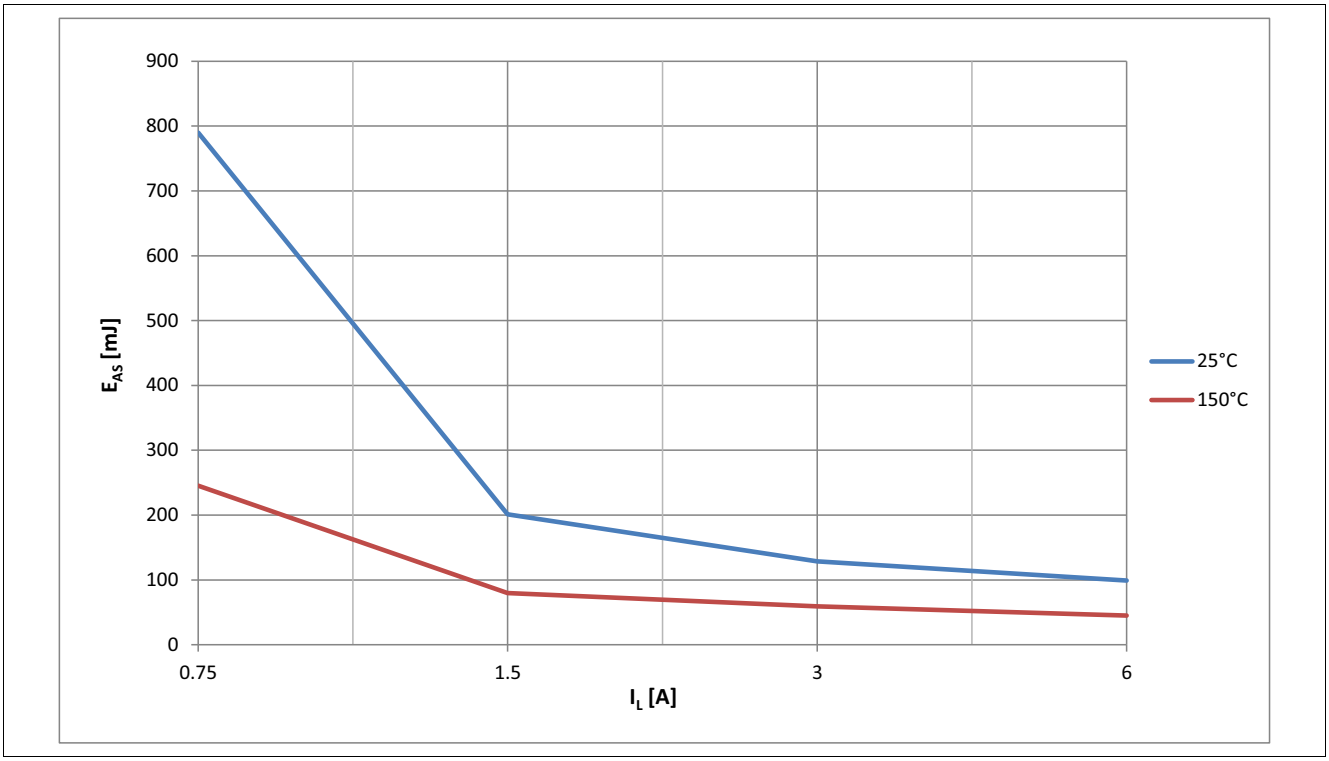


Figure 23 Typical destruction point. E_{AS} vs. I_L @ $T_{J(0)}$ = 25°C and 150°C, V_{BAT} = 13.5 V

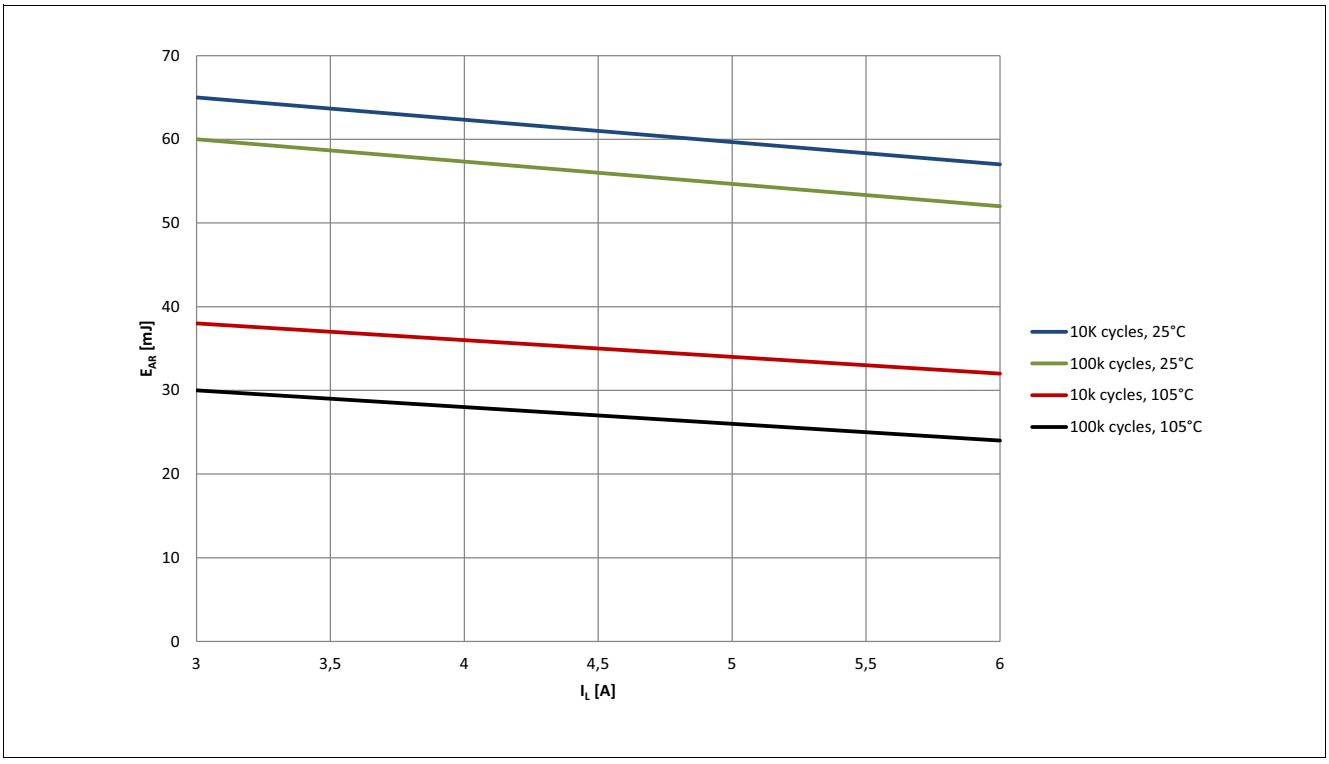


Figure 24 Typical E_{AR} vs. I_L @ $T_{J(0)}$= 25°C and 105°C, V_{BAT} = 13.5 V

Characterization Results

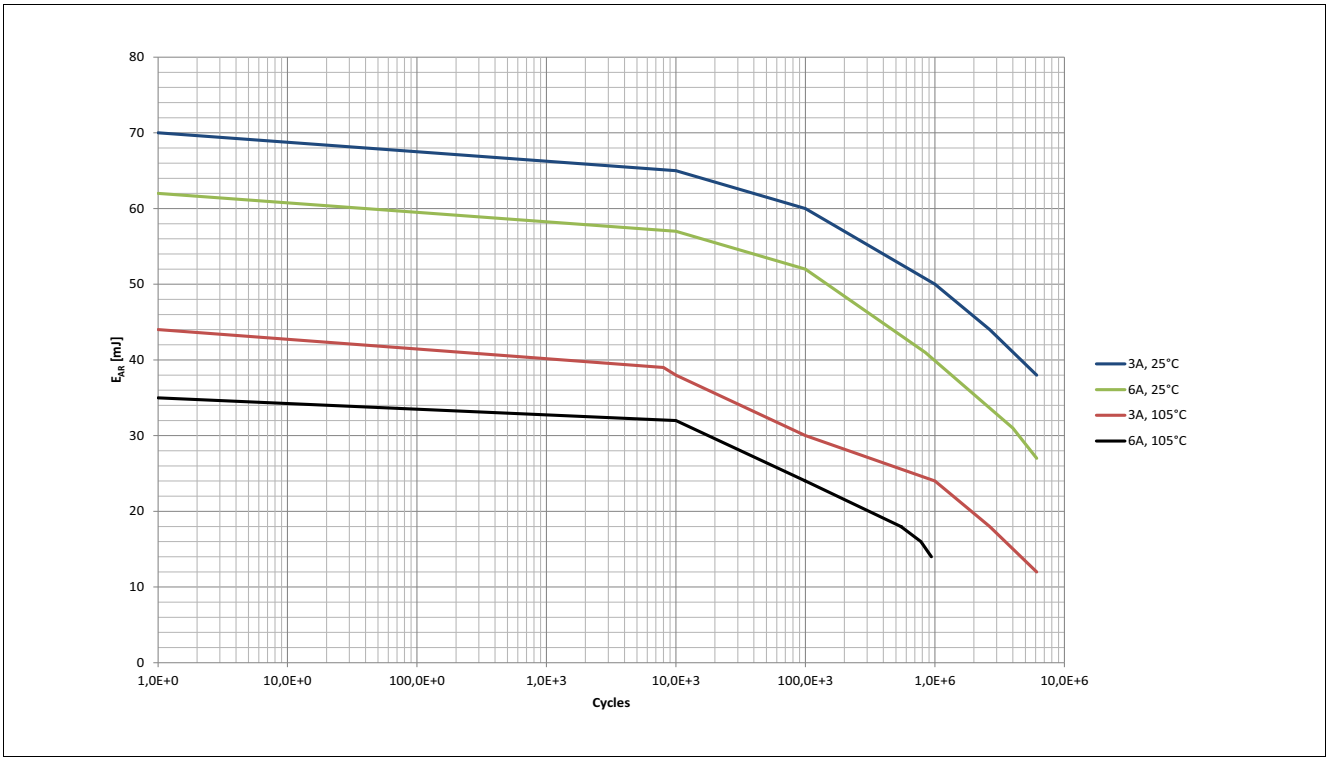


Figure 25 Typical E_{AR} vs. Nr of cycles @ $T_{J(0)}$ = 25°C and 105°C, V_{BAT} = 13.5 V

Dynamic characteristics (switching times):

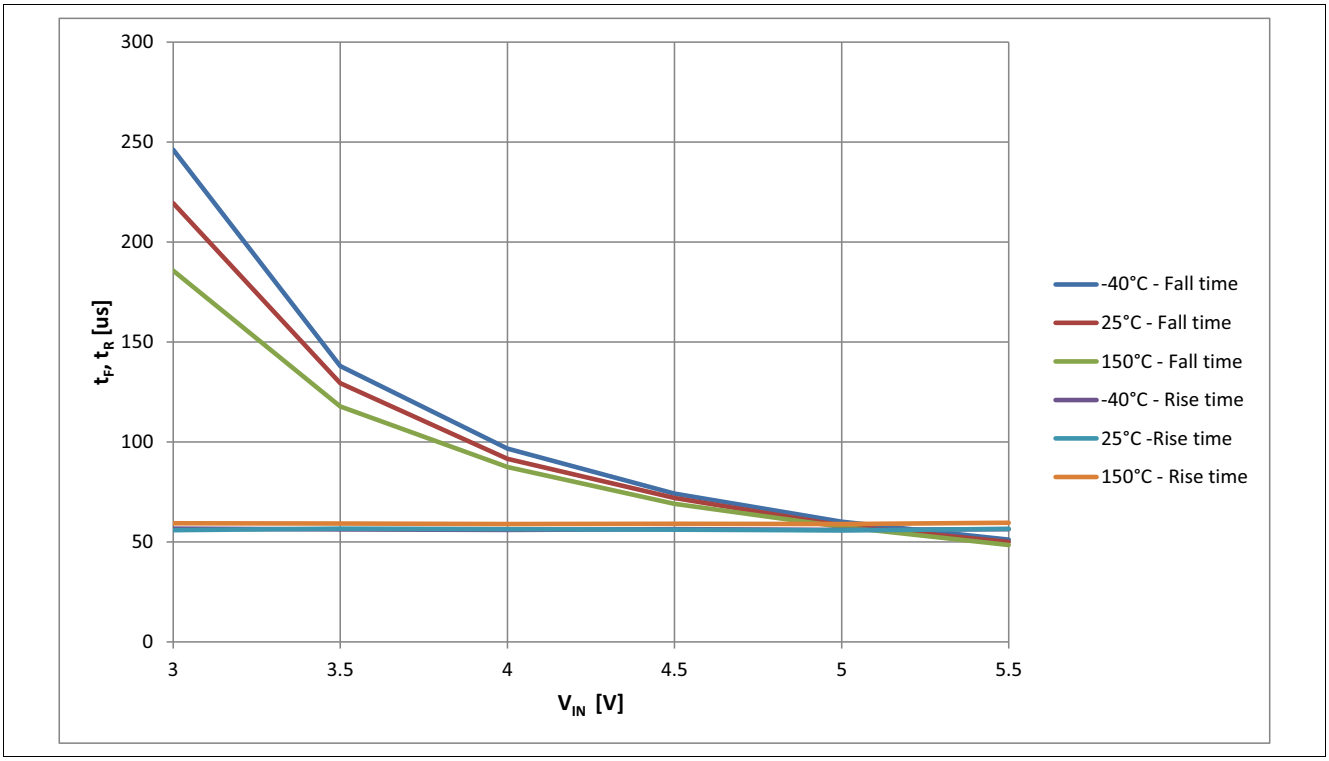


Figure 26 Typical t_F, t_R vs V_{IN} @ T_J = -40 … 150°C

Characterization Results

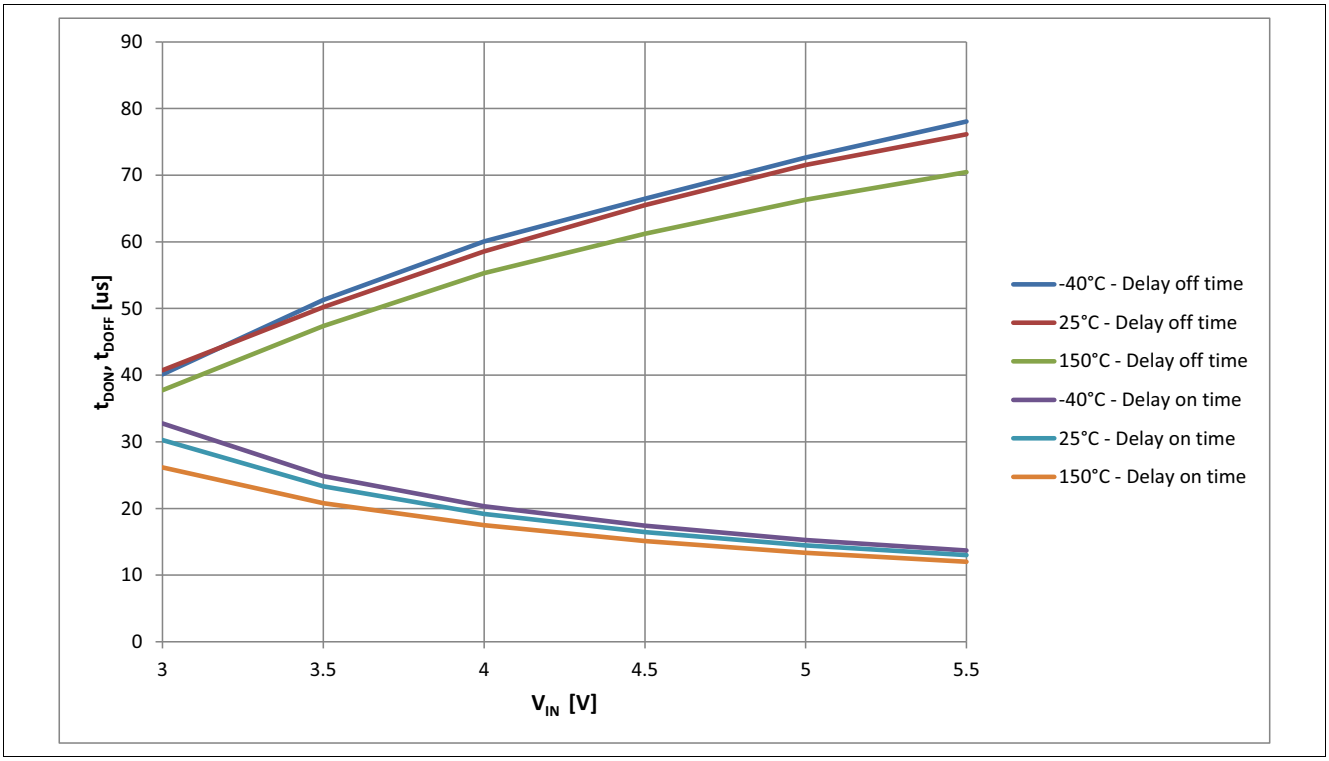


Figure 27 Typical t_{DON}, t_{DOFF} vs V_{IN} @ T_J = -40 … 150°C

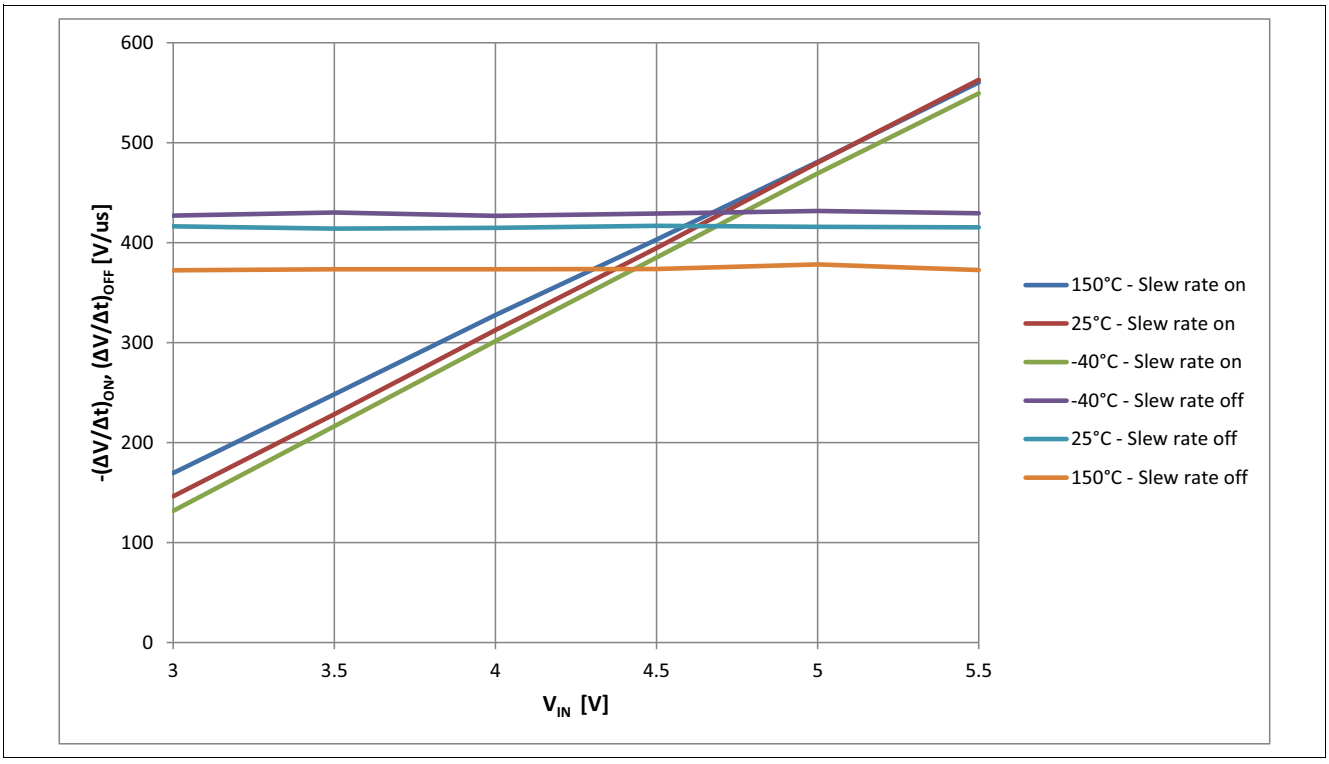


Figure 28 Typical $-(\Delta V/\Delta t)_{ON}$, $(\Delta V/\Delta t)_{OFF}$ vs V_{IN} @ T_J = -40 … 150°C

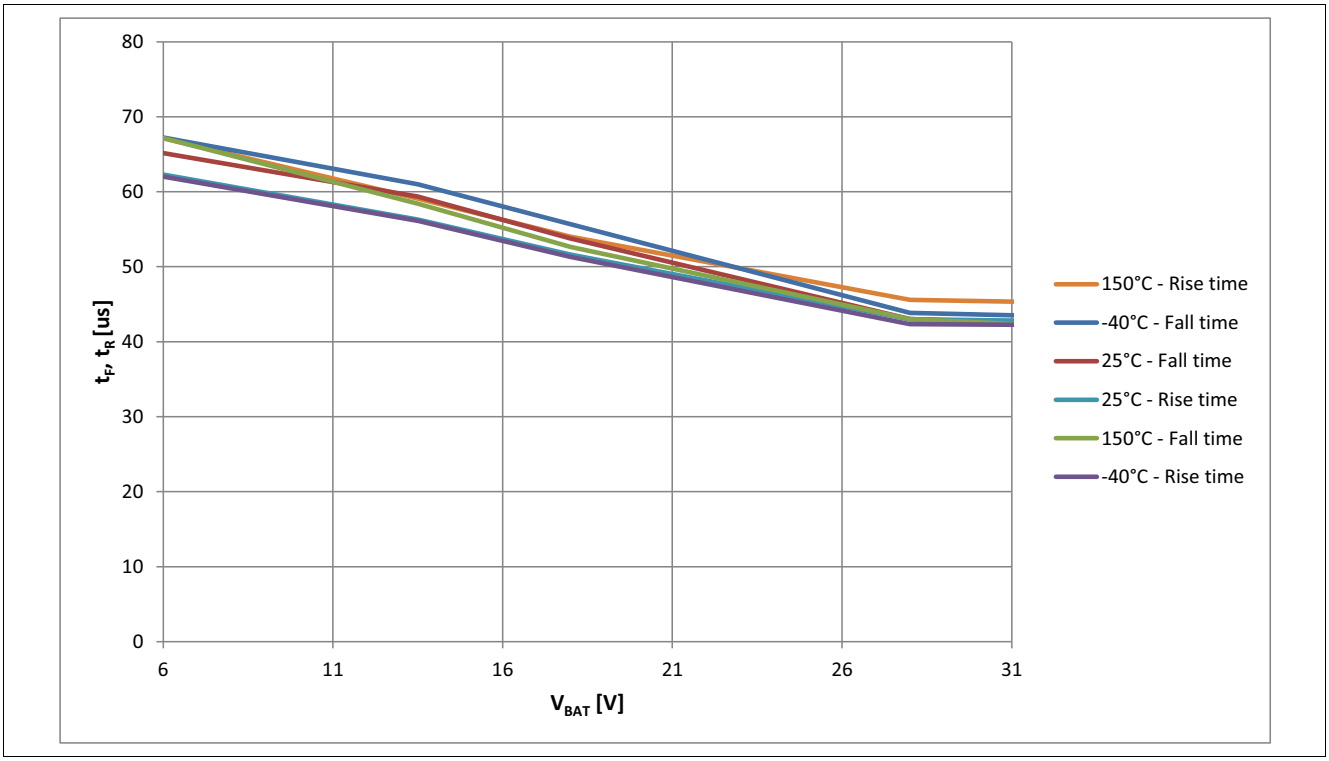


Figure 29 Typical t_F, t_R vs V_{BAT} @ V_{IN} = 5 V, T_J = -40 … 150°C

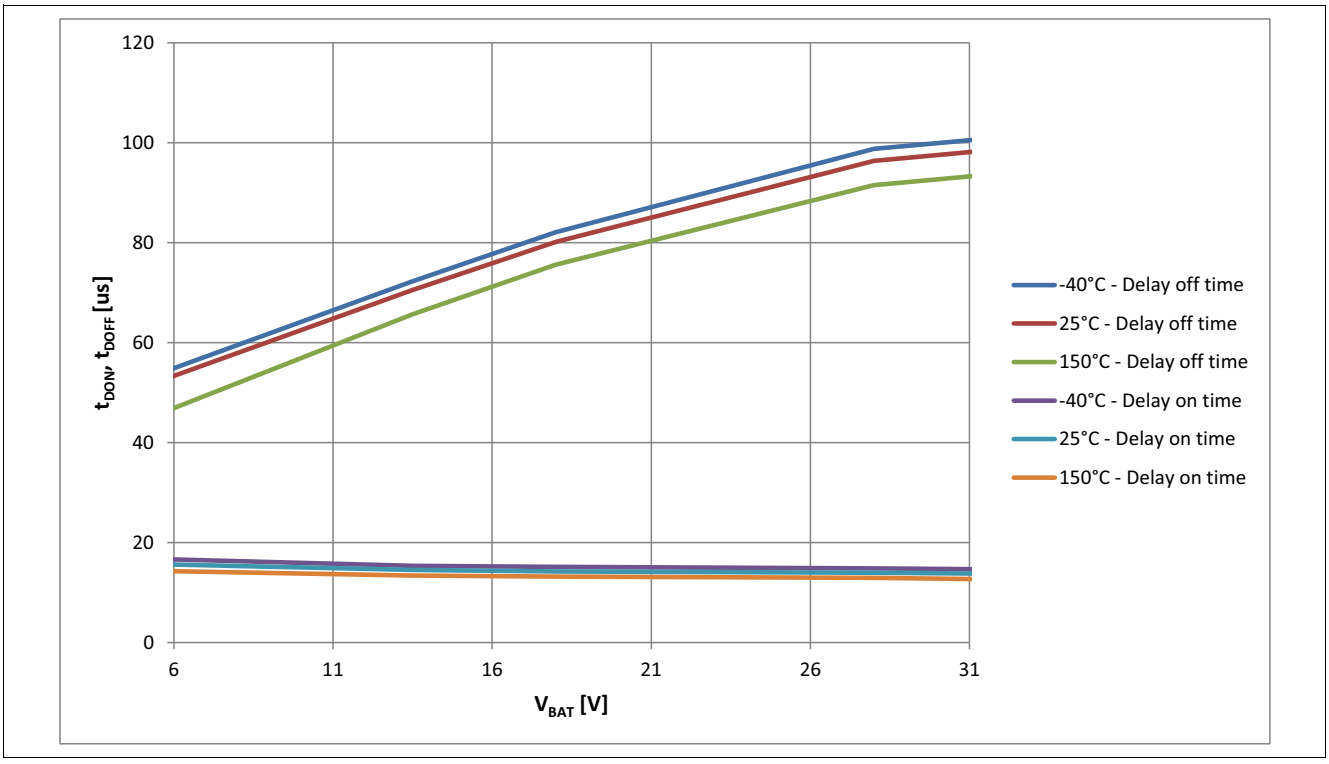


Figure 30 Typical t_{DON}, t_{DOFF} vs V_{BAT} @ V_{IN} = 5 V, T_J = -40 … 150°C

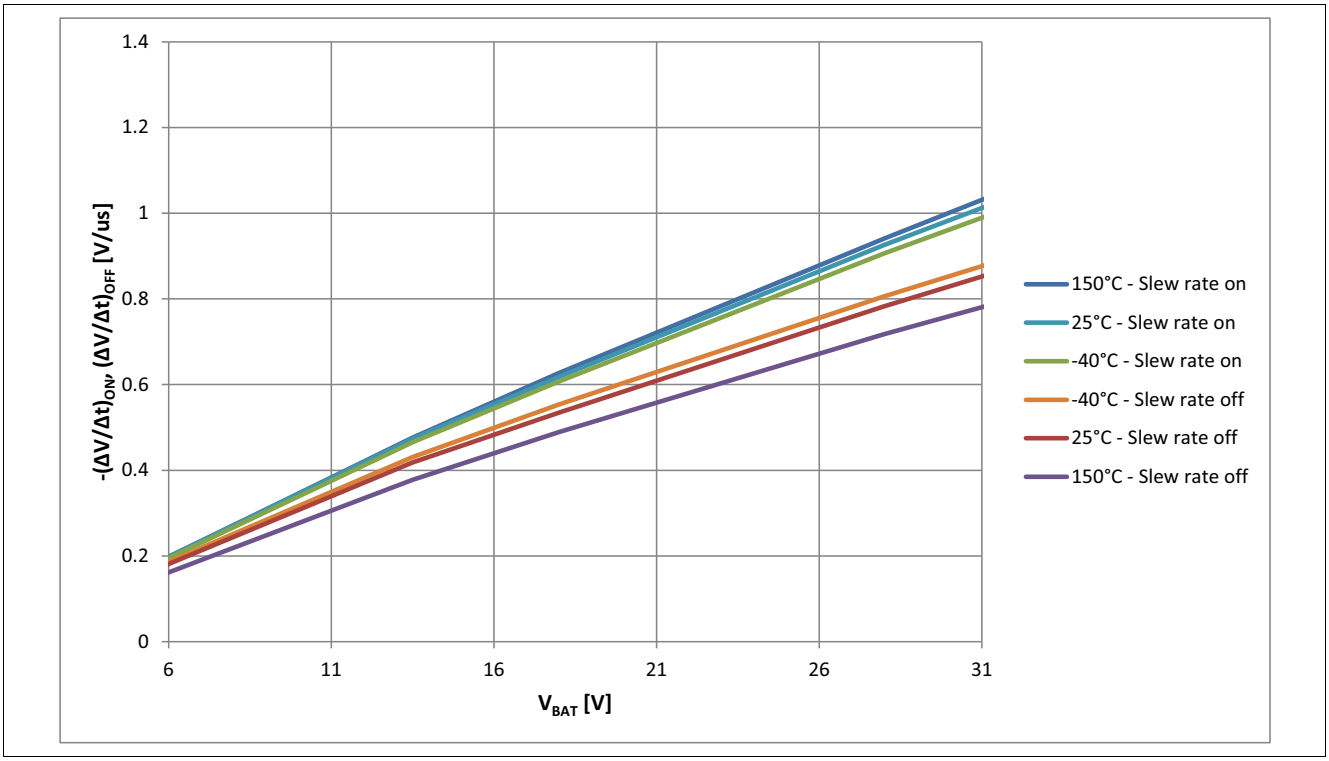


Figure 31 Typical $-(\Delta V/\Delta t)_{ON}$, $(\Delta V/\Delta t)_{OFF}$ vs V_{BAT} @ V_{IN} = 5 V, T_J = -40 … 150°C

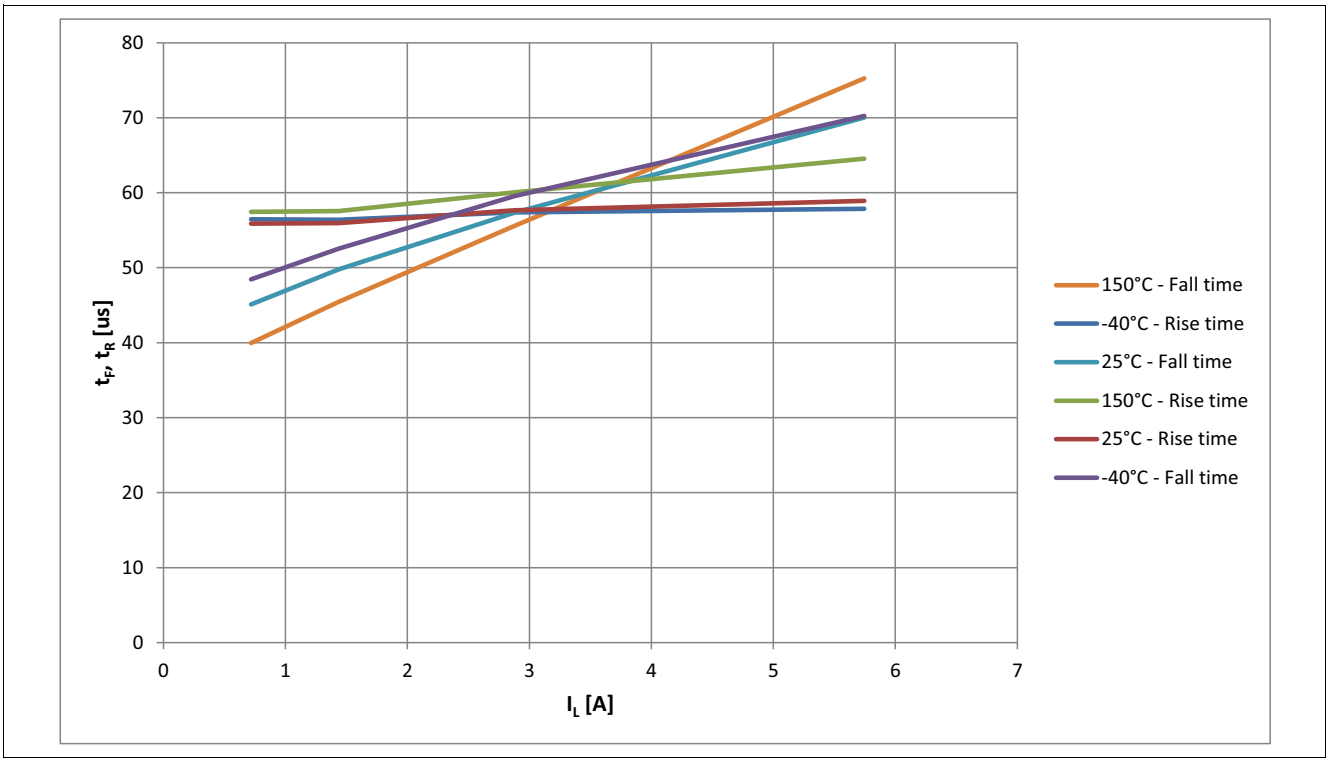


Figure 32 Typical t_F, t_R vs I_L @ V_{IN} = 5 V, T_J = -40 … 150°C

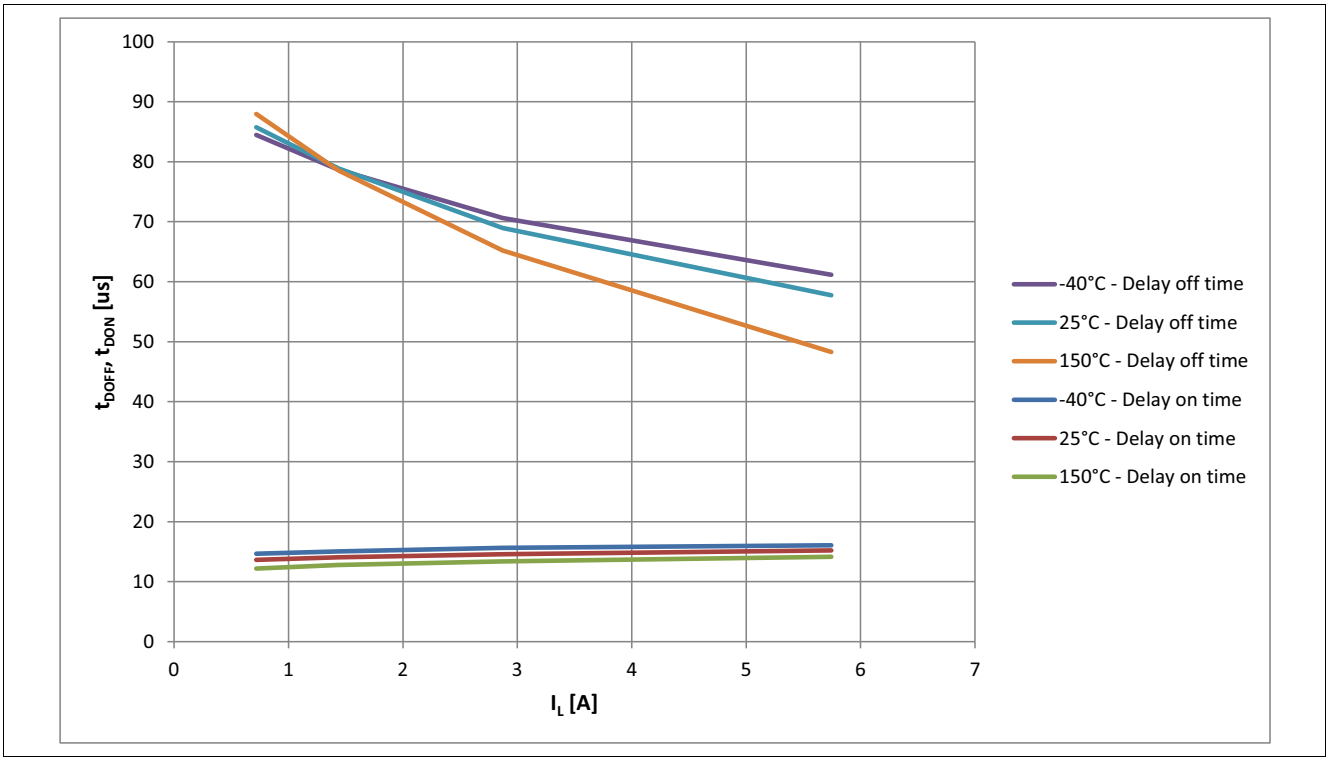


Figure 33 Typical t_{DON}, t_{DOFF} vs I_L @ V_{IN} = 5 V, T_J = -40 … 150°C

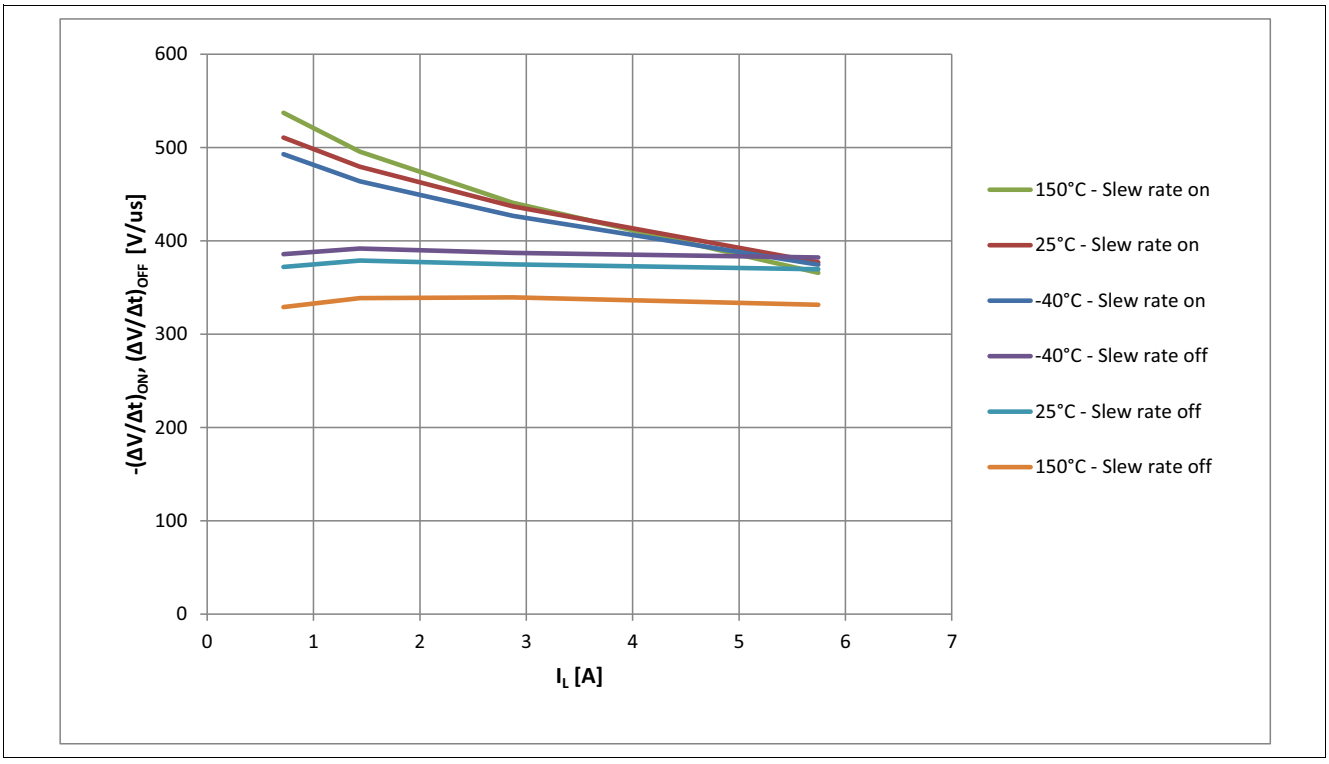


Figure 34 Typical $-(\Delta V/\Delta t)_{ON}$, $(\Delta V/\Delta t)_{OFF}$ vs I_L @ V_{IN} = 5 V, T_J = -40 … 150°C

Characterization Results

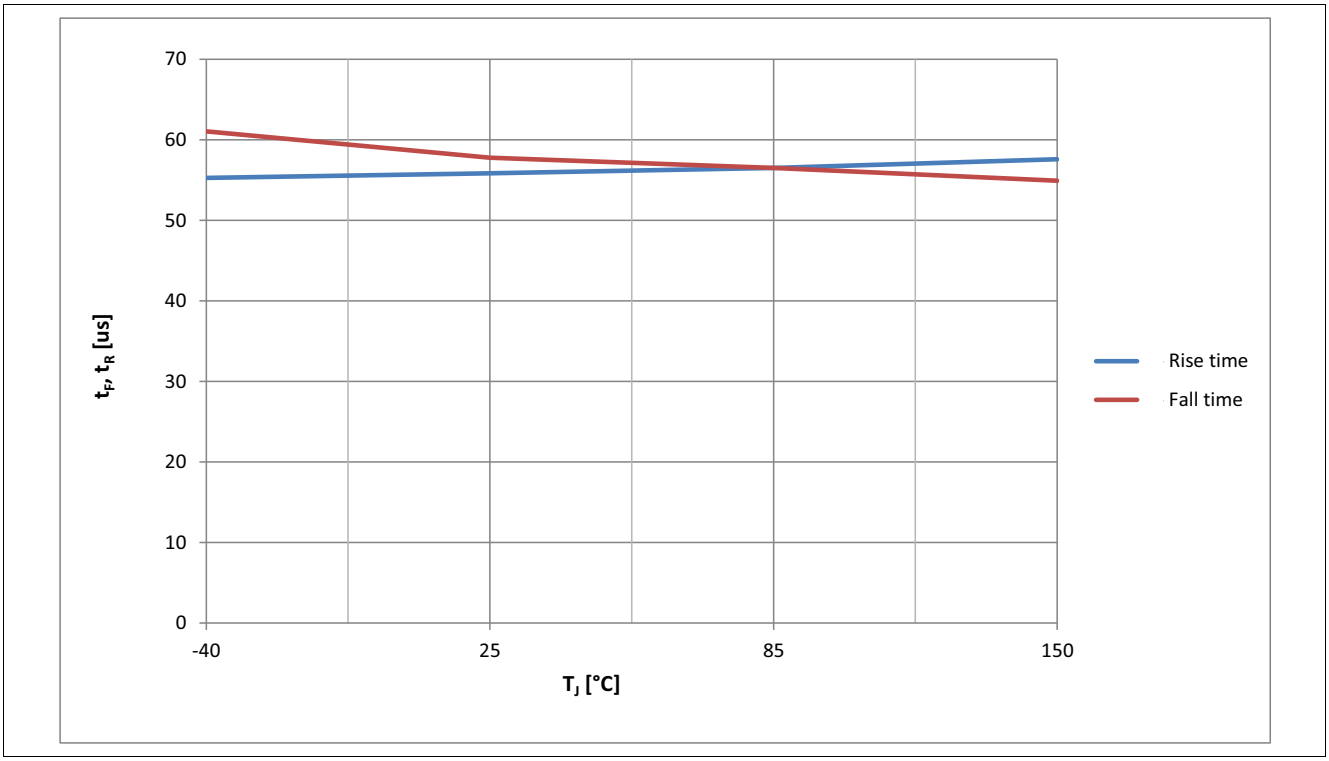


Figure 35 Typical t_F, t_R vs T_J @ V_{IN} = 5 V

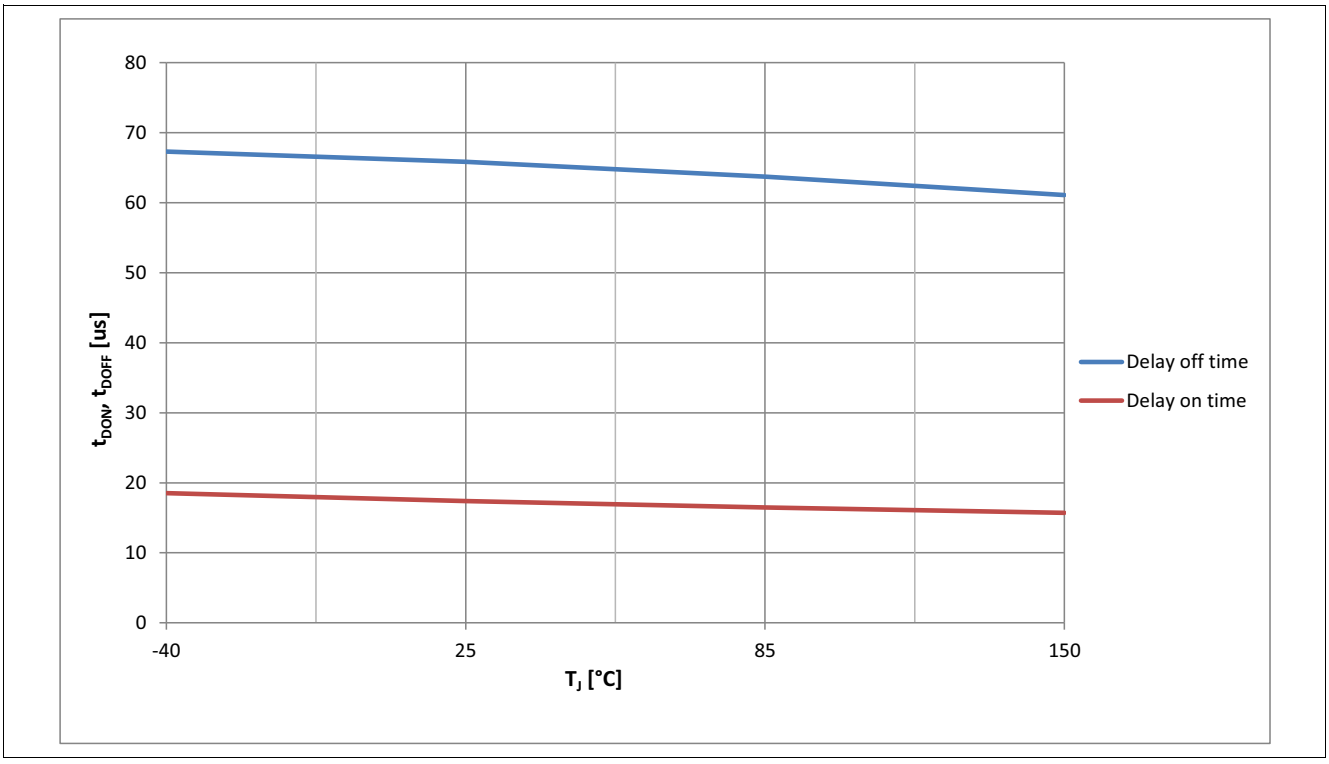


Figure 36 Typical t_{DON}, t_{DOFF} vs T_J @ V_{IN} = 5 V

Characterization Results

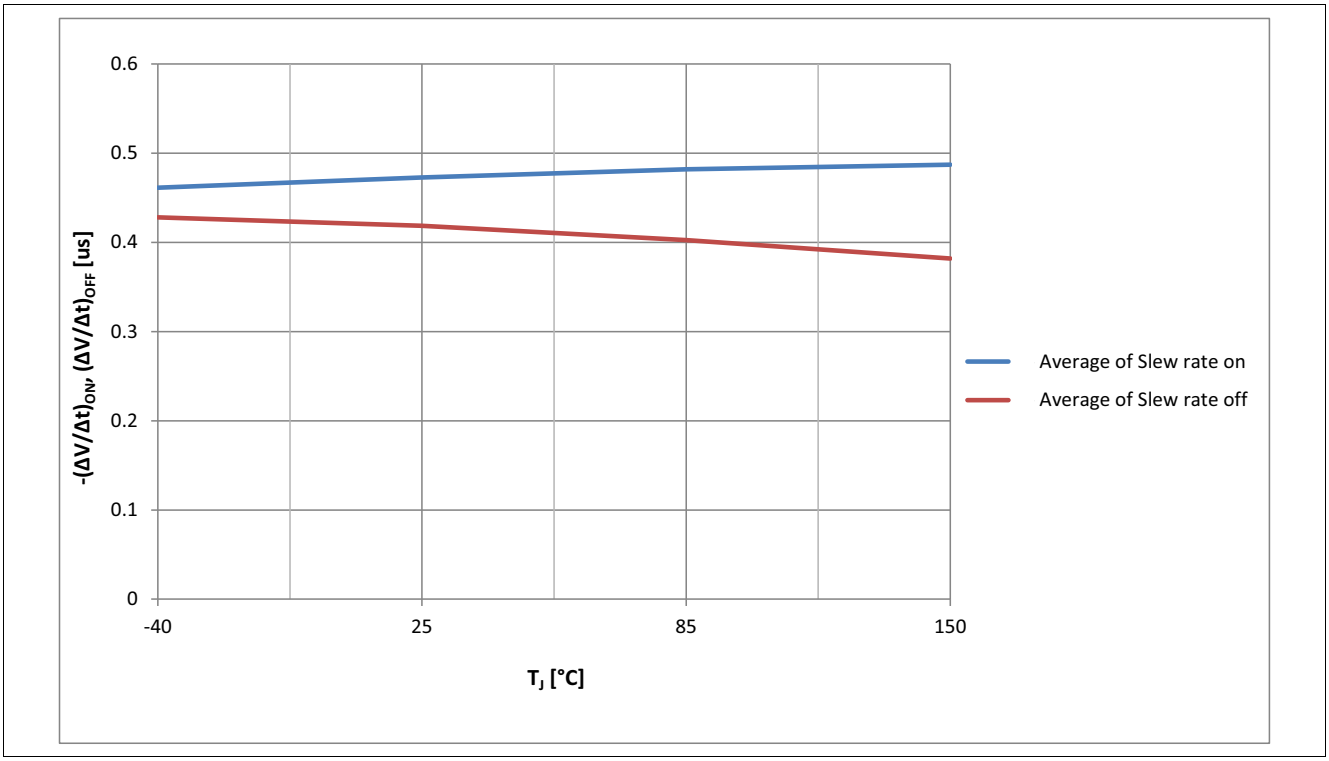


Figure 37 Typical $-(\Delta V/\Delta t)_{ON}$, $(\Delta V/\Delta t)_{OFF}$ vs T_J @ V_{IN} = 5 V

10.2 Protection

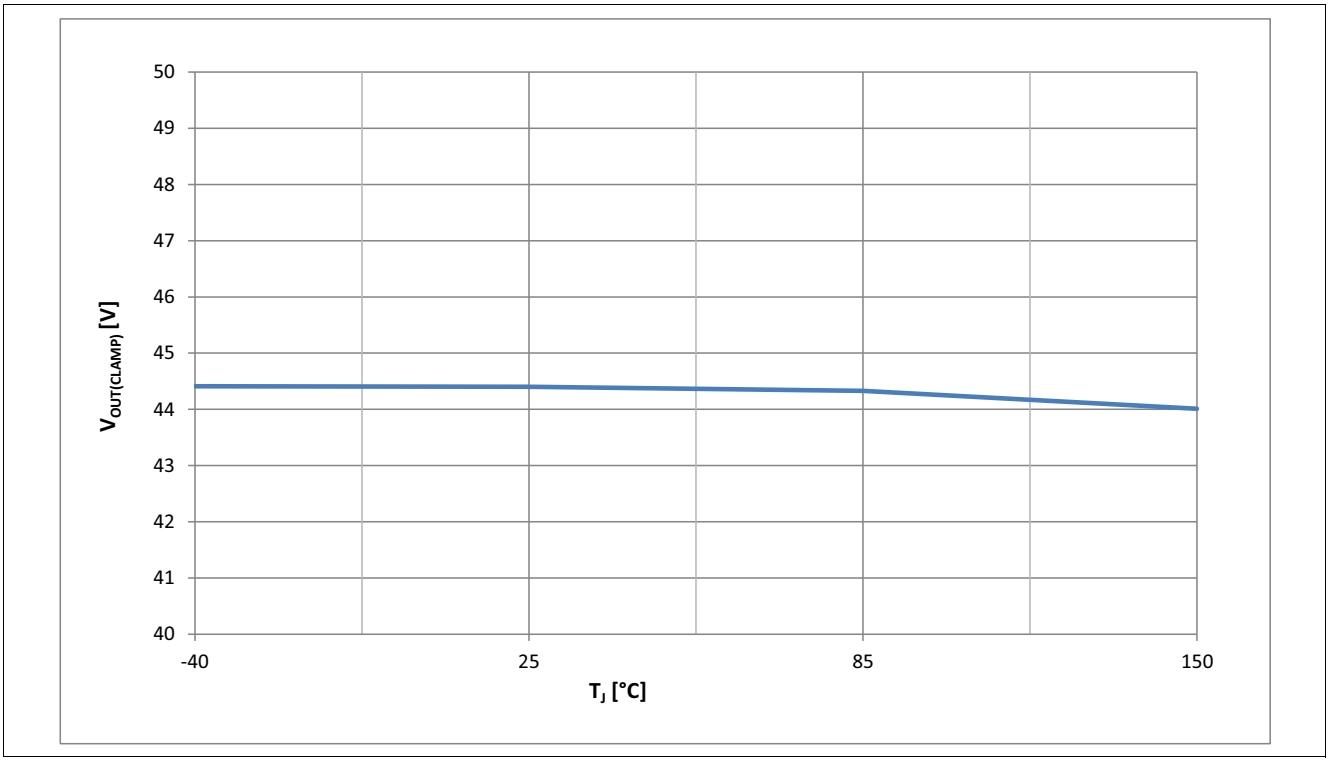


Figure 38 Typical $V_{OUT(CLAMP)}$ vs. T_J @ I_L = 6 mA

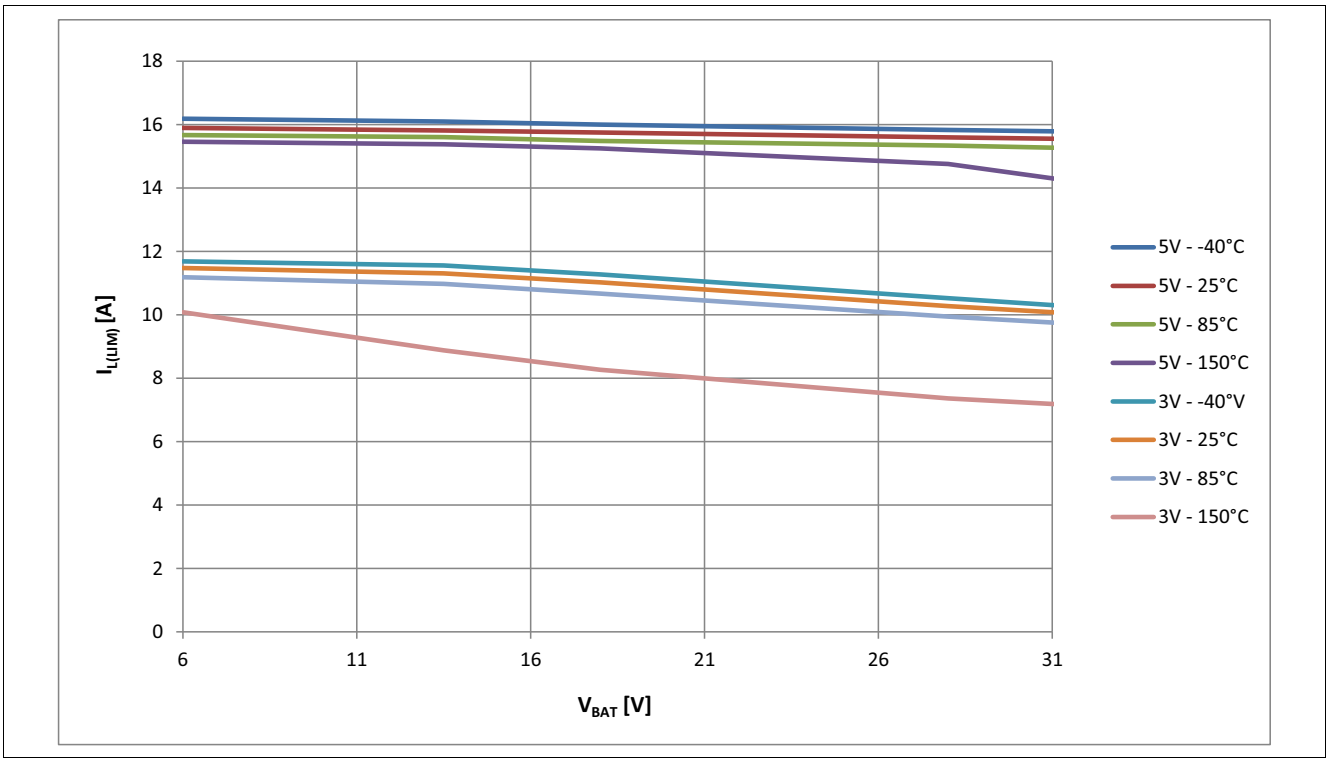


Figure 39 Typical $I_{L(LIM)}$ vs. V_{BAT} @ T_J = -40 … 150°C, V_{IN} = 3 V and 5 V

10.3 Input Stage

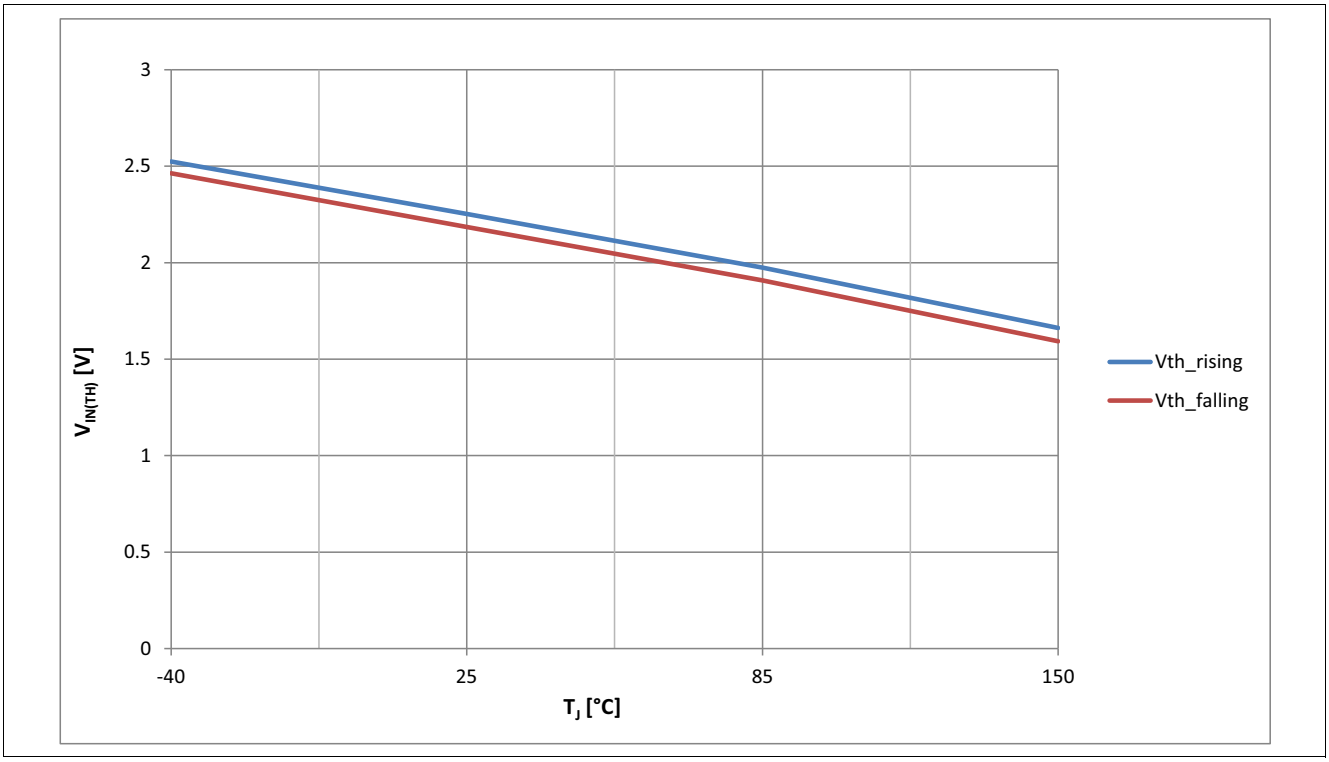


Figure 40 Typical $V_{IN(TH)}$ vs. T_J @ I_L = 0.6 mA

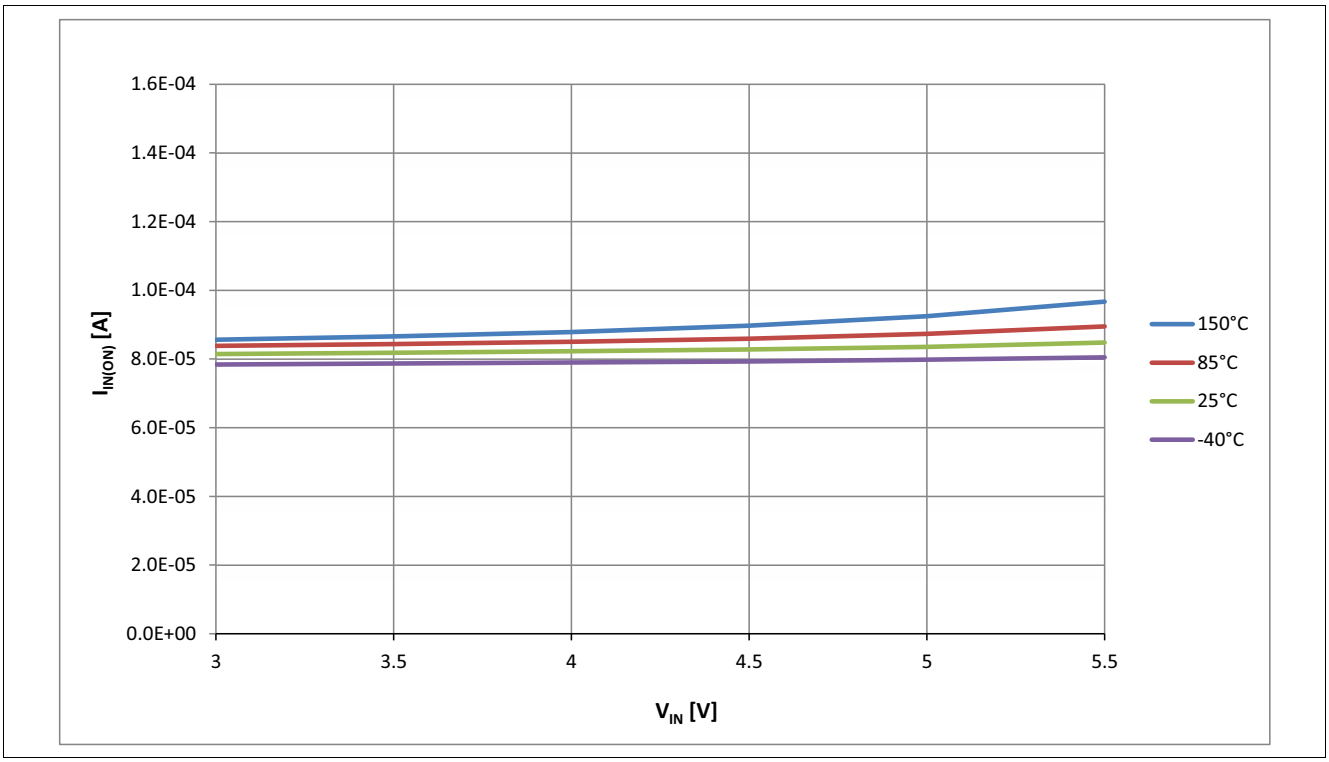


Figure 41 Typical $I_{IN(ON)}$ vs. V_{IN} @ T_J = -40 … 150°C, I_L = $I_{L(NOM)}$

Characterization Results

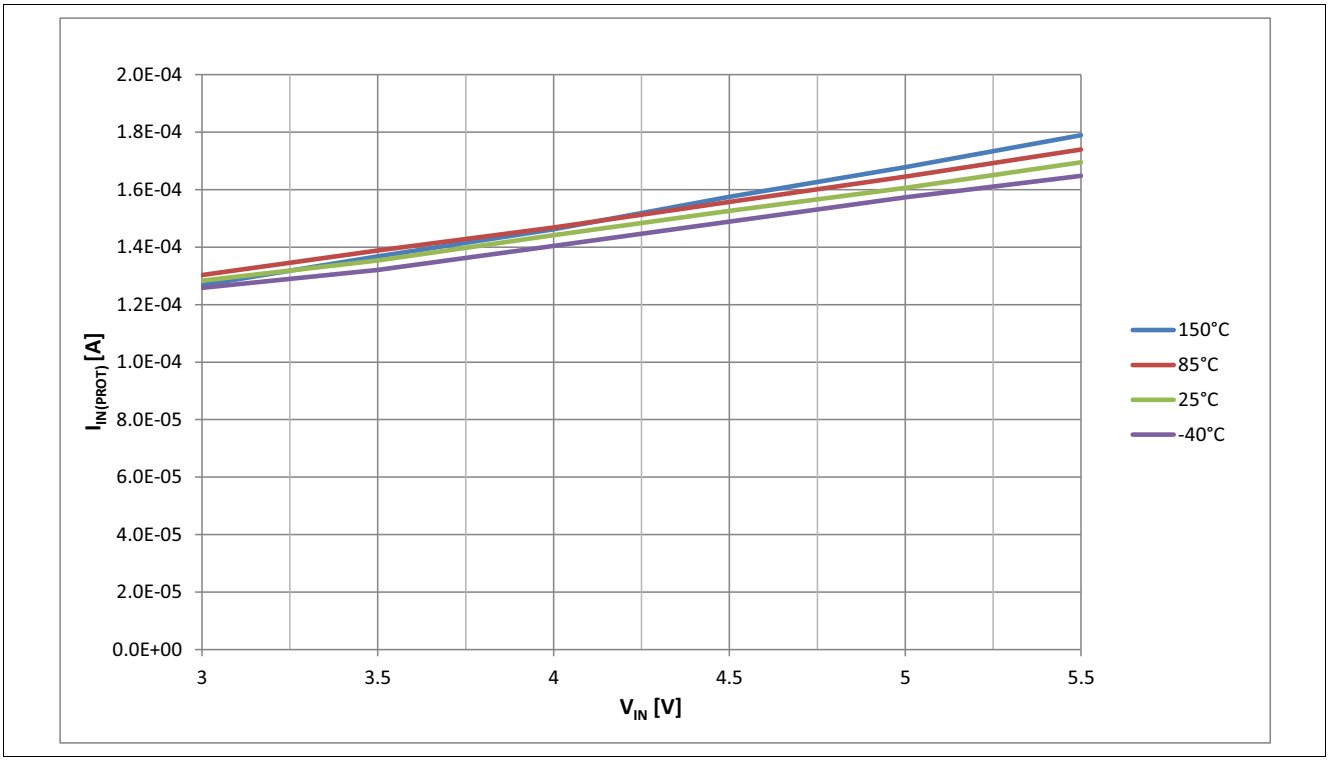


Figure 42 Typical $I_{IN(PROT)}$ vs. V_{IN} @ T_J = -40 … 150°C, I_L = $I_{L(NOM)}$

10.4 Diagnosis

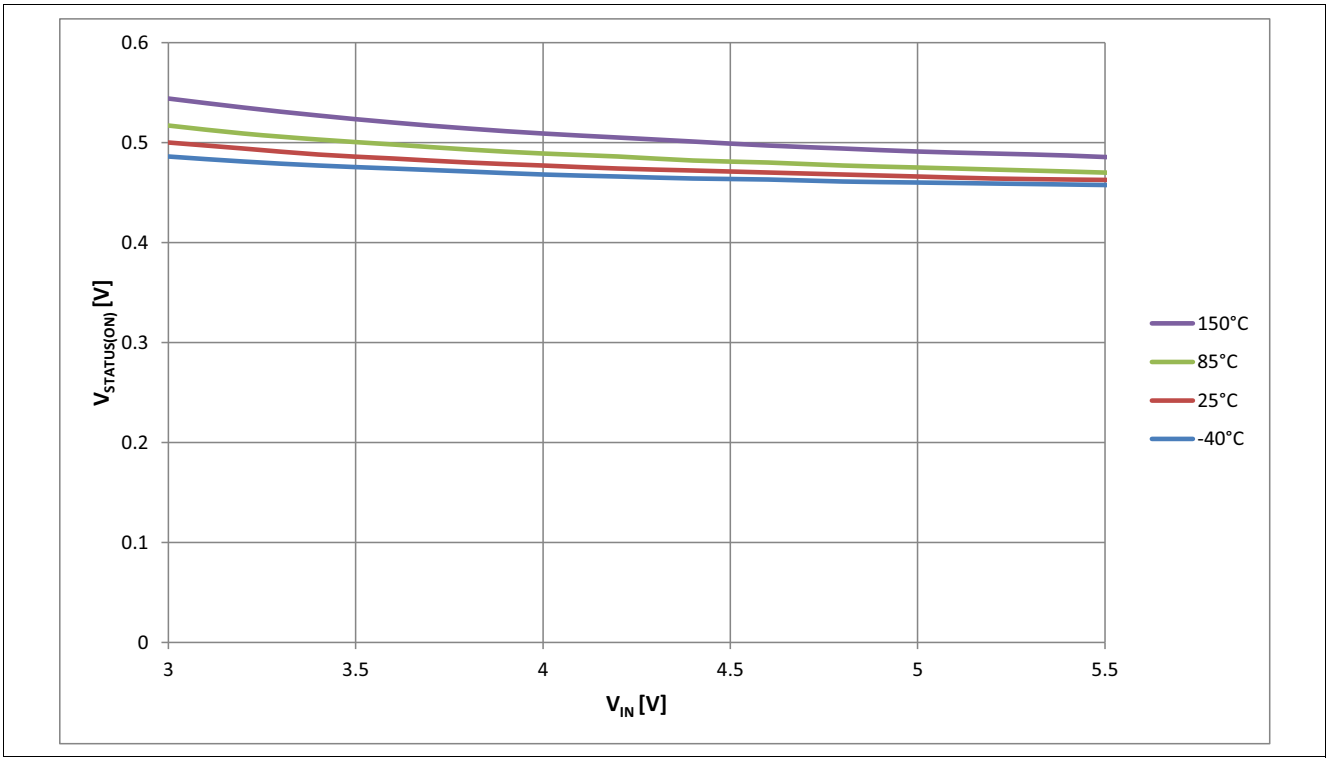


Figure 43 Typical $V_{STATUS(ON)}$ vs. V_{IN} @ T_J = -40 … 150°C

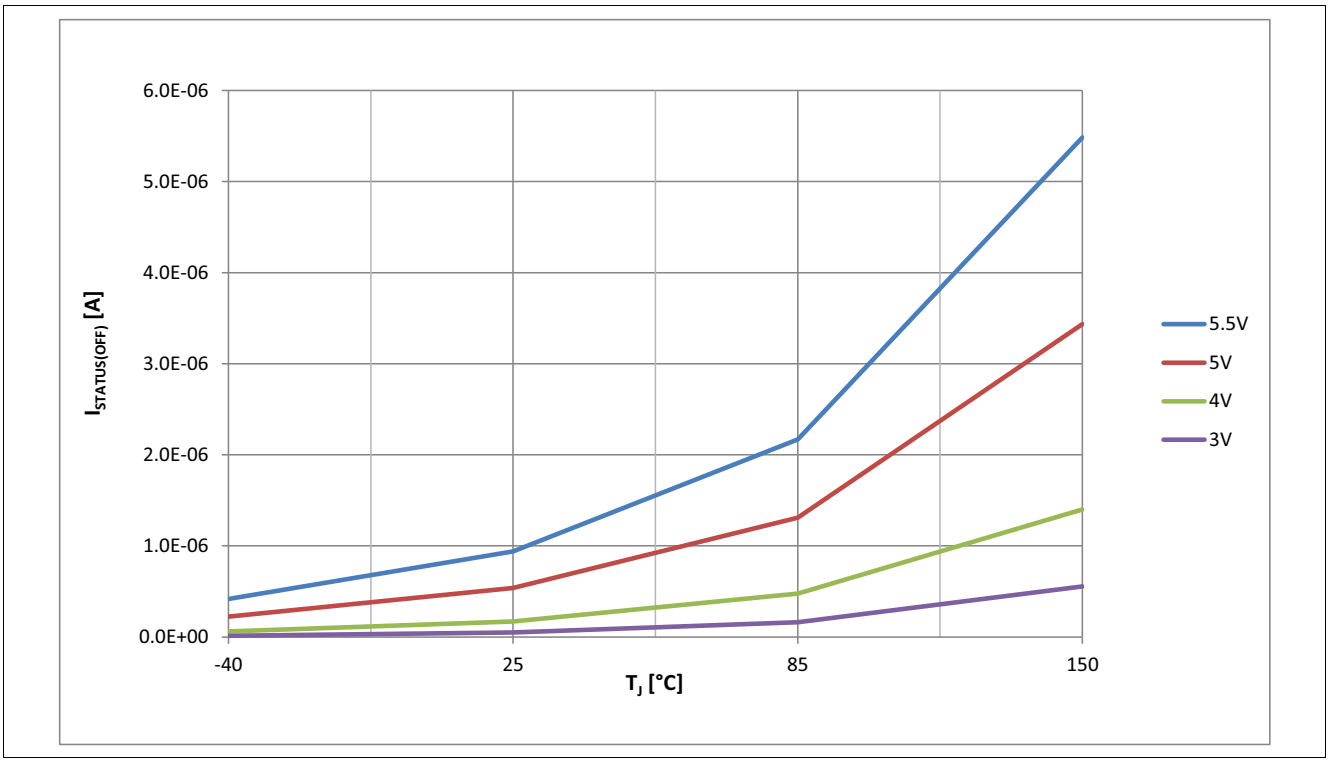


Figure 44 Typical $I_{STATUS(OFF)}$ vs. T_J @ V_{STATUS} = 3 … 5.5 V, V_{IN} = 0 V

Characterization Results

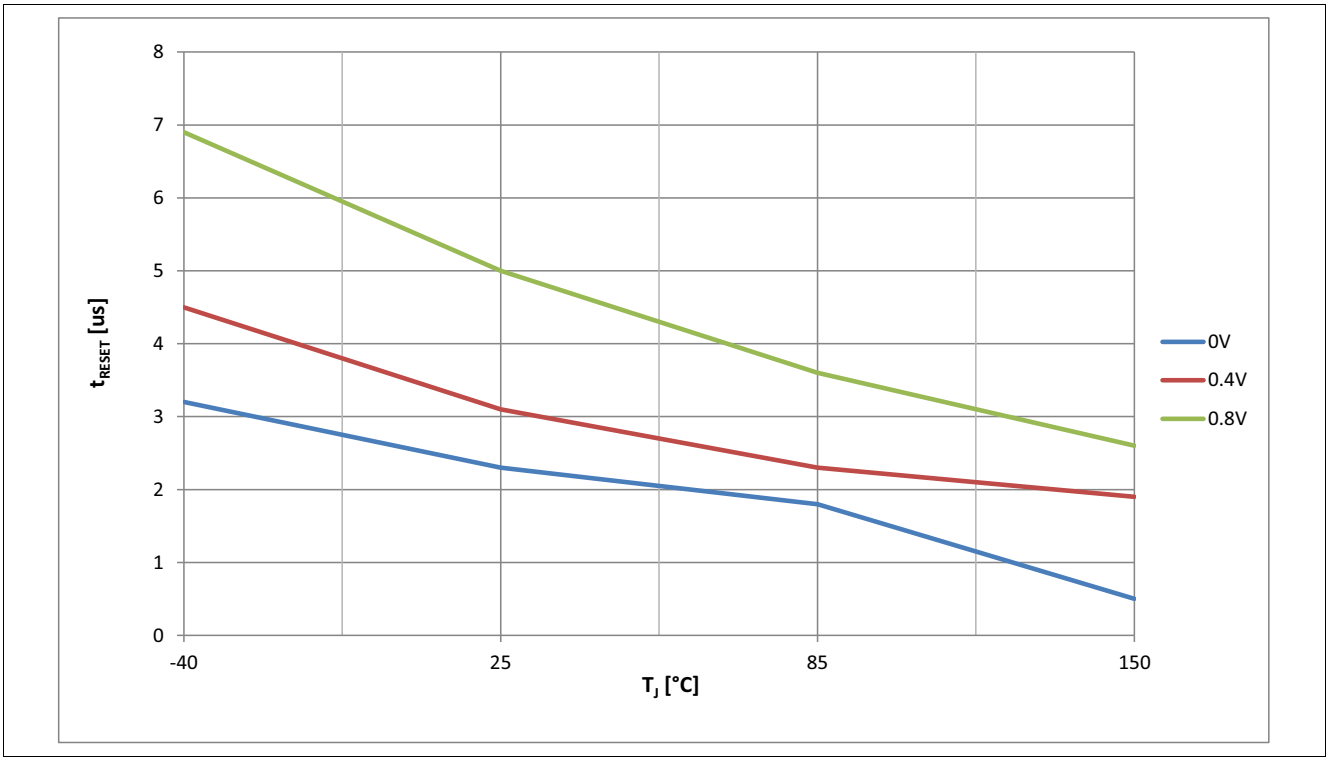


Figure 45 Typical t_{RESET} vs T_J @ V_{IN} = 0 … 0.8 V

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

11.1 Application Diagram

An application example with the BTS3080EJ is shown below.

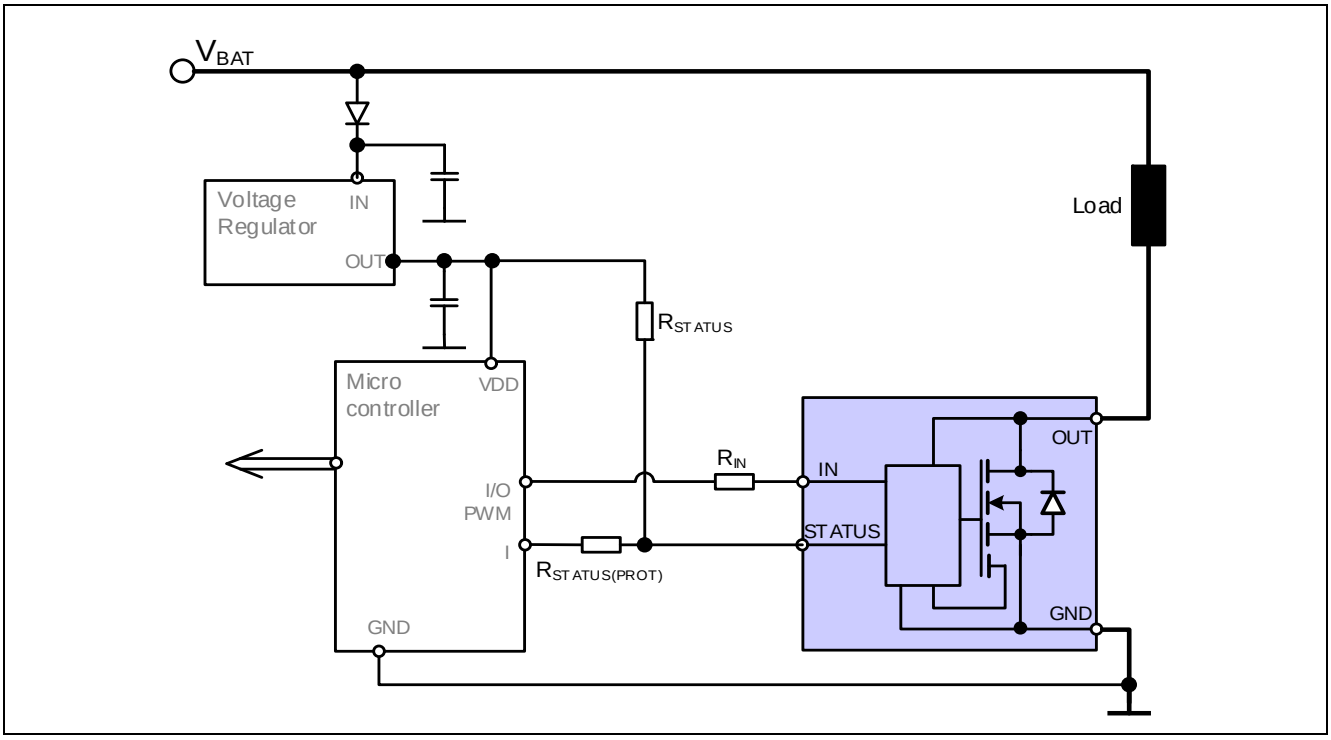
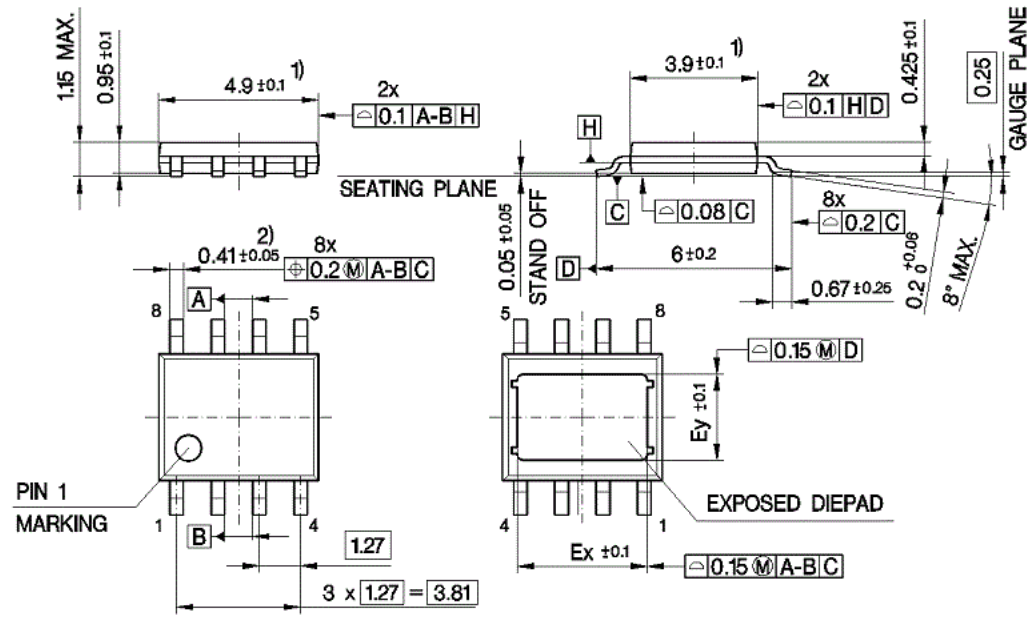


Figure 46 Application example circuitry

Recommended values for V_{IN}= 5 V and V_{DD}= 5 V:
R_{STATUS}=4.7 kΩ
$R_{STATUS(PROT)}$=3.3 kΩ
R_{IN}=3.3 kΩ

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

12 Package Outlines



2) DAMBAR PROTRUSION SHALL BE MAXIMUM 0.1 MM IN EXCESS OF LEAD WIDTH
1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE

EXPOSED DIEPAD AND FOOTPRINT DIMENSIONS					
PACKAGE	LEADFRAME	Ex	Ey	S1	S2
PG-TDSO-8-4	C66065-A6944-C001	3	2.65	0.825	1.35
PG-TDSO-8-43					
PG-TDSO-8-3	C66065-A6944-C002	4	2.65	1.075	1.85
PG-TDSO-8-31					

Figure 47 PG-TDSO8-31

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

13 Revision History

Version	Date	Changes
Rev. 1.0	2016-09-12	Datasheet released

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Do you have a question about any aspect of this document?
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