HI-8450, HI-8451, HI-8454, HI-8455

Single / Quad ARINC 429 Line Receivers with Integrated DO-160G Level 3 Lightning Protection

December 2016

GENERAL DESCRIPTION

Holt's family of ARINC 429 line receivers include internal lightning protection circuitry which ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components. Pin surge levels for Level 3 are summarized below. The HI-8450 and HI-8451 are single ARINC 429 line receivers available in compact 8-pin SOIC packages. The HI-8454 and HI-8455 contain 4 independent ARINC 429 line receivers.

Waveform 3	Waveform 4	Waveform 5A	Waveform 5B
VOC/ISC	VOC/ISC	VOC/ISC	VOC/ISC
600V/24A	300V/60A	300V/300A	300V/300A

The devices are designed to operate from either a 5V or 3.3V supply. Each receiver channel translates incoming ARINC 429 data bus signals to a pair of TTL / CMOS outputs.

The TESTA and TESTB inputs bypass the analog inputs for testing purposes. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the devices are in test mode.

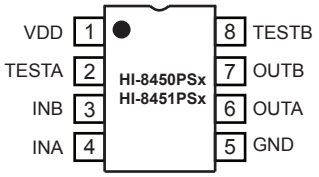
The HI-8451 and HI-8454 produce low outputs when the TESTA and TESTB inputs are held high, whereas the HI-8450 produces high impedance outputs when the TESTA and TESTB inputs are held high. The HI-8455 does not have TEST inputs and these pins may be considered no-connect (NC).

The parts are available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

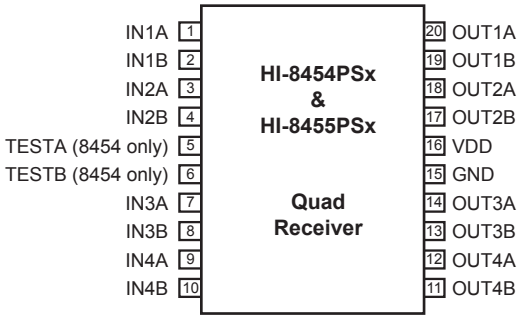
FEATURES

- Internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B)
- Direct connection to ARINC 429 bus with no external components
- 3.3V or 5.0V single supply operation
- Test inputs bypass analog inputs and force digital outputs to a one, zero, or null state (not available on HI-8455)
- Industrial and Extended temperature ranges
- Burn-in available

PIN CONFIGURATION (TOP VIEW)



8-PIN PLASTIC SOIC - NB



20-PIN PLASTIC TSSOP PACKAGE

Table 1. Function Table

ARINC INPUTS INA - INB	TESTA	TESTB	OUTA	OUTB
-2.5 to +2.5V	0	0	0	0
< -6.5V	0	0	0	1
> +6.5V	0	0	1	0
x	0	1	0	1
x	1	0	1	0
x	1	1	0 (1)	0 (1)
x	1	1	HI-Z (2)	HI-Z (2)

Note (1): HI-8451 and HI-8454 only.

Note (2): HI-8450 only.

FUNCTIONAL DESCRIPTION

Figure 1 shows the general architecture of an ARINC 429 receiver. The receiver operates off the VDD supply only. The inputs RINA and RINB may be connected directly to the ARINC 429 bus. Internal lightning protection circuitry ensures compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components.

After level translation, the inputs are buffered and become inputs to a differential amplifier. The amplitude of the differential signal is compared to levels derived from a divider between VDD and Ground. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V.

The status of the ARINC receiver input is latched. A Null input resets the latches and a One or Zero input sets the latches.

The logic at the output is controlled by the test signal which is generated by the logical OR of the TESTA and TESTB pins (not available on HI-8455). If TESTA and TESTB are both One, the outputs are pulled low (HI-8451 and HI-8454 only). This allows the digital outputs of a transmitter to be connected to the test inputs through control logic for system self-test purposes. In the case of HI-8450, if TESTA and TESTB are both One, the outputs are high impedance (HI-Z).

BLOCK DIAGRAMS

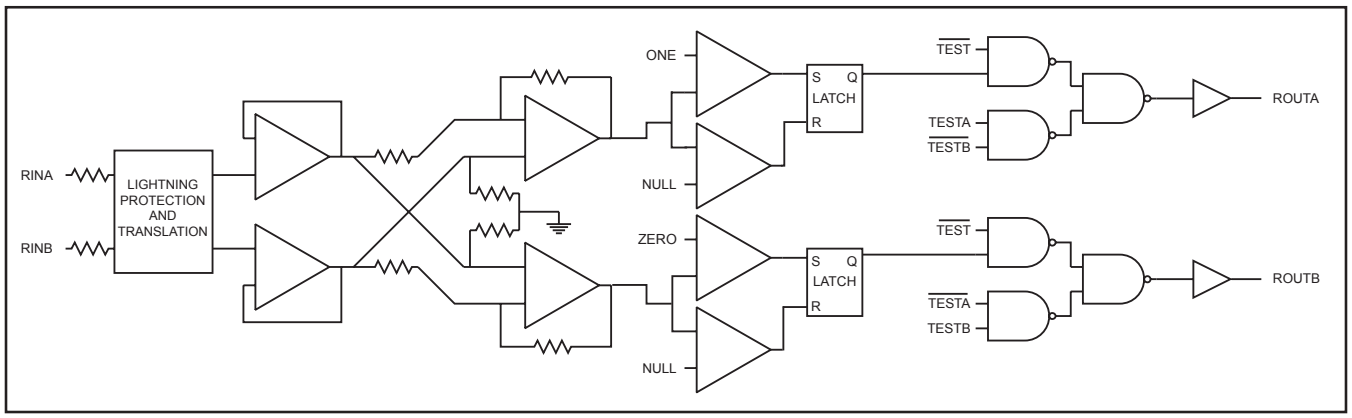


Figure 1. Line Receiver Block Diagram

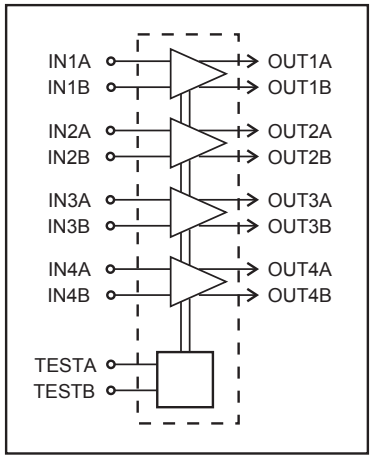


Figure 2. HI-8454 Block Diagram

PIN DESCRIPTIONS

Table 2. Pin Descriptions

Symbol	Function	Description
IN1A	ARINC INPUT	Receiver 1 positive input
IN1B	ARINC INPUT	Receiver 1 negative input
IN2A	ARINC INPUT	Receiver 2 positive input
IN2B	ARINC INPUT	Receiver 2 negative input
TESTA	LOGIC INPUT	Test input (not available on HI-8455)
TESTB	LOGIC INPUT	Test input (not available on HI-8455)
IN3A	ARINC INPUT	Receiver 3 positive input
IN3B	ARINC INPUT	Receiver 3 negative input
IN4A	ARINC INPUT	Receiver 4 positive input
IN4B	ARINC INPUT	Receiver 4 negative input
OUT4B	LOGIC OUTPUT	Receiver 4 “ZERO” output
OUT4A	LOGIC OUTPUT	Receiver 4 “ONE” output
OUT3B	LOGIC OUTPUT	Receiver 3 “ZERO” output
OUT3A	LOGIC OUTPUT	Receiver 3 “ONE” output
GND	POWER	Ground supply voltage
VDD	POWER	+3.3V or +5V supply voltage
OUT2B	LOGIC OUTPUT	Receiver 2 “ZERO” output
OUT2A	LOGIC OUTPUT	Receiver 2 “ONE” output
OUT1B	LOGIC OUTPUT	Receiver 1 “ZERO” output
OUT1A	LOGIC OUTPUT	Receiver 1 “ONE” output

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD})	-0.3V to +7V
Logic input voltage range	-0.3V to +5.5V
ARINC input voltage	-120V to + 120V
Solder Temperature (reflow)	260°C
Storage Temperature	-65°C to +150°C
ESD-HBM (JS-001-2012)	
Logic and supply pins	2,000V
ARINC 429 bus input pins	1,000V

RTCA/DO-160G, Section 22 pin injection	
Waveform	Voc/Isc
3	1,000V/40A
4	500V/100A
5A	500V/500A
5B	500V/500A

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
V_{DD}	3.0V to +5.5V
Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

ELECTRICAL CHARACTERISTICS

Table 3. DC Electrical Characteristics

V_{DD} = +5.0V ± 10% or +3.3V ± 10%, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Units
ARINC INPUTS							
Input Voltage	ONE or ZERO	V_{DIN}	Differential Input voltage	6.5	10	13	V
	NULL	V_{NIN}	Differential Input voltage			2.5	V
	Common mode	V_{COM}	With respect to GND			±5.0	V
Input Resistance	INA to INB	R_{DIFF}	Supplies floating	30			kΩ
	Input to GND or V_{DD}	R_{SUP}	Supplies floating	15			kΩ
Input Hysteresis		V_{HYS}		0.5	1.0		V
Input Capacitance	ARINC differential	C_{AD}			5	10	pF
	ARINC single ended to GND	C_{AS}				10	pF

Parameters		Symbol	Test Conditions	Min	Typ	Max	Units
TEST INPUTS							
Logic Input Voltage	High	V_{IH}		80%V_{DD}			V
	Low	V_{IL}				20%V_{DD}	V
Logic Input Current	Sink	I_{IH}	$V_{IH} = V_{DD}$			200	µA
	Source	I_{IL}	$V_{IL} = 0V$	-1.0			µA
OUTPUTS							
Logic Output Voltage	High	V_{OH}	I_{OH} = -5.0mA, V_{DD} = 5.0V	2.4			V
			I_{OH} = -4.0mA, V_{DD} = 3.3V	2.4			V
	Low	V_{OL}	I_{OH} = 5.0mA, V_{DD} = 5.0V			0.4	V
			I_{OH} = 4.0mA, V_{DD} = 3.3V			0.5	
Logic Output Voltage (CMOS)	High	V_{OHC}	I_{OH} = -100µA	V_{DD}−0.2			V
	Low	V_{OLC}	I_{OL} = 100µA			GND+0.2	V
SUPPLY CURRENT							
V_{DD} Current (HI-8454, HI-8455)		I_{DD}	V_{DD} = 5.0V		14	20	mA
			V_{DD} = 3.3V		9	15	mA
V_{DD} Current (HI-8450, HI-8451)		I_{DD}	V_{DD} = 5.0V		12	18	mA
			V_{DD} = 3.3V		8	14	mA

Table 4. AC Electrical Characteristics

V_{DD} = +5.0V ± 10% or +3.3V ± 10%, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters		Symbol	Test Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS							
Propagation Delay	IN to OUT	t_{LH}	C_L = 50pF		150	300	ns
		t_{HL}	C_L = 50pF		150	300	ns
Output Rise Time		t_R	10% to 90%		15	50	ns
Output Fall Time		t_F	90% to 10%		15	50	ns
Propagation Delay	TEST to OUT	t_{TOH}			50		ns
		t_{TOL}			50		ns

LIGHTNING INDUCED TRANSIENT VOLTAGE WAVEFORMS

Waveform 3.

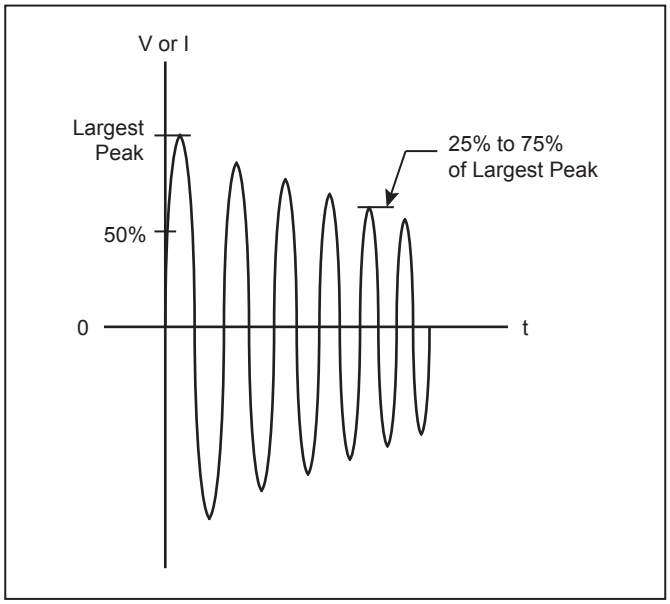


Figure 3. DO-160G Lightning Induced Transient Voltage Waveform 3.
Voc = 600V, Isc = 24A, Frequency = 1MHz ± 20%.

Waveform 4.

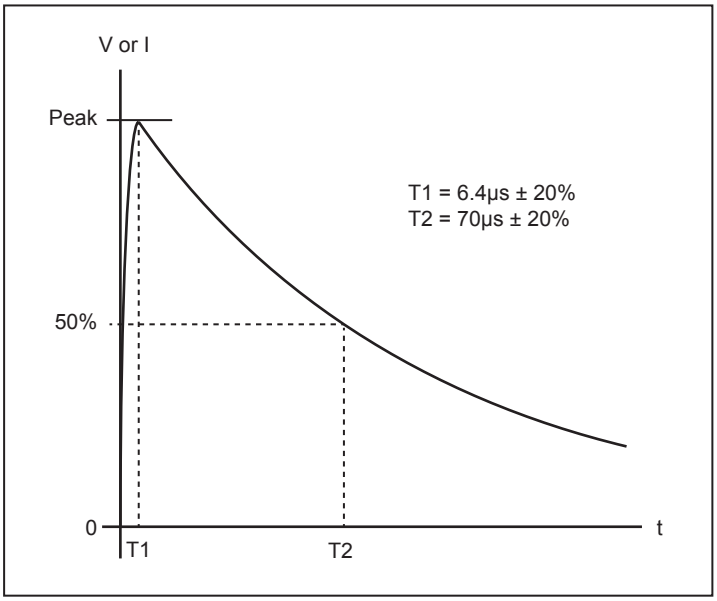


Figure 4. DO-160G Lightning Induced Transient Voltage Waveform 4.
Voc = 300V, Isc = 60A.

Waveform 5.

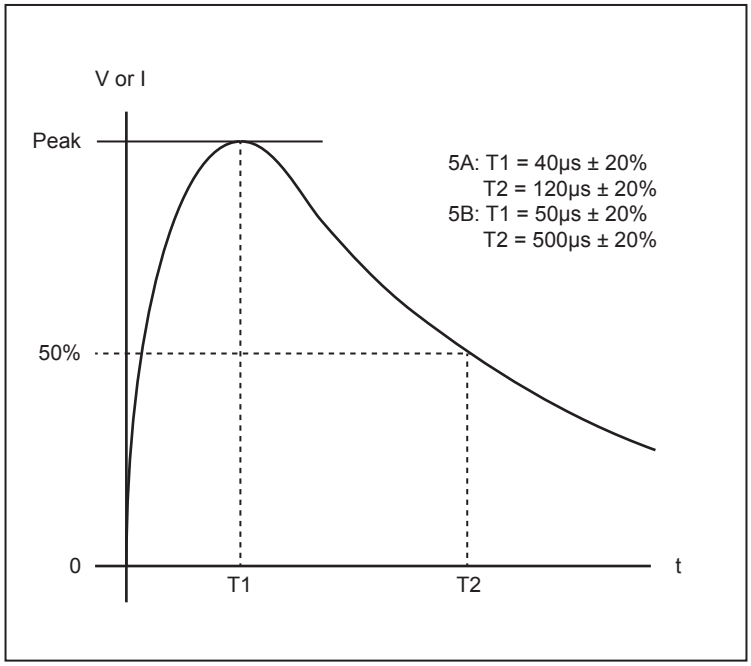
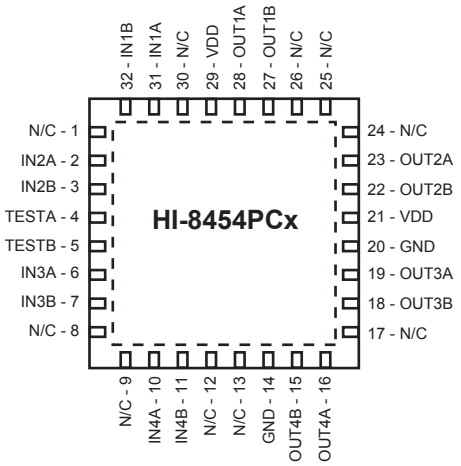


Figure 5. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
Voc = 300V, Isc = 300A.

ADDITIONAL PIN CONFIGURATIONS



32-PIN PLASTIC QFN

ORDERING INFORMATION

HI - 845xxx x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
8450PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
8451PS	8 PIN PLASTIC NARROW BODY SOIC (8HN)
8454PS	20 PIN PLASTIC TSSOP (20HS)
8454PC	32 PIN PLASTIC QFN (32PCS)
8455PS	20 PIN PLASTIC TSSOP (20HS)

REVISION HISTORY

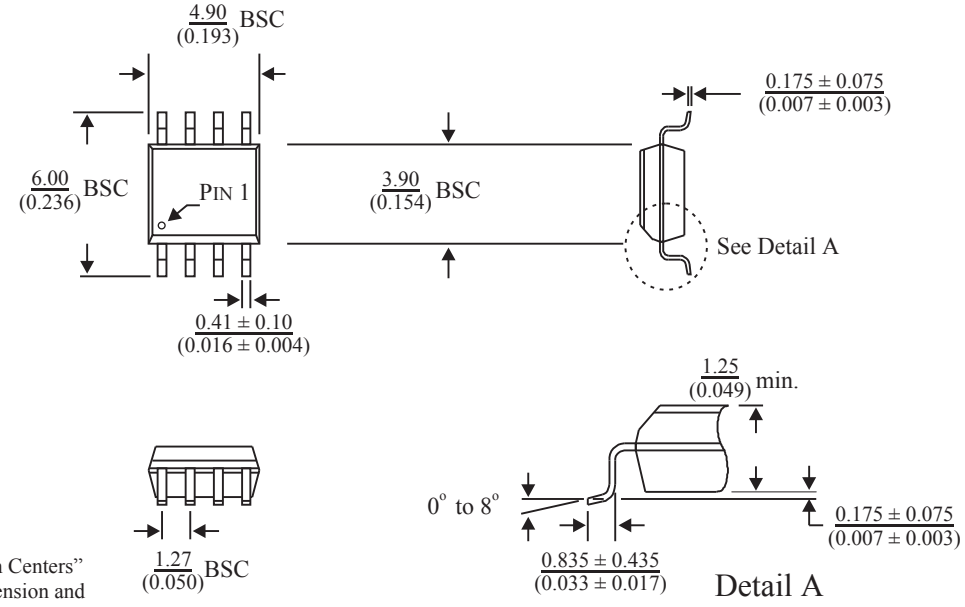
Revision		Date	Description of Change
DS8450,	Rev. New	01/14/14	Initial Release
	Rev. A	12/05/16	Remove Power Dissipation spec from “Absolute Maximum Ratings”.

PACKAGE DIMENSIONS

8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

millimeters (inches)

Package Type: 8HN

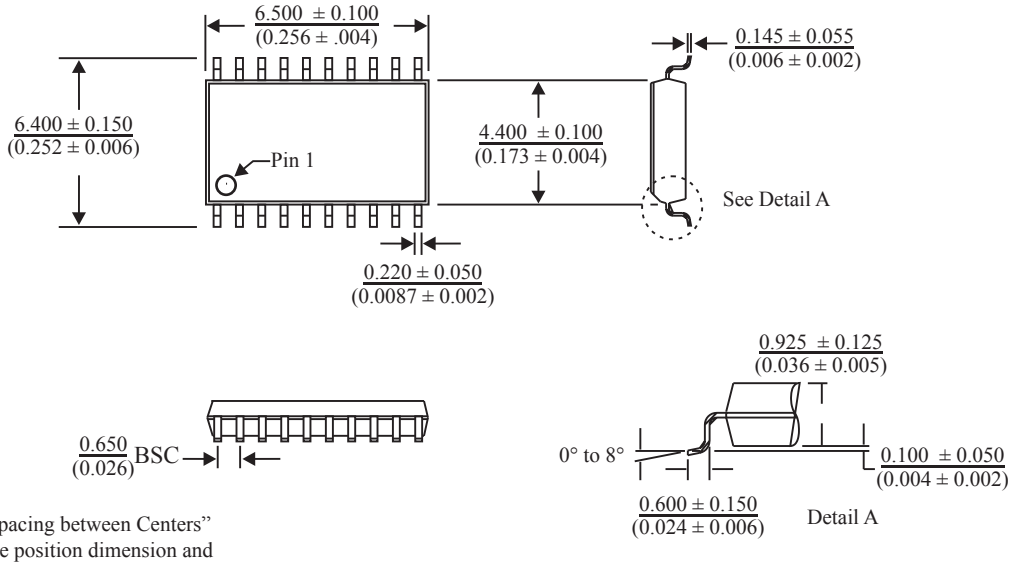


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

20-PIN PLASTIC TSSOP

millimeters (inches)

Package Type: 20HS

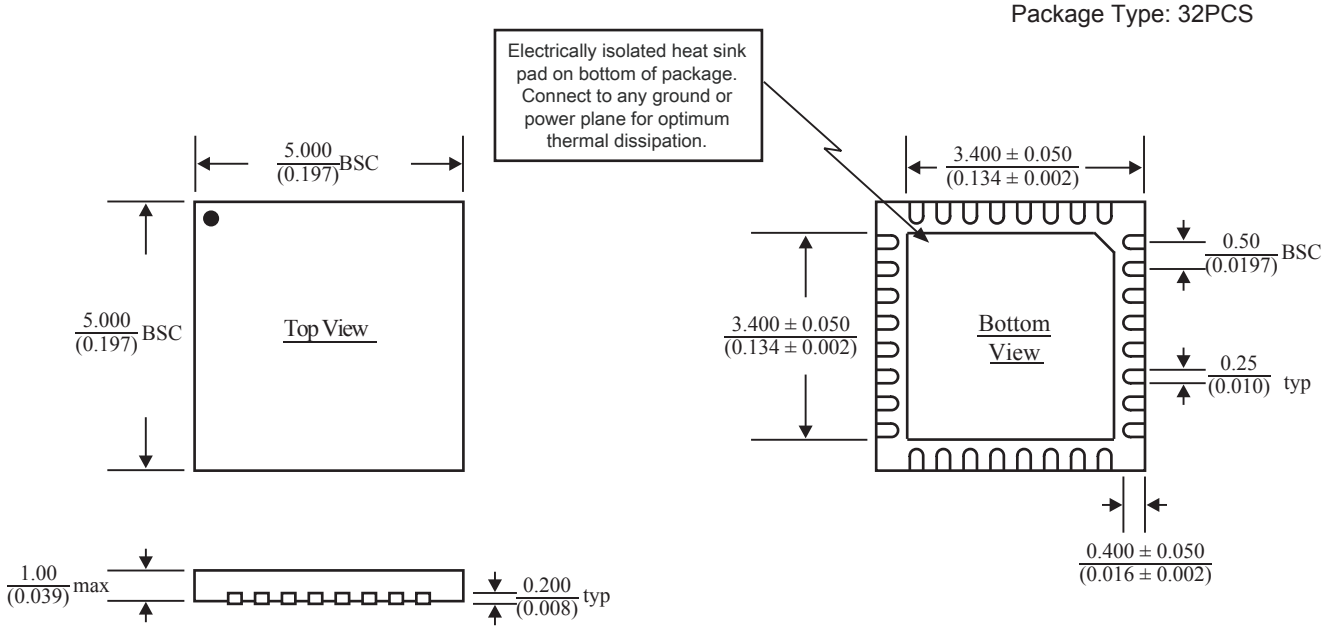


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

32-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 32PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)