

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR720E18	1800	$T_{vj} = -40^{\circ}\text{C}$ to 125°C , $I_{DRM} = I_{RRM} = 30\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR720E16	1600	
DCR720E14	1400	
DCR720E12	1200	

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR720E18

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	1800 V
$I_{T(AV)}$	720 A
I_{TSM}	8300 A
dV/dt^*	1000 V/μs
dI/dt	200 A/μs

* Higher dV/dt selections available

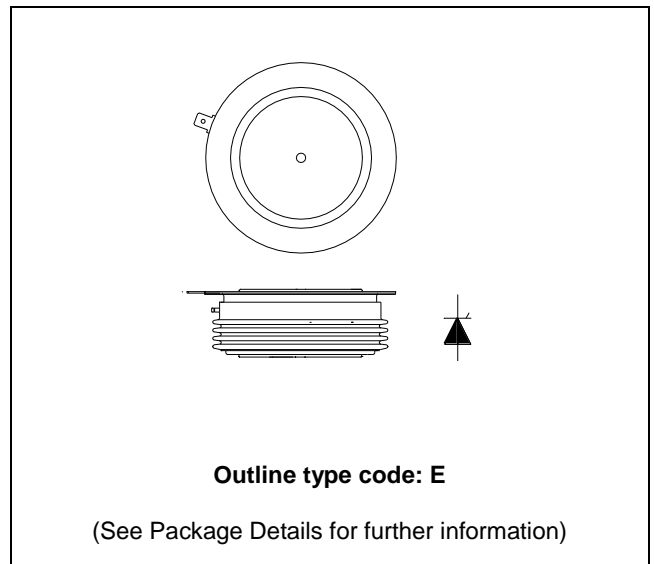


Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
I _{T(AV)}	Mean on-state current	Half wave resistive load	720	A
I _{T(RMS)}	RMS value	-	1220	A
I _T	Continuous (direct) on-state current	-	1100	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125°C	8.3	kA
I ² t	I ² t for fusing	V _R = 0	0.344	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled DC	-	0.041	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Double side cooled DC	-	0.01	°C/W
T _{vj}	Virtual junction temperature	Blocking V _{DRM} / V _{RDM}	-	125	°C
T _{stg}	Storage temperature range		-40	140	°C
F _m	Clamping force		4	6	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	30	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	1000	-	V/ μs	
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1000A Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$	Repetitive 50Hz	-	200	A/ μs
			Non-repetitive	-	1000	A/ μs
V_T	On-state voltage	$I_T = 1500A$, $T_{case} = 125^{\circ}C$		1.97	V	
$V_{T(TO)}$	Threshold voltage – Low level	$T_{case} = 125^{\circ}C$	-	1.09	V	
r_T	On-state slope resistance – Low level	$T_{case} = 125^{\circ}C$	-	0.587	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$	-	3.0	μs	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 100V$, $dl/dt = 10A/\mu s$, $dV_{DR}/dt = 20V/\mu s$ linear to 67% V_{DRM}	-	150	μs	
Q_S	Stored charge	$I_T = 1000A$, $t_p = 1000\mu s$, $T_j = 125^{\circ}C$, $dl/dt = 10A/\mu s$,	-	1500	μC	
I_{RR}	Reverse recovery current		-	110	A	
I_L	Latching current	$T_j = 25^{\circ}C$,	-	1	A	
I_H	Holding current	$T_j = 25^{\circ}C$,	-	200	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V$, $T_{case} = 25^{\circ}C$	3	V
V_{GD}	Gate non-trigger voltage	At 40% V_{DRM} , $T_{case} = 125^{\circ}C$	TBD	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V$, $T_{case} = 25^{\circ}C$	300	mA
I_{GD}	Gate non-trigger current	At 40% V_{DRM} , $T_{case} = 125^{\circ}C$	TBD	mA

CURVES

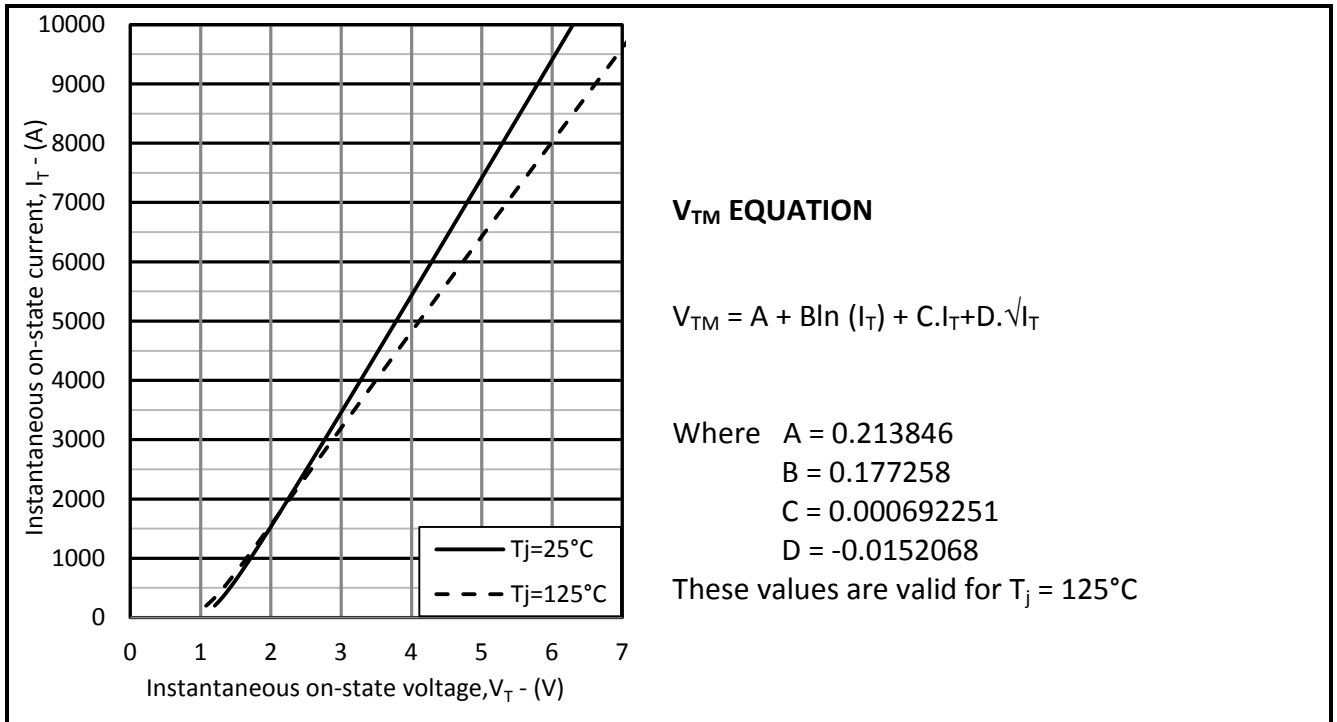


Fig.2 Maximum & minimum on-state characteristics

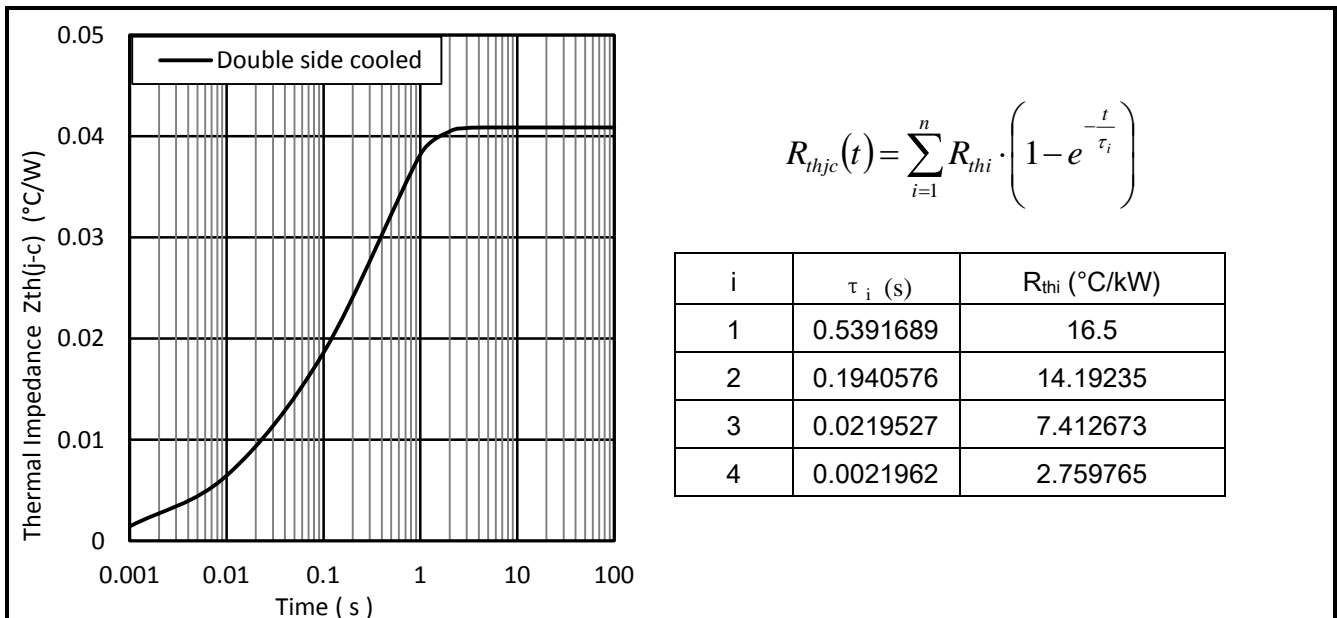


Fig.3 Maximum (limit) transient thermal impedance – junction to case (°C/W)

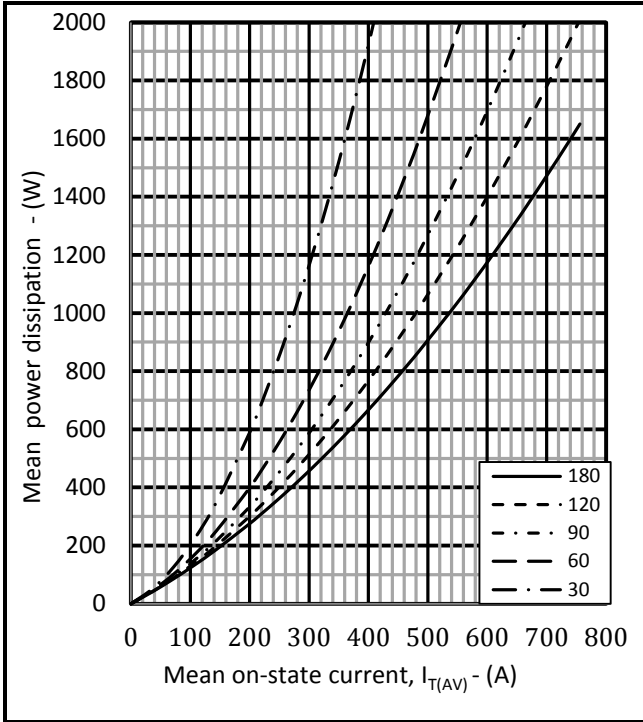


Fig.4 On-state power dissipation – sine wave

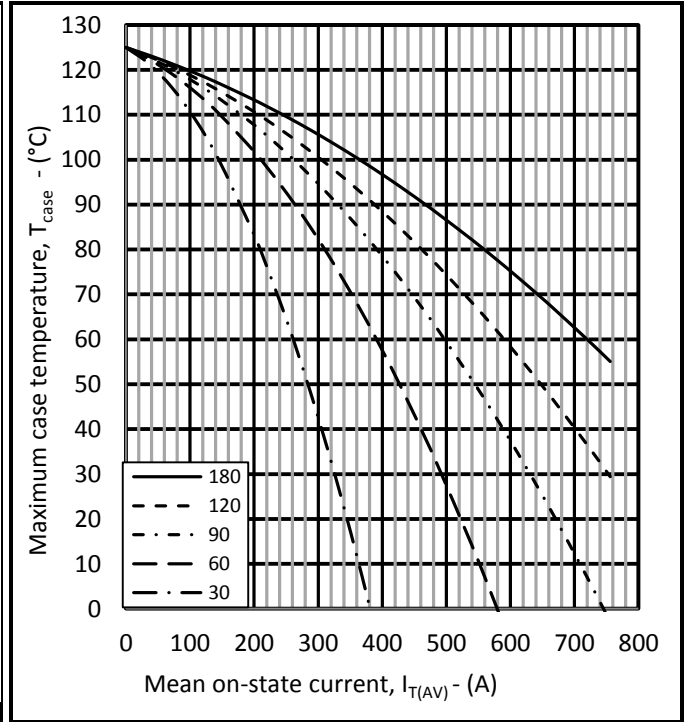


Fig.5 Maximum permissible case temperature, double side cooled – sine wave

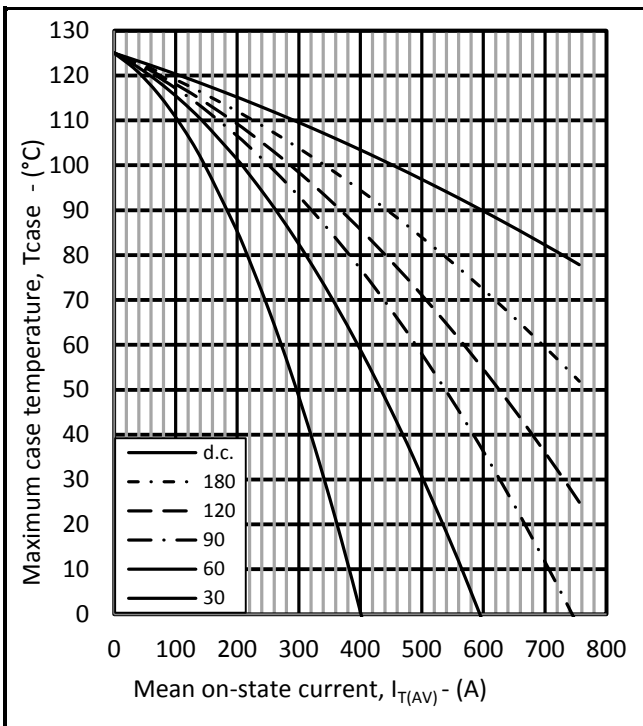


Fig.6 Maximum permissible case temperature, double side cooled – rectangular wave

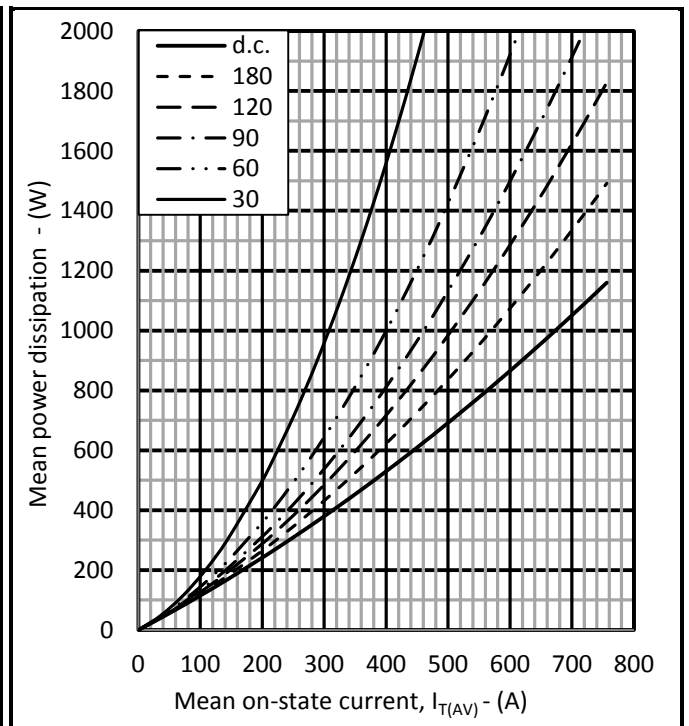


Fig.7 On-state power dissipation – rectangular wave

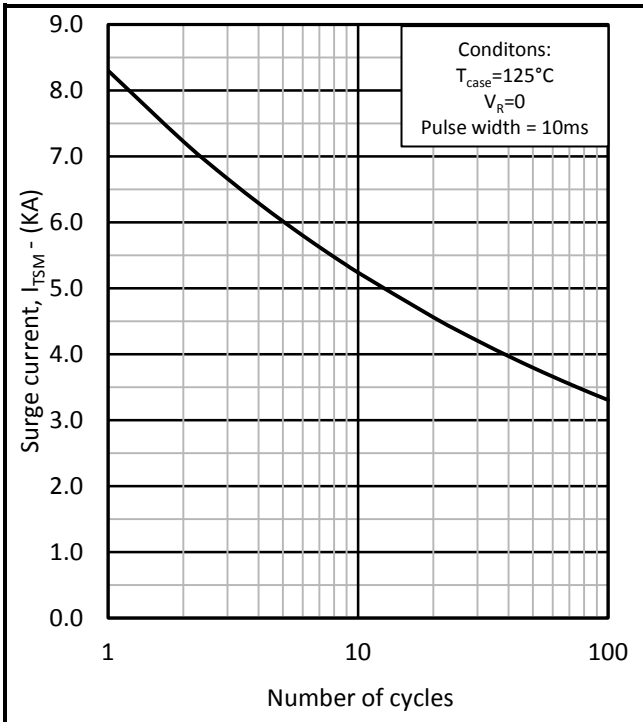


Fig.8 Multi-cycle surge current

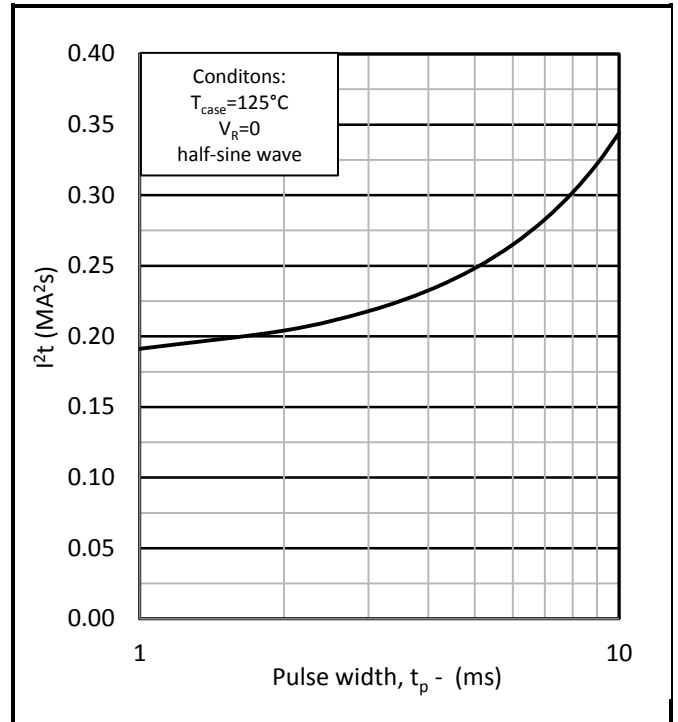


Fig.9 Single-cycle I^2t

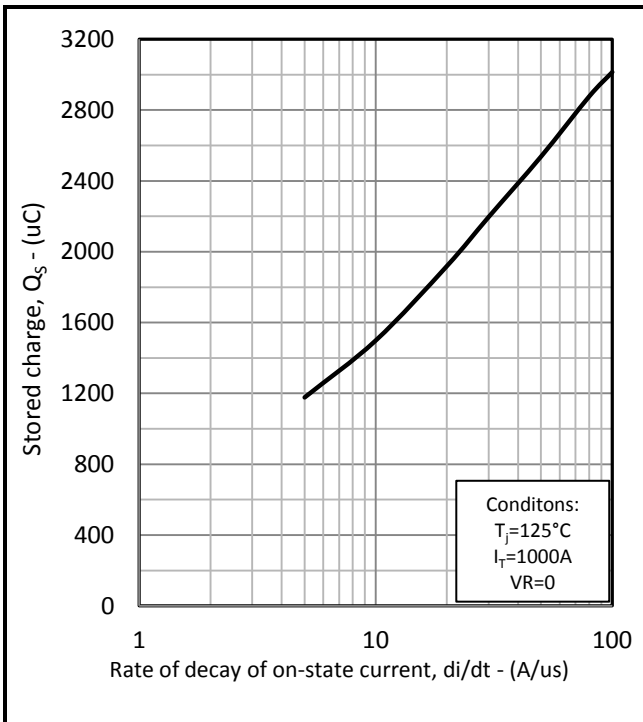


Fig.10 Stored charge vs di/dt

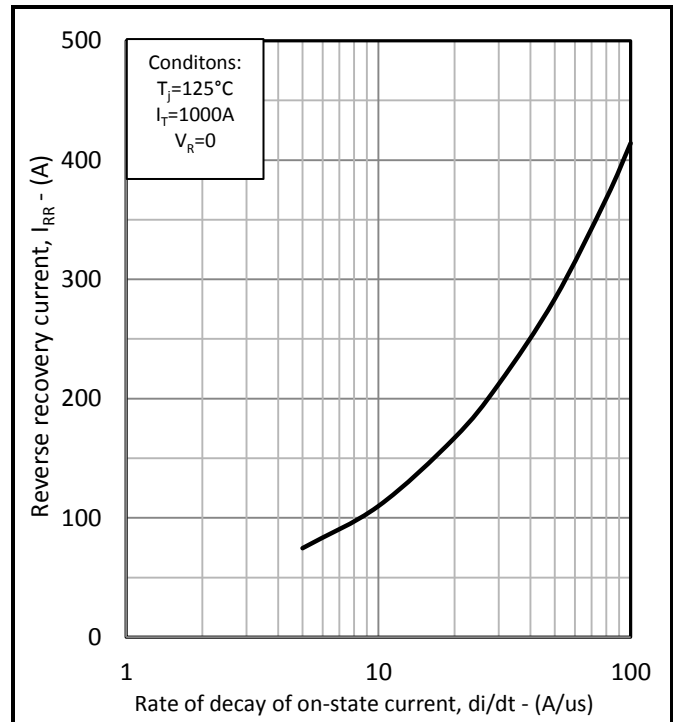


Fig.11 Reverse recovery current vs di/dt

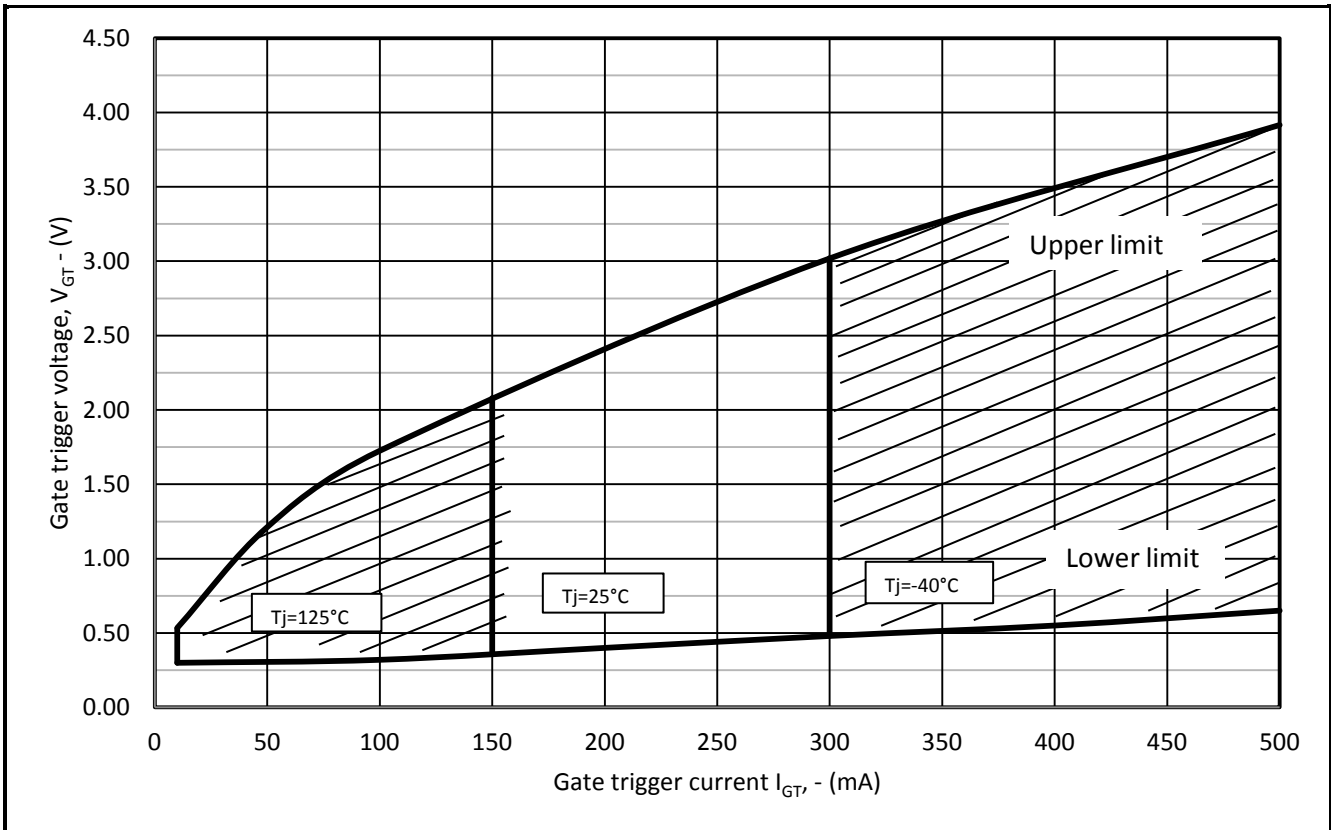
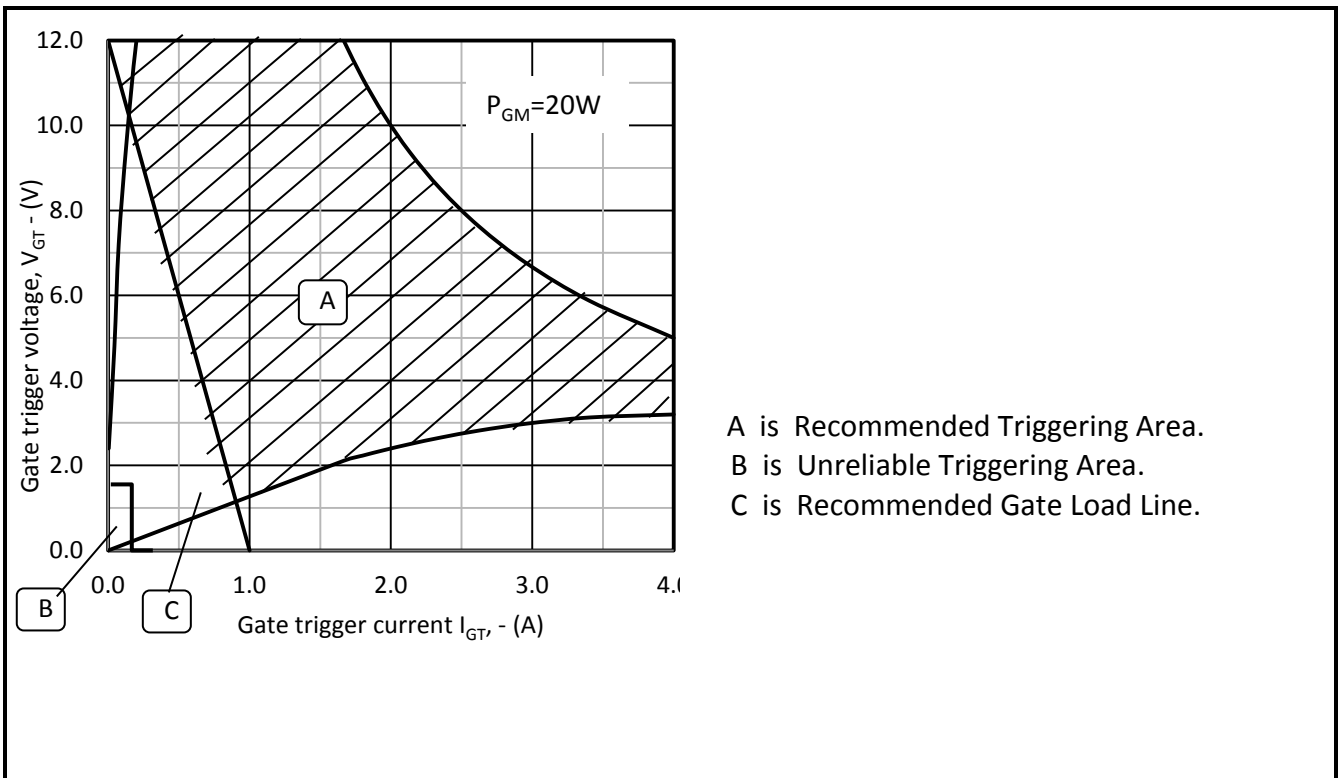


Fig.12 Gate characteristics



A is Recommended Triggering Area.
B is Unreliable Triggering Area.
C is Recommended Gate Load Line.

Fig.13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

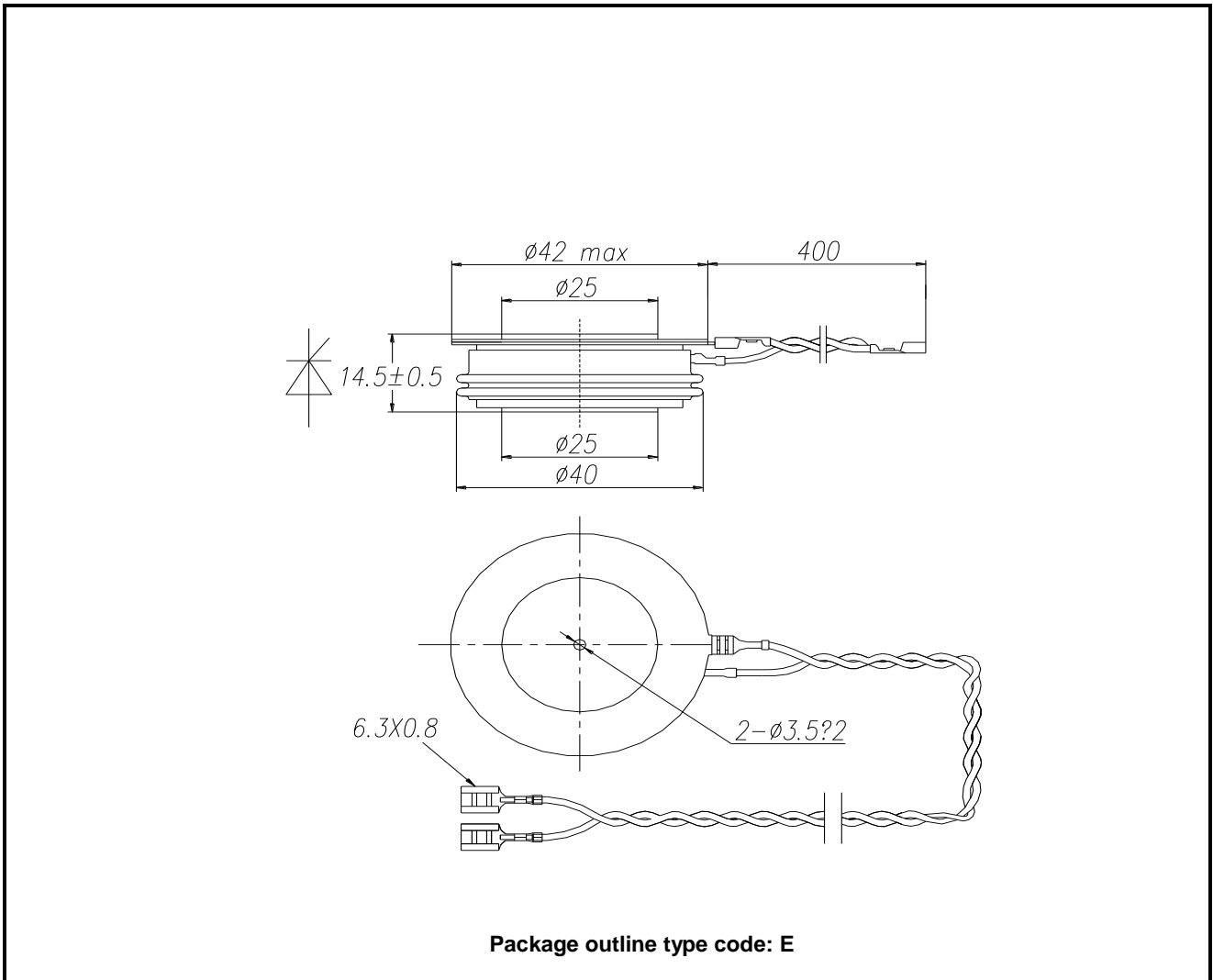


Fig.14 Package outline

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Extended exposure to conditions outside the product ratings may affect reliability leading to premature product failure. Use outside the product ratings is likely to cause permanent damage to the product. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture, a large current to flow or high voltage arcing, resulting in fire or explosion. Appropriate application design and safety precautions should always be followed to protect persons and property.

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Target Information:	This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.
Preliminary Information:	The product design is complete and final characterisation for volume production is in progress. The datasheet represents the product as it is now understood but details may change.
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