0.7V to V_{CC}-1V, 3A 1ch Ultra-Low Dropout Linear Regulator

BD3512MUV

General Description

BD3512MUV is an ultra-low dropout linear chipset regulator, which operates at a very low input supply. It offers ideal performance in low input to output voltage applications. The input-to-output voltage difference is minimized by using a built-in N-Channel power MOSFET with a maximum ON-Resistance of R_{ON}=100mΩ. By lowering the dropout voltage, the regulator achieves high output current of up to I_{OUTMAX}=3.0A, thereby, reducing conversion loss, making it comparable to a switching regulator and its power transistor, choke coil, and rectifier diode constituents. It is a low-cost design and is available in significantly downsized package profiles. An external resistor sets the output voltage which ranges from 0.65V to 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to anything the power supply sequence is required.

Features

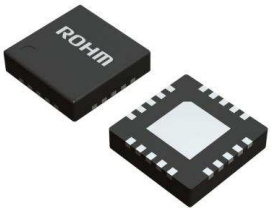
- Incorporates High-Precision Reference Voltage Circuit (0.65V±1%)
- Built-in VCC Undervoltage Lockout Circuit (V_{CC}=3.80V)
- NRCS (Soft-start) Function Reduces the Magnitude of In-rush Current
- Built-in N-Channel MOSFET
- Built-in Current Limit Circuit (3.0A min)
- Built-in Thermal Shutdown (TSD) Circuit (Timer latch)
- Tracking Function

Key Specifications

- IN Input Voltage Range: 0.7V to V_{CC}-1V
- VCC Input Voltage Range: 4.3V to 5.5V
- Output Voltage Range: 0.65V to 2.7V
- Output Current: 3.0A (Max)
- ON-Resistance: 65mΩ(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature: -10°C to +100°C

Package

W(Typ) x D(Typ) x H(Max)

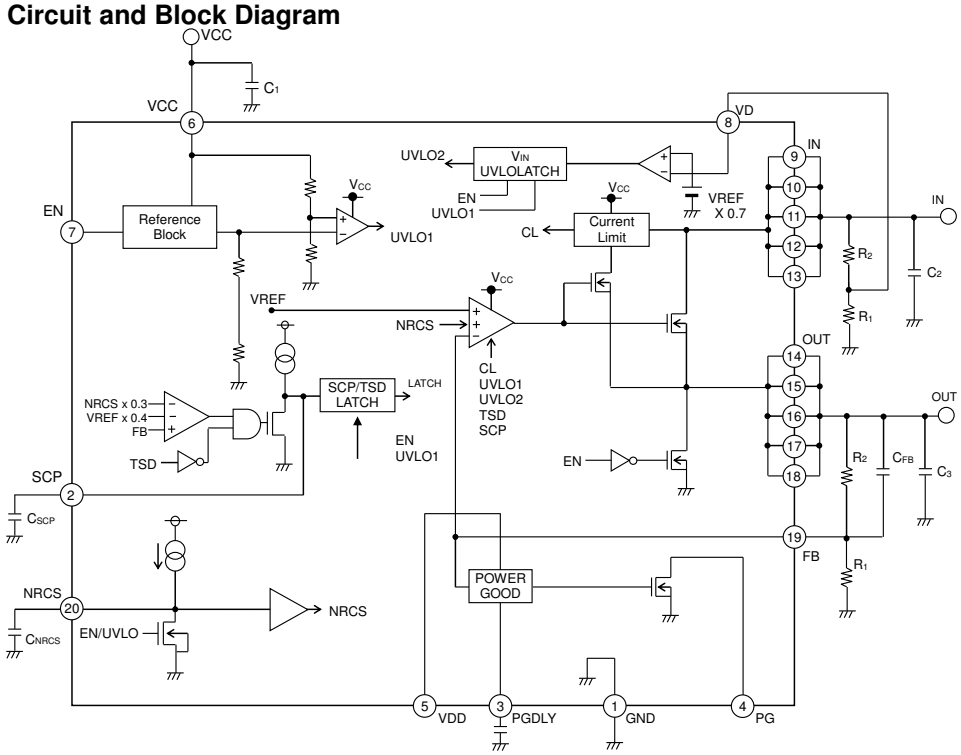


VQFN020V4040
4.00mm x 4.00mm x 1.00mm

Applications

Notebook and Desktop computers, LCD-TV, DVD, Digital appliances

Typical Application Circuit and Block Diagram



○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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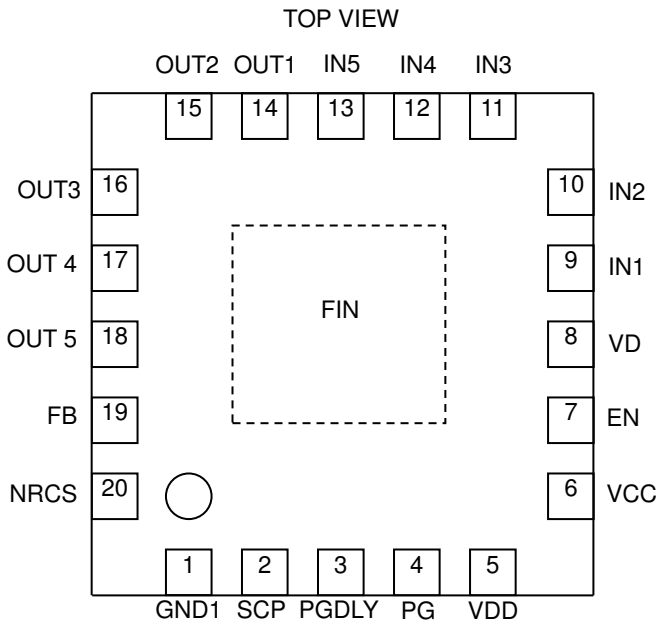
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	PIN Function
1	GND1	Ground pin 1
2	SCP	SCP delay time setting capacitor connection pin
3	PGDLY	PGOOD delay setting capacitor connection pin
4	PG	Power good pin
5	VDD	Power supply pin
6	VCC	Power supply pin
7	EN	Enable input pin
8	VD	IN input voltage detect pin
9	IN1	Input voltage pin 1
10	IN2	Input voltage pin 2
11	IN3	Input voltage pin 3
12	IN4	Input voltage pin 4
13	IN5	Input voltage pin 5
14	OUT1	Output voltage pin 1
15	OUT 2	Output voltage pin 2
16	OUT 3	Output voltage pin 3
17	OUT 4	Output voltage pin 4
18	OUT 5	Output voltage pin 5
19	FB	Reference voltage feedback pin
20	NRCS	In-rush current protection (NRCS) capacitor connection pin
bottom	FIN	Connected to heat sink and GND

(Note) Please short N.C to the GND line.

Description of Blocks

1. AMP
   This is an error amplifier, which compares the reference voltage (0.65V) to FB voltage to drive the output N-Channel FET. Frequency optimization aids in attaining rapid transient response, and to support the use of ceramic capacitors on the output. AMP output voltage ranges from GND to VCC. When EN is OFF, or when UVLO is active, output goes LOW and the output of the N-Channel FET switches to OFF state.

2. EN
   The EN block controls the ON and OFF state of the regulator via the EN logic input pin. During OFF state, circuit voltage stabilizes at 0μA which minimizes the current consumption during standby mode. The FET is switched ON to enable the discharge of NRCS and OUT, thereby draining the excess charge and preventing the load side of an IC from malfunctioning. Since there is no electrical connection required (e.g. between the VCC pin and the ESD prevention diode), module operation is independent of the input sequence.

3. UVLO
   To prevent malfunctions that can occur during sudden decrease in VCC, the UVLO circuit switches the output to OFF state, and (like the EN block) discharges NRCS and OUT. Once the UVLO threshold voltage (TYP3.80V) is reached, the power-ON reset is triggered and the output is restored.

4. CURRENT LIMIT
   During ON state, it monitors the output current of the IC against the current limit value. When the output current exceeds this value, this block lowers the output current to protect the load of the IC. When it overcomes the overcurrent state, output voltage is restored to allowable value.

5. NRCS (Non Rush Current on Start-up)
   The soft start function is enabled by connecting an external capacitor between the NRCS pin and ground. Output ramp-up can be set to any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a constant current source about 20μA (TYP) to charge the external capacitor. Capacitors with low susceptibility (0.001μF to 1μF) to temperature are recommended, in order to assure a stable soft-start time.

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Description of Blocks –continued

6. TSD (Thermal Shut down)
   The shutdown (TSD) circuit is automatically latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus protecting the IC against “thermal runaway” and heat damage. Since the TSD circuit is designed only to shut down the IC in the occurrence of extreme heat, it is important that the Tj(max) parameter should not be exceeded in the thermal design, in order to avoid potential problems with the TSD.

7. IN
   The IN line acts as the major current supply line, and is connected to the output N-Channel FET drain. Since there is no electrical connection (such as between the VCC pin and the ESD protection diode) required, IN operates independent of the input sequence. However, since an output N-Channel FET body diode exists between IN and OUT, a V_{IN}-V_{OUT} electric (diode) connection is present. Therefore, when output is switched ON or OFF, reverse current may flow from OUT to IN.

8. PGOOD
   It determines the status of the output voltage. This is an open-drain pin, which is connected to VCC pin through the pull-up resistance (100kΩ or so). When the output voltage ranges from V_{OUT} x 0.9 to V_{OUT} x 1.1(TYP), the status is high.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Input Voltage 1	V_{CC}	6.0 (Note 1)	V
Input Voltage 2	V_{IN}	6.0 (Note 1)	V
Input Voltage 3	V_{DD}	6.0 (Note 1)	V
Input Voltage 4	V_{VD}	1	V
Maximum Output Current	I_{OUT}	3 (Note 1)	A
Enable Input Voltage	V_{EN}	6.0	V
PGOOD Input Voltage	V_{PGOOD}	6.0	V
Power Dissipation 1	Pd1	0.34 (Note 2)	W
Power Dissipation 2	Pd2	0.70 (Note 3)	W
Power Dissipation 3	Pd3	2.21 (Note 4)	W
Power Dissipation 4	Pd4	3.56 (Note 5)	W
Operating Temperature Range	Topr	-10 to +100	°C
Storage Temperature Range	Tstg	-55 to +125	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Should not exceed Pd.
(Note 2) Derating in done 2.7mV/°C for operating above Ta ≥ 25°C no heat sink
(Note 3) Derating in done 5.6mV/°C for operating above Ta ≥ 25°C
PCB size:74.2mm x 74.2mm x 1.6mm when mounted on a 1-layer glass epoxy board(copper foil area : 10.29mm^2)
(Note 4) Derating in done 17.7mV/°C for operating above Ta ≥ 25°C
PCB size:74.2mm x 74.2mm x 1.6mm when mounted on a 4-layer glass epoxy board(copper foil area : front and reverse 10.29mm^2 , 2nd and 3rd 5505mm^2)
(Note 5) Derating in done 28.5mV/°C for operating above Ta ≥ 25°C
PCB size:74.2mm x 74.2mm x 1.6mm when mounted on a 4-layer glass epoxy board(copper foil area : each 5505mm^2)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min	Max	Unit
Input Voltage 1	V_{CC}	4.3	5.5	V
Input Voltage 2	V_{IN}	0.7	V_{CC}-1 (Note 6)	V
Input Voltage 3	V_{DD}	4.5	5.5	V
Output Voltage Setting Range	V_{OUT}	V_{FB}	2.7	V
Enable Input Voltage	V_{EN}	-0.3	+5.5	V

(Note 6) VCC and IN do not have to be implemented in the order listed.

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Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=5V, V_{EN}=3V, V_{IN}=1.7V, R_1=3.9kΩ, R_2=3.3kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	-	1.4	2.2	mA	
VCC Shutdown Mode Current	I_{ST}	-	0	10	μA	V_{EN}=0V
Maximum Output Current	I_{OUT}	3.0	-	-	A	
Output Voltage Temperature Coefficient	Tcvo	-	0.01	-	%/°C	
Feedback Voltage 1	V_{FB1}	0.643	0.650	0.657	V	
Feedback Voltage 2	V_{FB2}	0.637	0.650	0.663	V	I_{OUT}=0A to 3A Tj=-10°C to +100°C
Line Regulation 1	Reg.l1	-	0.1	0.5	%/V	V_{CC}=4.3V to 5.5V
Line Regulation 2	Reg.l2	-	0.1	0.5	%/V	V_{IN}=1.5V to 3.3V
Load Regulation	Reg.L	-	0.5	10	mV	I_{OUT}=0A to 3A
Minimum dropout voltage	dVo	-	65	100	mV	I_{OUT}=1A,V_{IN}=1.2V
Standby Discharge Current	I_{DEN}	1	-	-	mA	V_{EN}=0V, V_{OUT}=1V
[ENABLE]						
Enable Pin Input Voltage High	V_{ENHI}	2	-	-	V	
Enable Pin Input Voltage Low	V_{ENLOW}	-0.2	-	+0.8	V	
Enable Input Bias Current	I_{EN}	-	6	10	μA	V_{EN}=3V
[FEEDBACK]						
Feedback Pin Bias Current	I_{FB}	-100	0	+100	nA	
[NRCS]						
NRCS Charge Current	I_{NRCS}	14	20	26	μA	V_{NRCS}=0.5V
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	V_{CCUVLO}	3.5	3.8	4.1	V	VCC: Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	V_{CCHYS}	100	160	220	mV	VCC: Sweep-down
VD Undervoltage Lockout Threshold Voltage	V_{DUVLO}	V_{REF} x 0.6	V_{REF} x 0.7	V_{REF} x 0.8	V	VD: Sweep-up
[SCP]						
SCP Startup Voltage	V_{OUTSCP}	V_{OUT} x 0.3	V_{OUT} x 0.4	V_{OUT} x 0.5	V	
SCP Threshold Voltage	V_{SCPTH}	1.05	1.15	1.25	V	
SCP Charge Current	I_{SCP}	1.4	2	2.6	μA	
SCP Standby Voltage	$V_{SCPSTBY}$	-	-	50	mV	
[PGOOD]						
Low-side Threshold Voltage	V_{THPGL}	V_{OUT} x 0.87	V_{OUT} x 0.9	V_{OUT} x 0.93	V	
High-side Threshold Voltage	V_{THPGH}	V_{OUT} x 1.07	V_{OUT} x 1.1	V_{OUT} x 1.13	V	
PGDLY Charge Current	I_{PGDLY}	1.4	2.0	2.6	μA	(Note)
Ron	R_{PG}	-	0.1	-	kΩ	

(Note) PGOOD delay time is determined using the formula below:

$$t_{PGDLY} = \frac{C(pF) \times 1.23}{I_{PGDLY}(\mu A)} (\mu sec)$$

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Typical Waveforms

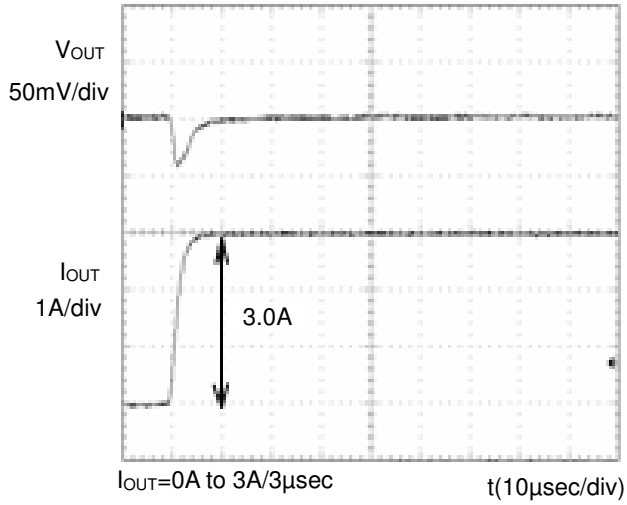

Figure 1. Transient Response
(0A to 3A)
C_{OUT}=22µF, C_{FB}=1000pF

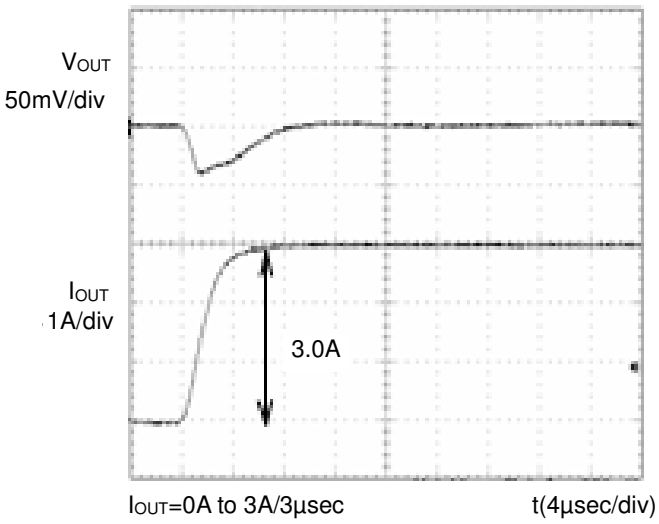

Figure 2. Transient Response
(0A to 3A)
C_{OUT}=100µF

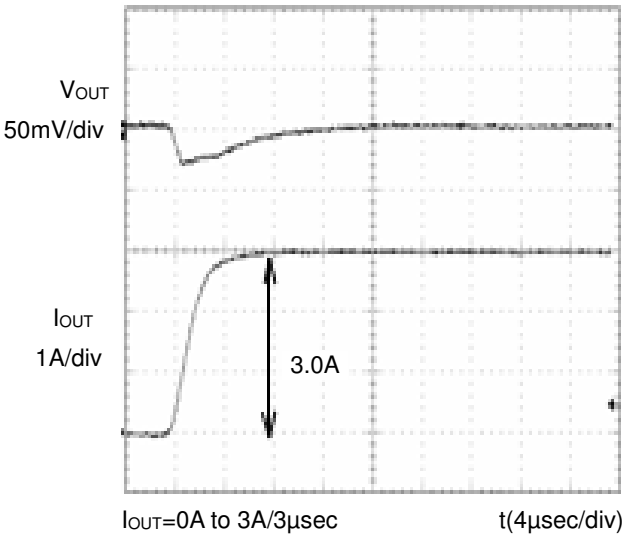

Figure 3. Transient Response
(0A to 3A)
C_{OUT}=100µF, C_{FB}=1000pF

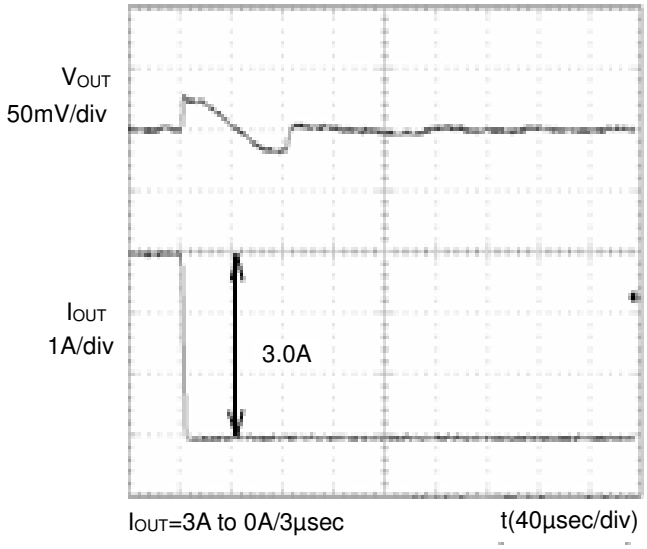

Figure 4. Transient Response
(3A to 0A)
C_{OUT}=22µF, C_{FB}=1000pF

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Typical Waveforms – continued

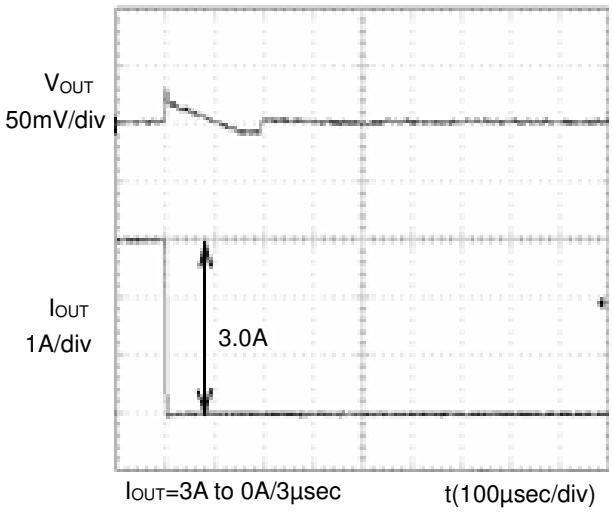

Figure 5. Transient Response
(3A to 0A)
C_{OUT}=100µF

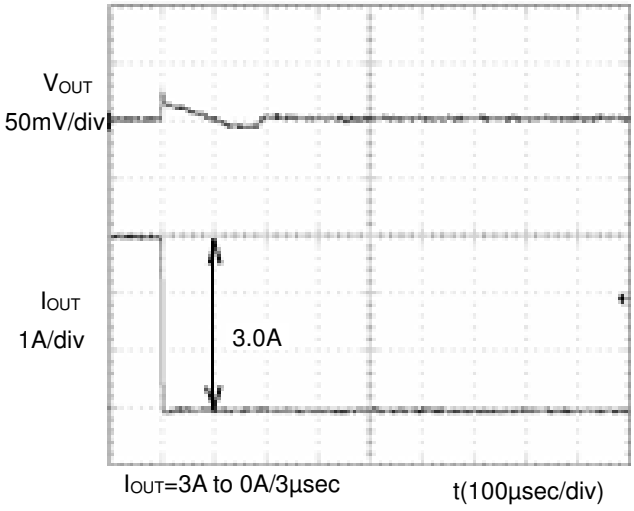

Figure 6. Transient Response
(3A to 0A)
C_{OUT}=100µF, C_{FB}=1000pF

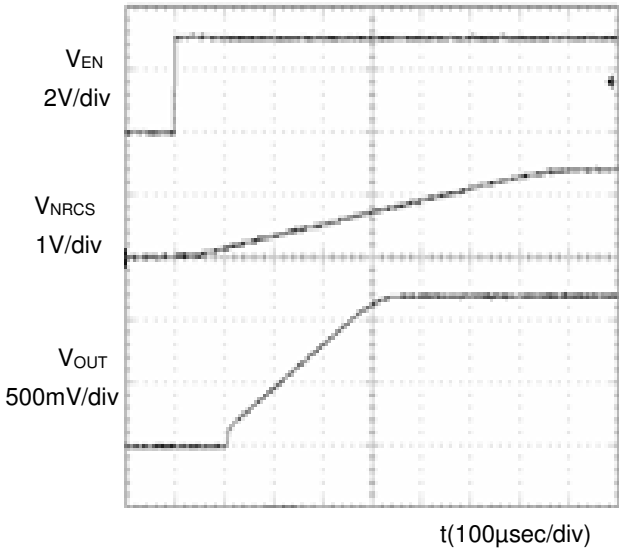

Figure 7. Waveform at Output Start

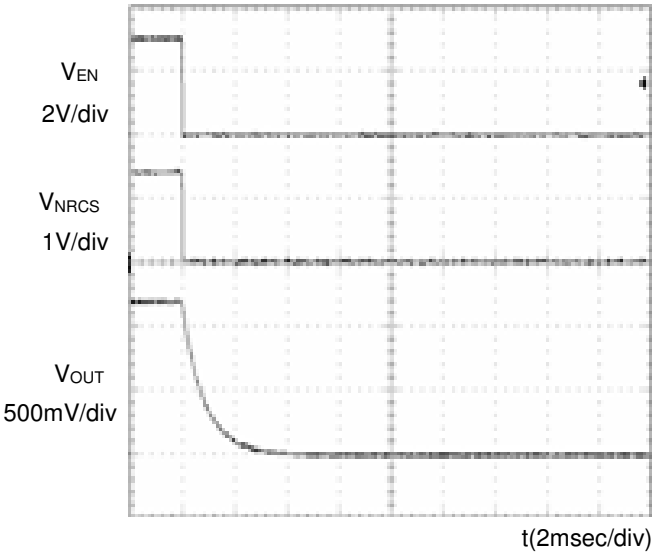

Figure 8. Waveform at Output OFF

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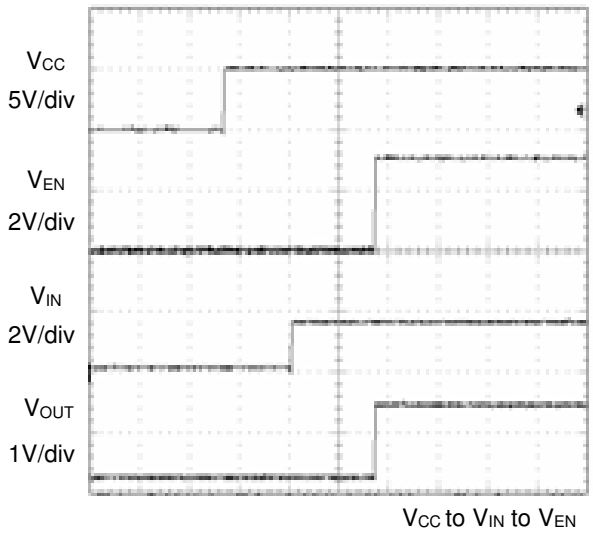

Figure 9. Input Sequence

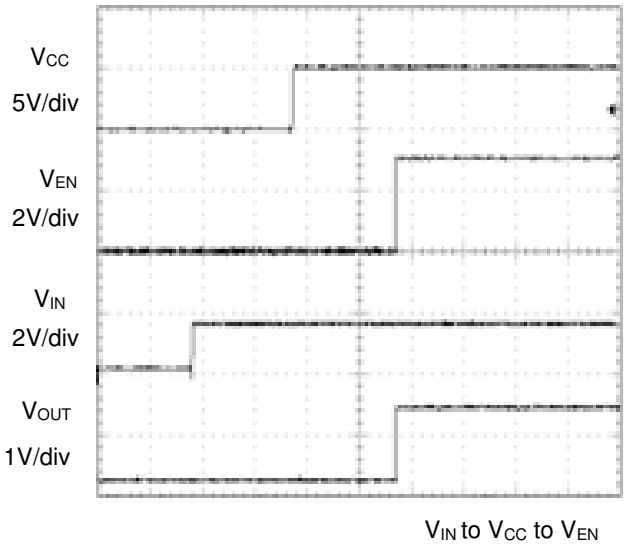

Figure 10. Input Sequence

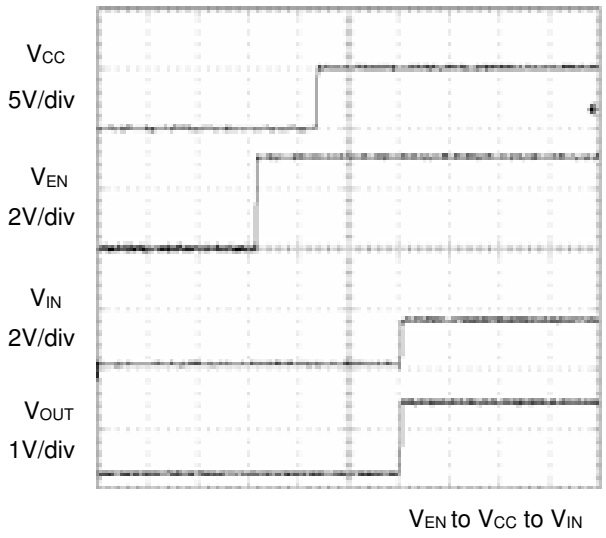

Figure 11. Input Sequence

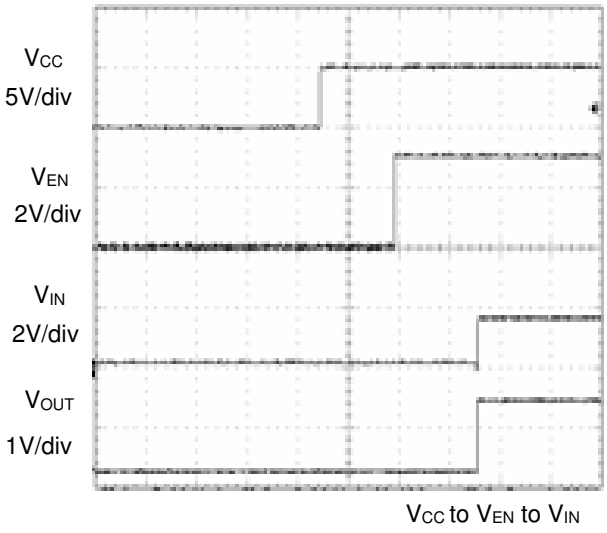

Figure 12. Input Sequence

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Typical Waveforms – continued

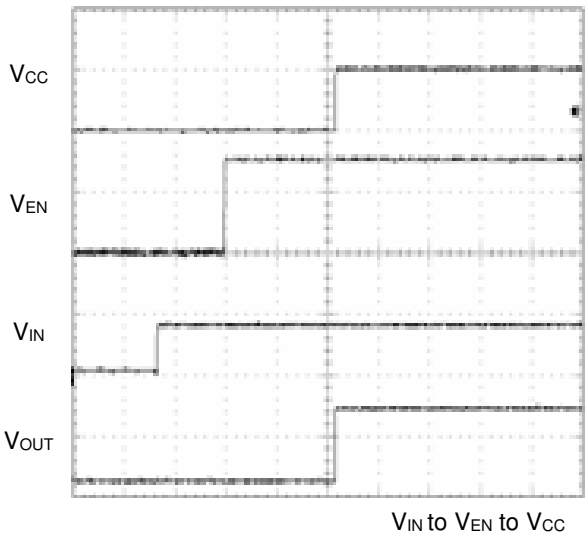

Figure 13. Input Sequence

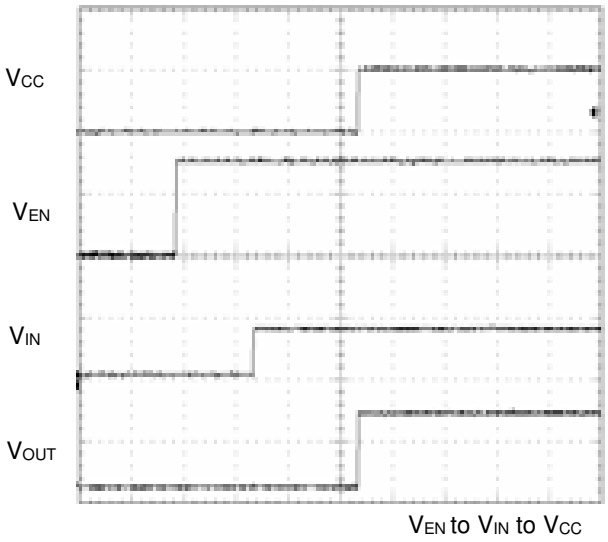

Figure 14. Input Sequence

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Typical Performance Curves

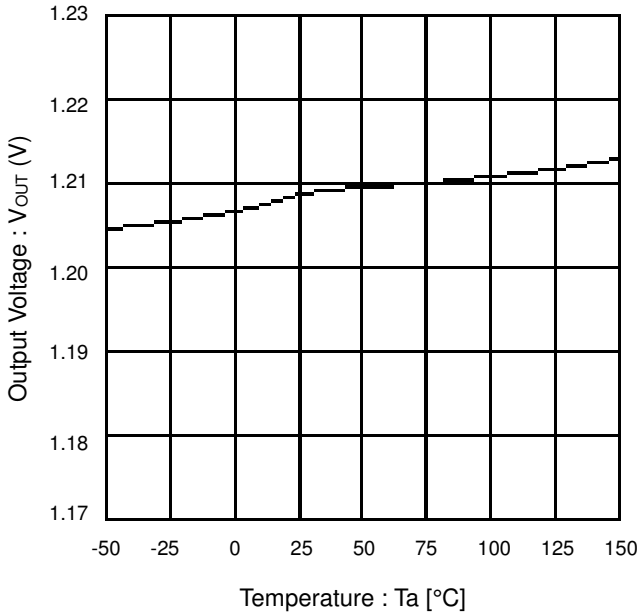

Figure 15. Output Voltage vs Temperature

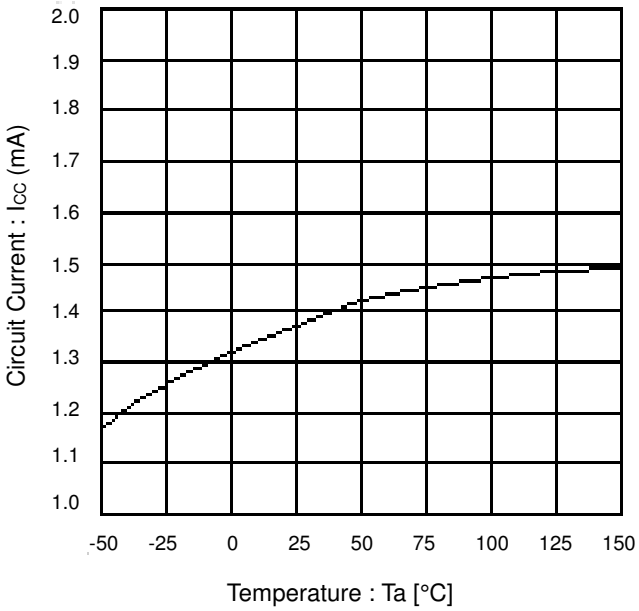

Figure 16. Circuit Current vs Temperature

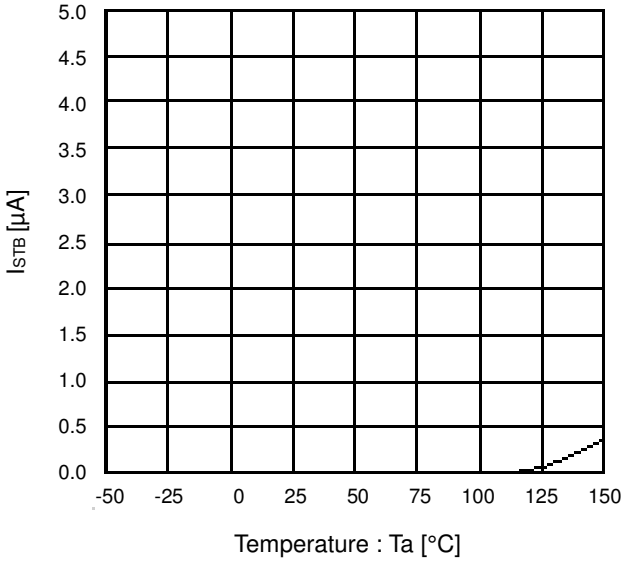

Figure 17. I_{STB} vs Temperature

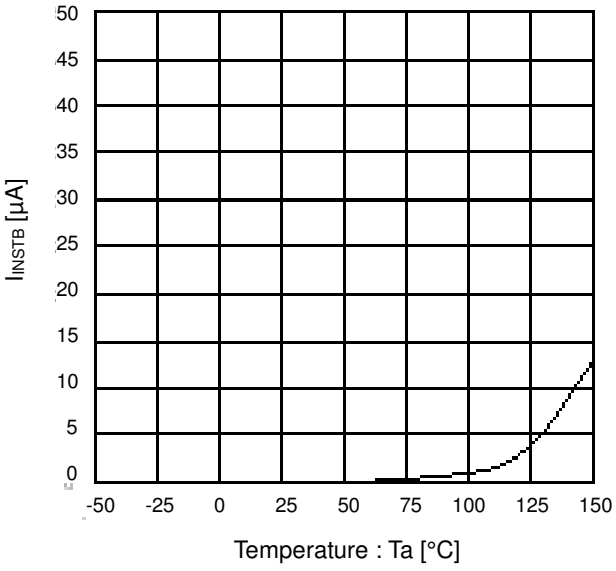

Figure 18. I_{INSTB} vs Temperature

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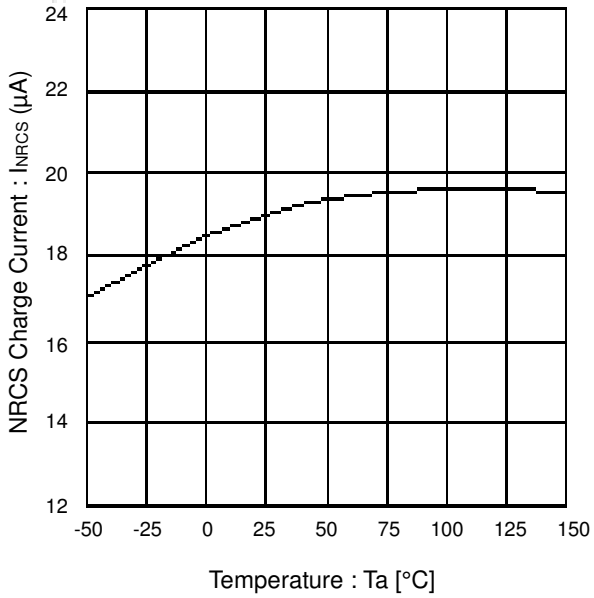

Figure 19. NRCS Charge Current vs Temperature

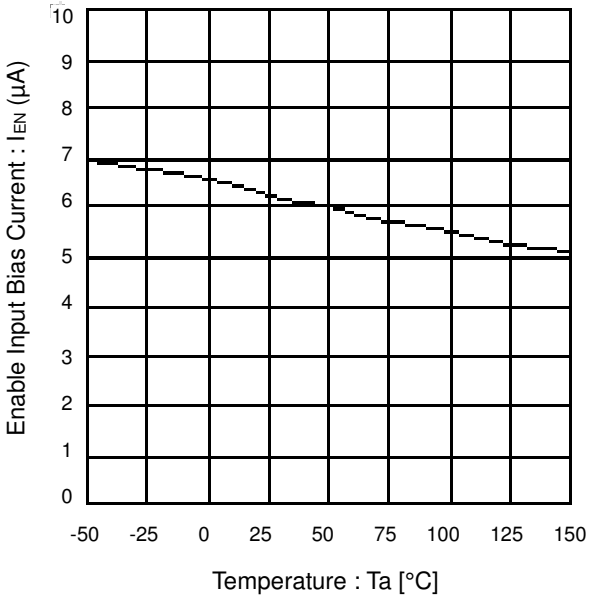

Figure 20. Enable Input Bias Current vs Temperature

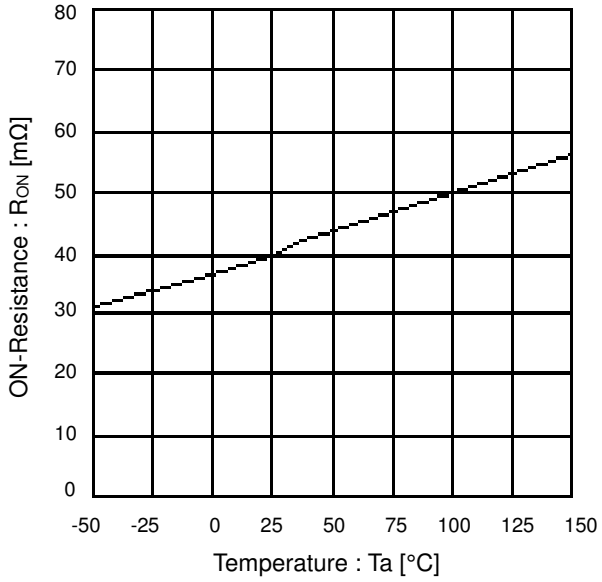

Figure 21. ON-Resistance vs Temperature
(V_{CC}=5V/V_{OUT}=1.2V)

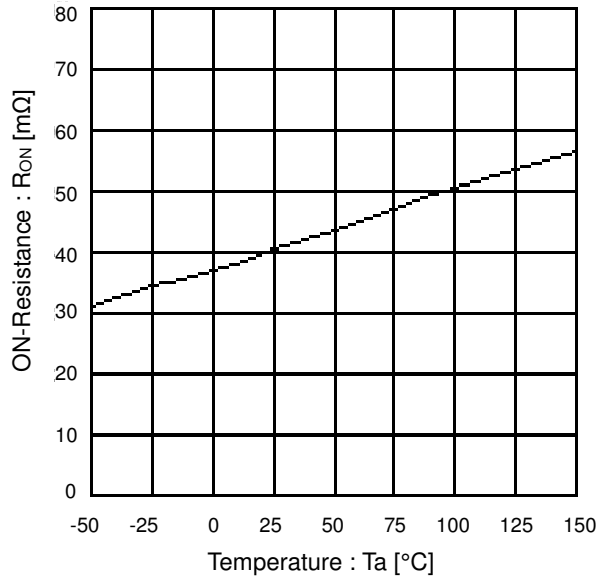

Figure 22. ON-Resistance vs Temperature
(V_{CC}=5V/V_{OUT}=1.5V)

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Typical Performance Curves – continued

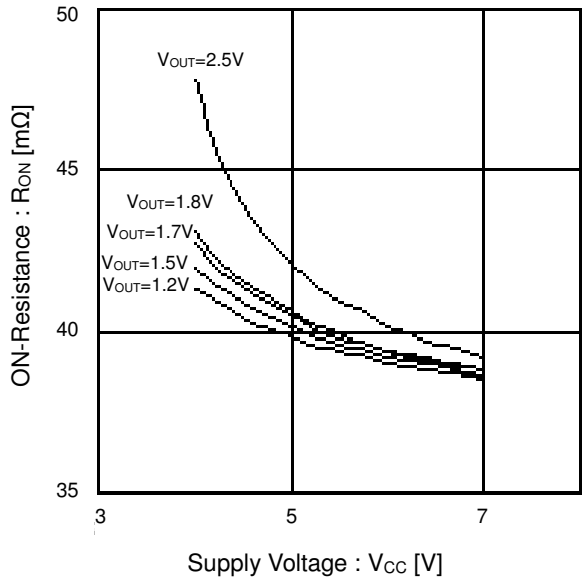

Figure 23. ON-Resistance vs Supply Voltage

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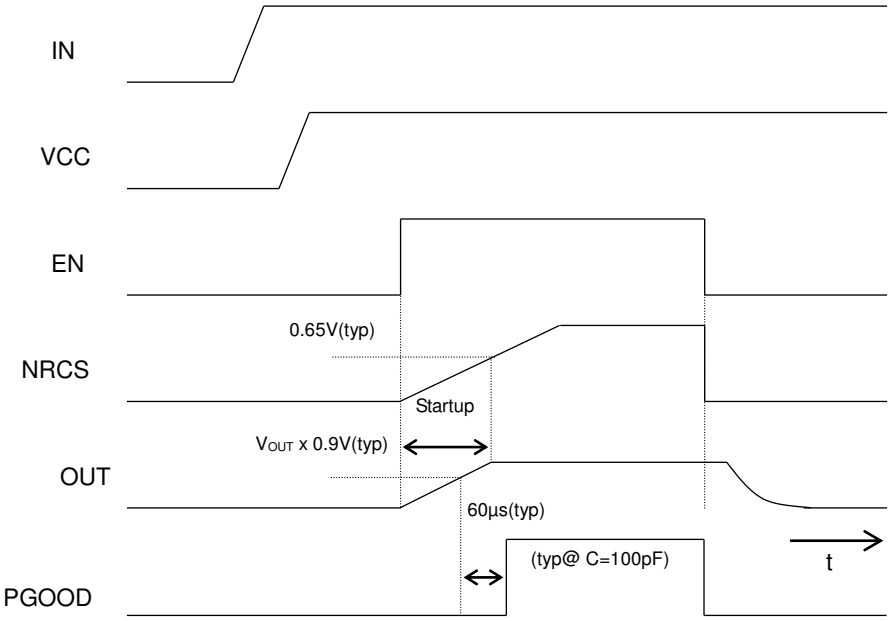
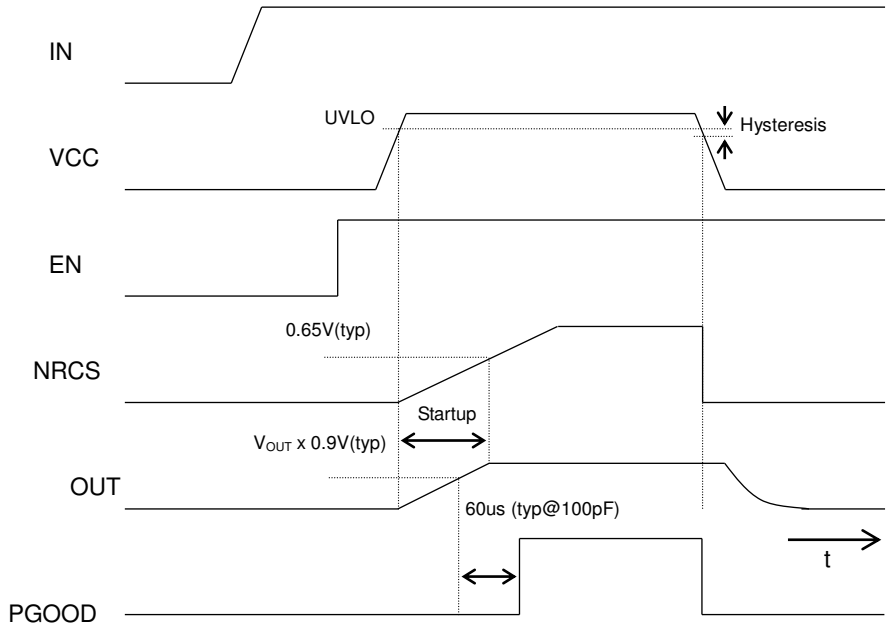
Timing Chart

EN ON/OFF



VCC ON/OFF



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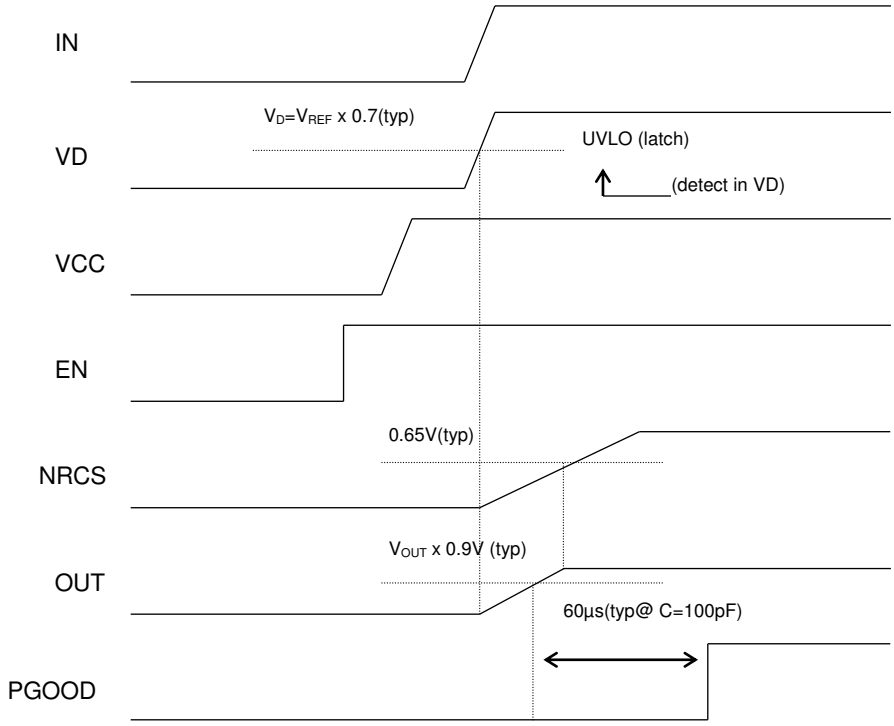
Timing Chart – continued

IN ON



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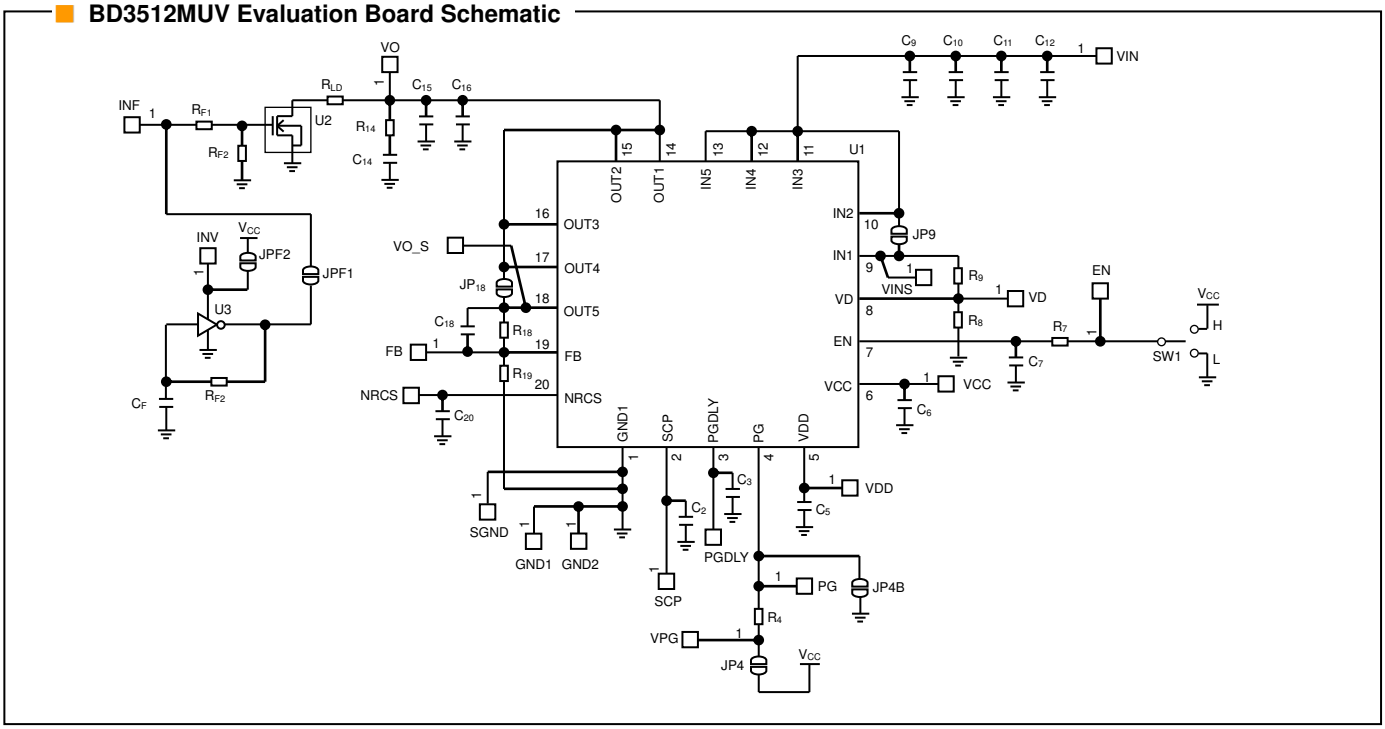
Application Information

1. Evaluation Board

BD3512MUV Evaluation Board Schematic



BD3512MUV Evaluation Board Standard Component List

Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD3512MUV
C_2	100pF	MURATA	CRM1882C1H101JA01
C_3	100pF	MURATA	CRM1882C1H101JA01
R_4	100kΩ	ROHM	MCR03EZPF1003
C_5	0.1µF	KYOCERA	CM05104K10A
C_6	1µF	KYOCERA	CM105B105K06A
R_7	0Ω	-	Jumper

Component	Rating	Manufacturer	Product Name
R_8	3.9kΩ	ROHM	MCR03EZPF3901
R_9	3.3kΩ	ROHM	MCR03EZPF3301
C_9	10µF	KYOCERA	CM21B106M06A
C_{16}	22µF	KYOCERA	CM316B226M06A
R_{18}	3.3kΩ	ROHM	MCR03EZPF3301
R_{19}	3.9kΩ	ROHM	MCR03EZPF3901
V_{20}	0.01µF	MURATA	GRM188B11H102KA01

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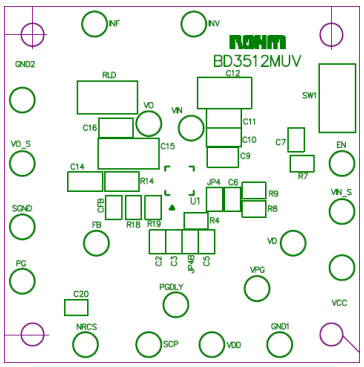
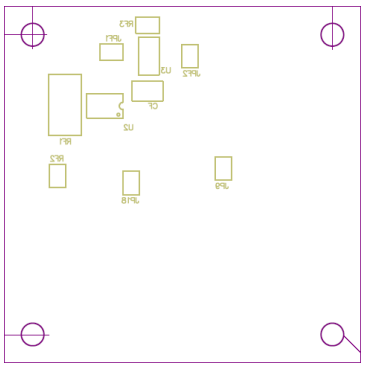
■ **BD3512MUV Evaluation Board Layout**

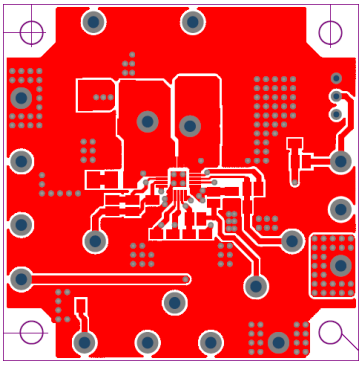
Silk Screen (Top)



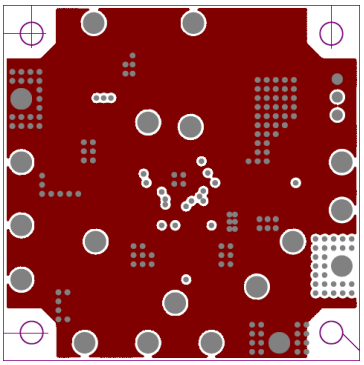
Silk Screen (Bottom)



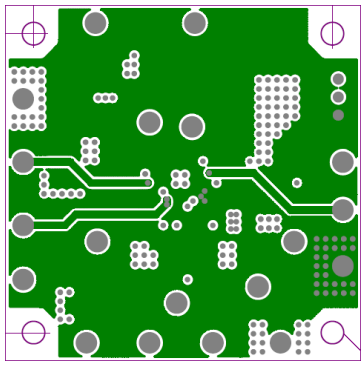
TOP Layer



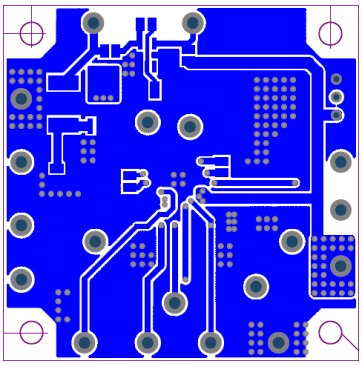
Middle Layer_1



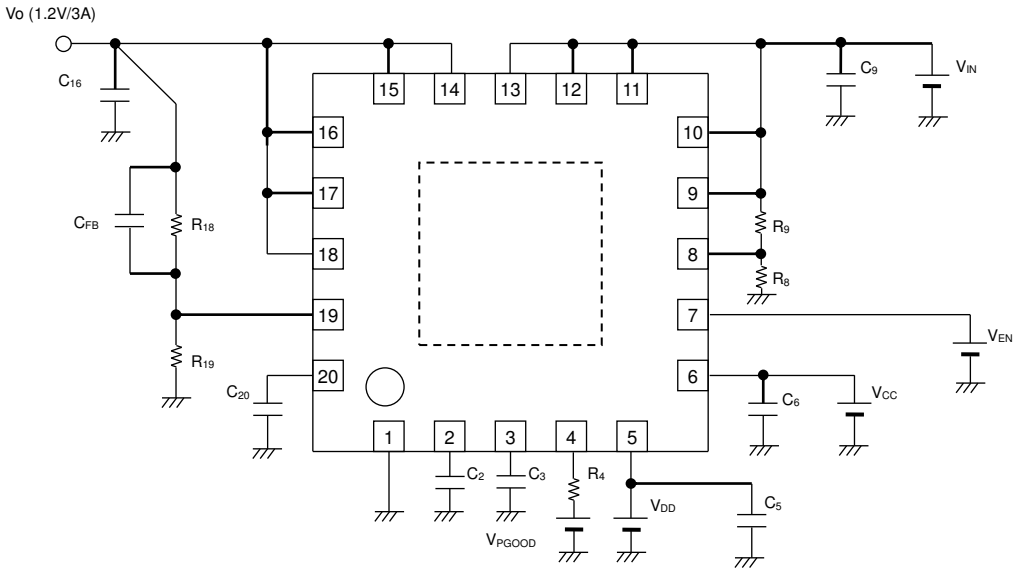
Middle Layer_2



Bottom Layer



2. Recommended Circuit Example



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Component	Recommended Value	Programming Notes and Precautions
R_{18}/R_{19}	3.3kΩ/3.9kΩ	IC output voltage can be set by the formula V_{FB} x (R_{18}+R_{19})/R_{19} using the values for the internal reference output voltage (V_{FB}) and the output voltage resistors (R_{18}, R_{19}). Select resistance values that will avoid the impact of the FB bias current (±100nA). The recommended total resistance value is 10KΩ.
R_4	100kΩ	This is the pull-up resistance for open-drain pin. It is recommended to set the value about 100kΩ.
C_{16}	22µF	To assure output voltage stability, please be certain that OUT1 to OUT5 pins and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22µF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. Please confirm operation across a variety of temperature and load conditions.
C_6/C_5	1µF/0.1µF	Input capacitors reduce the output impedance of the voltage supply source connected to the (VCC,VDD) input pins. If the impedance of this power supply were to increase, input voltage (V_{CC},V_{DD}) could become unstable, leading to oscillation or lowering ripple rejection function. While a low-ESR 1µF/0.1µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.
C_9	10µF	Input capacitors reduce the output impedance of the voltage supply source connected to the (IN) input pins. If the impedance of this power supply were to increase, input voltage (V_{IN}) could become unstable, leading to oscillation or lowering ripple rejection function. While a low-ESR 10µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.
C_{20}	0.01µF	The Non-Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (IN to OUT) and affects output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or when the UVLO function is deactivated. The temporary reference voltage is proportional to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportional to this reference voltage. Capacitors with low susceptibility to temperature are recommended to ensure a stable soft-start time.
C_{FB}	1000pF	This component is employed when the C_{16} capacitor causes, or may cause, oscillation. It provides more precise internal phase compensation.

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3. Heat Loss

In thermal design, consider the temperature range wherein the IC is guaranteed to operate and apply appropriate margins. The temperature conditions that need to be considered are listed below:

(1) Ambient temperature (Ta) should not be higher than 100°C.
(2) Chip junction temperature (Tj) should not be higher than 150°C.

The chip's junction temperature can be determined as follows:

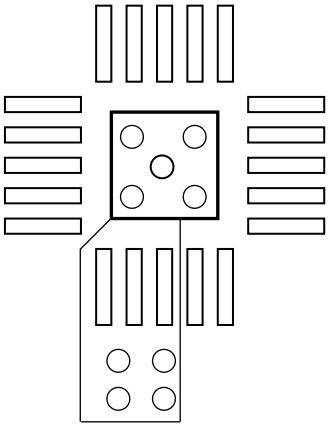
① Calculation based on ambient temperature (Ta)

$$Tj = Ta + \theta j - a \times W$$

<Reference values>

θj-a:VQFN020V4040 367.6°C/W IC only
178.6°C/W 1-layer board(copper foil area : 10.29mm^2)
56.6°C/W 4-layer board(copper foil area : front and reverse 10.29mm^2 , 2nd and 3rd 5505mm^2)
35.1°C/W 4-layer board(copper foil area : each 5505mm^2)
Substrate size: 74.2 x 74.2 x 1.6mm^3 (substrate with thermal via)

It is recommended to layout multiple VIAs, for heat radiation, in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multi-layer substrate). This package is so small (size: 4.0mm x 4.0mm) to layout the VIA at the bottom of IC. Spreading the pattern and increasing the number of VIA, as shown in the figure below, enable to achieve most heat radiation characteristics. It is recommended that the size and number of VIA are designed suitable for the actual application (see figure below).



Most heat loss in BD3512MUV occurs at the output N-Channel FET. Power loss is determined by multiplying the total V_{IN}-V_{OUT} voltage by the output current. Be sure to confirm the system input-to-output voltage and the output current conditions in relation to the heat dissipation characteristics of the IN and OUT in the design. Considering that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3512MUV) make certain to factor conditions such as substrate size into the thermal design.

$$\text{Power consumption (W)} = \left\{ \text{Input voltage } (V_{IN}) - \text{Output voltage } (V_{OUT})\ (V_{OUT} \approx V_{REF}) \right\} \times I_{OUT}(\text{Ave})$$

For instance, V_{IN}=1.5V, V_{OUT}=1.25V, I_{OUT}(Ave) = 3A,

$$\begin{aligned} Power\ consumption\,(W) &= \{1.5\,(V) - 1.25\,(V)\} \times 3.0\,(A) \\ &= 0.75\,(W) \end{aligned}$$

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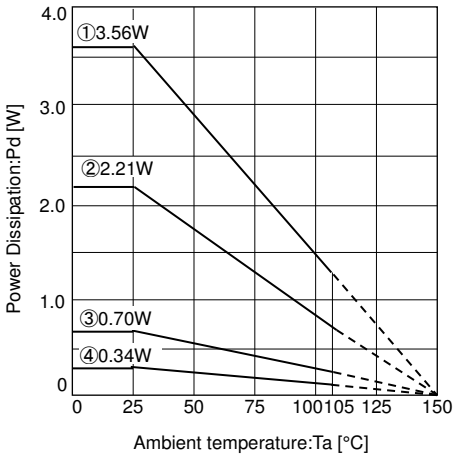
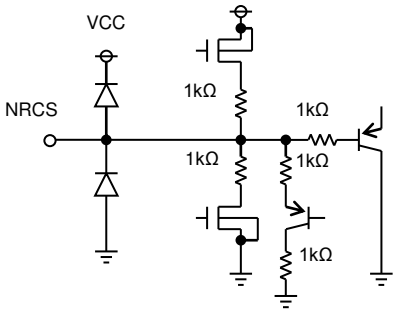
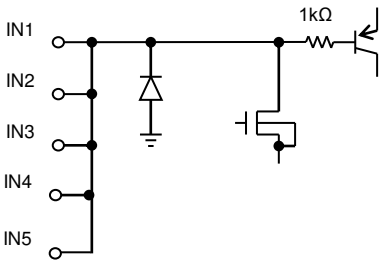
Power Dissipation

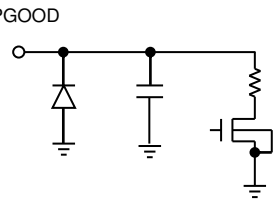


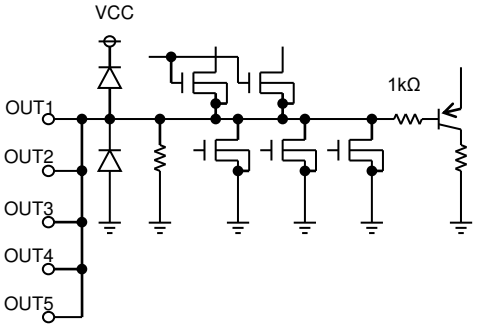
① 4 layers (Copper foil area : 5505mm^2)
copper foil in each layers.
θ j-a=35.1°C/W
② 4 layers (Copper foil area front and reverse : 10.29mm^2、
2nd and 3rd : 5505mm^2)
θ j-a=56.6°C/W
③ 1 layer (Copper foil area : 10.29m^2)
θ j-a=178.6°C/W
④ IC only.
θ j-a=367.6°C/W

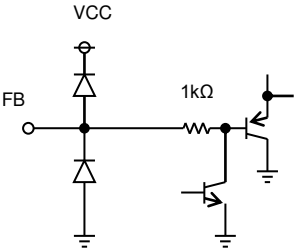
I/O Equivalent Circuits

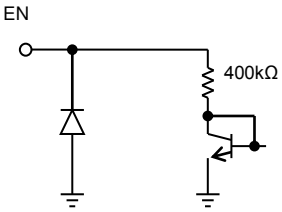












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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

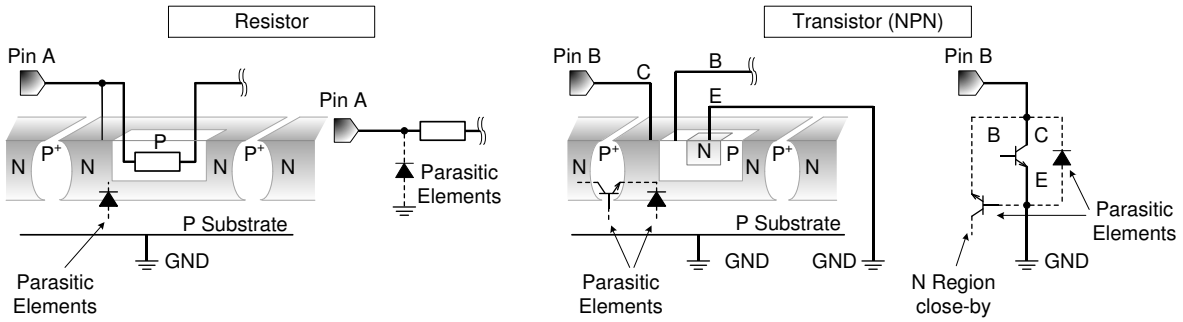


Figure 24. Example of monolithic IC structure

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

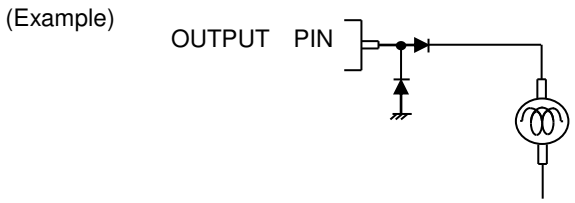
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

	TSD on Temperature [°C] (typ)
BD3512MUV	175

15. Output Pin

In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.



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Ordering Information

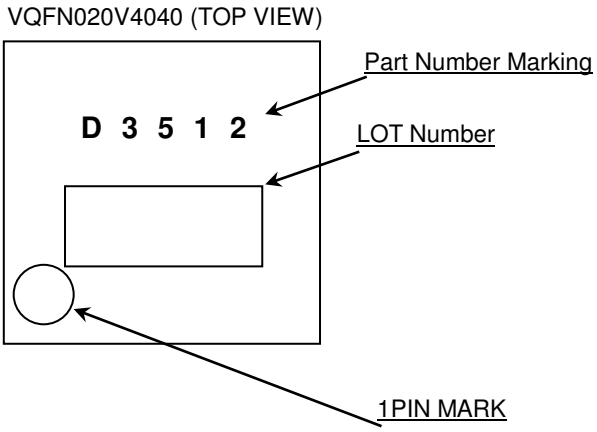
B D 3 5 1 2 M U V - E 2

Part Number

Package
MUV: VQFN020V4040

Packaging and forming specification
E2: Emboss tape reel opposite draw-out side: 1 pin

Marking Diagram



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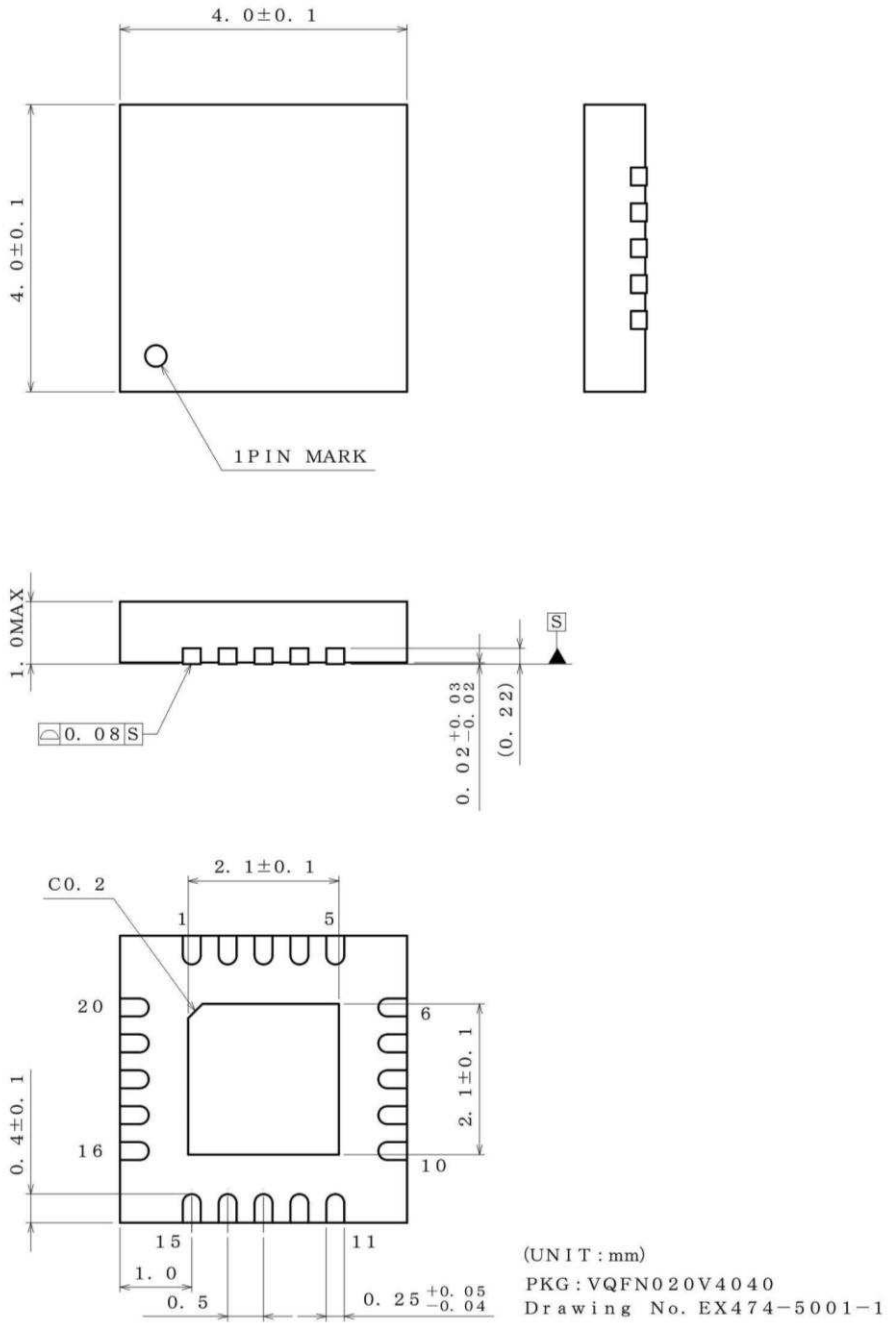
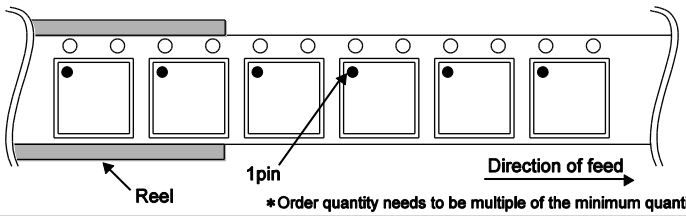
Physical Dimension, Tape and Reel Information

Package Name	VQFN020V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
02.Nov.2015	001	New Release

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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