Silicon PNP Power Transistors 2SB1016

DESCRIPTION

·With TO-220Fa package
·High breakdown voltage
·Low collector saturation voltage
·Complement to type 2SD1407

APPLICATIONS

·Power amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base

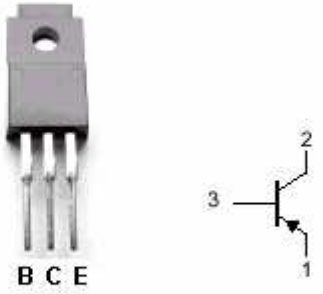

Fig.1 simplified outline (TO-220Fa) and symbol

Absolute maximum ratings(Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-100	V
V_{CEO}	Collector -emitter voltage	Open base	-100	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-5	A
I_B	Base current		-0.5	A
P_C	Collector power dissipation	T_C=25□	30	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-50mA; I_B=0	-100			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-4A ;I_B=-0.4A			-2.0	V
V_{BE}	Base-emitter voltage	I_C=-4A; V_{CE}=-5V			-1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=-100V; I_E=0			-100	μA
I_{EBO}	Emitter cut-off current	V_{EB}=-5V; I_C=0			-1	mA
h_{FE-1}	DC current gain	I_C=-1A ; V_{CE}=-5V	40		240	
h_{FE-2}	DC current gain	I_C=-4A ; V_{CE}=-5V	20			
f_T	Transition frequency	I_C=-1A; V_{CE}=-5V		5		MHz
C_{OB}	Collector output capacitance	f=1MHz ; V_{CB}=-10V;I_E=0		270		pF

◆ **h_{FE-1} Classifications**

R	O	Y
40-80	70-140	120-240

PACKAGE OUTLINE

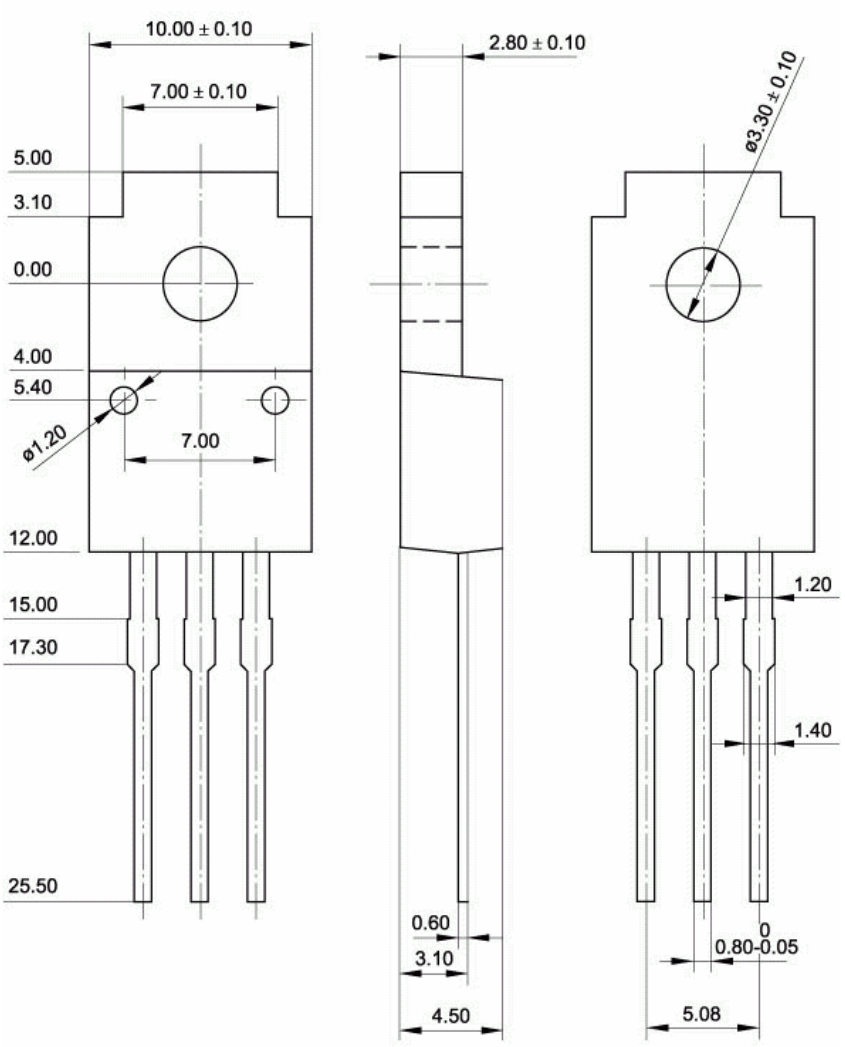

Fig.2 Outline dimensions (unindicated tolerance:±0.15 mm)

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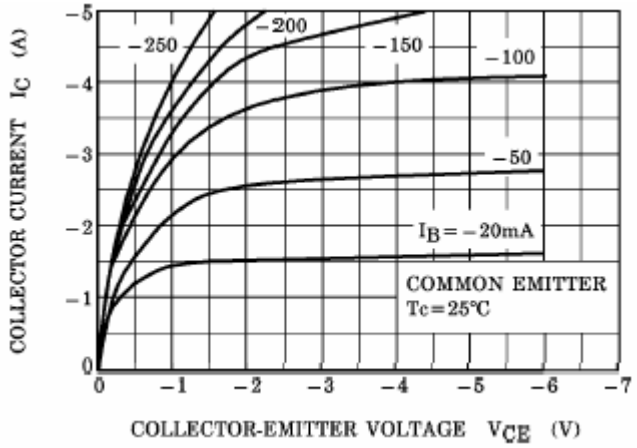

Fig.3 Static Characteristic

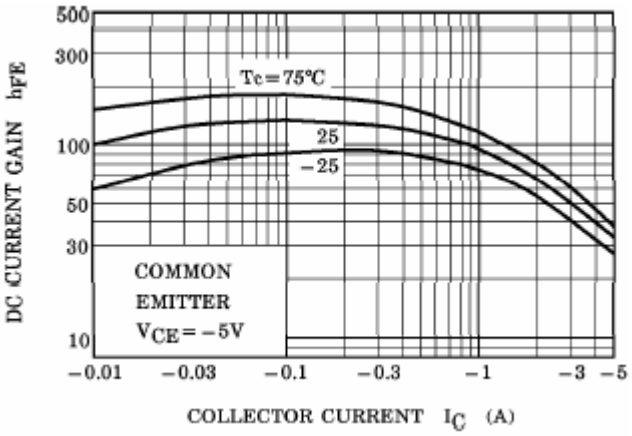

Fig.4 DC current Gain

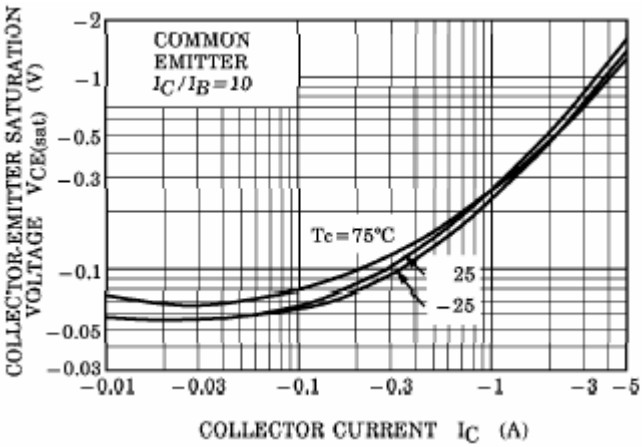

Fig.5 Collector-Emitter Saturation Voltage

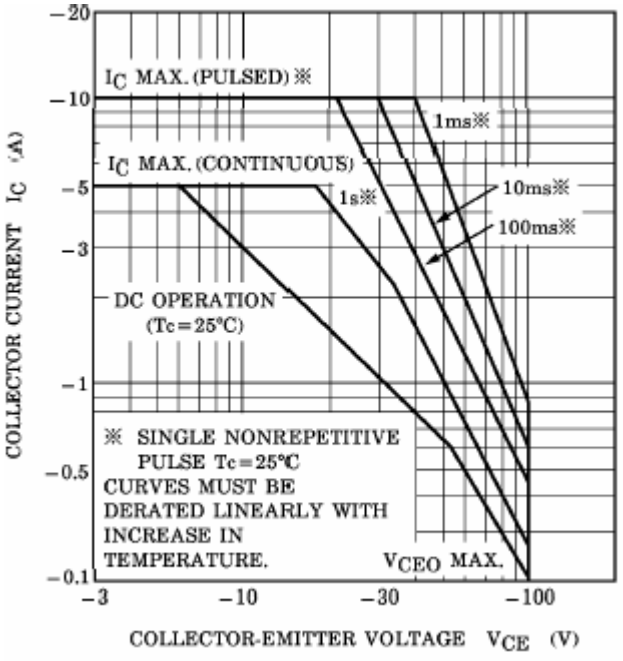

Fig.6 Safe Operating Area

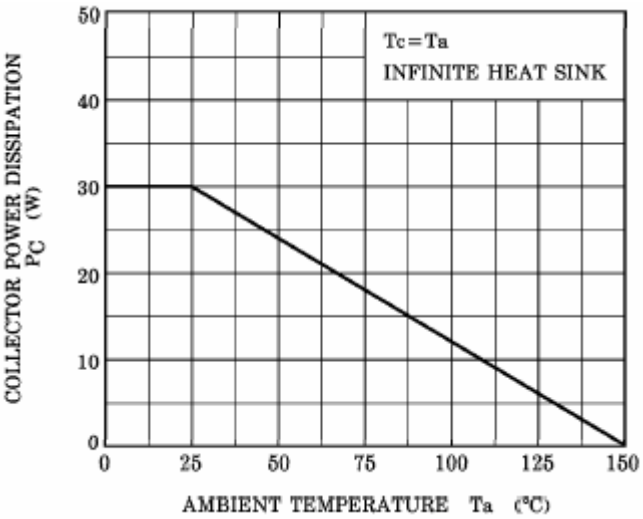

Fig.7 Pc−Ta Derating