Si51218

THREE OUTPUTS FACTORY PROGRAMMABLE CLOCK GENERATOR

Features

- Generates up to 3 LVCMOS clock outputs from 32.768 kHz to 200 MHz
- Accepts crystal or reference clock input
  - 3 to 166 MHz reference clock input
  - 8 to 48 MHz crystal input
- Programmable FSEL, $\overline{PD}$ and OE input functions
- Low power dissipation
- Separate voltage supply pins
  - V_{DD} = 2.5 to 3.3 V
  - V_{DDO}= 1.8 to 3.3 V ($V_{DDO} \leq V_{DD}$)
- Low cycle-cycle jitter
- Programmable output rise and fall times
- Ultra small 8-pin TDFN package (1.4 mm x 1.6 mm)
- Operation temperature: 0–70 °C

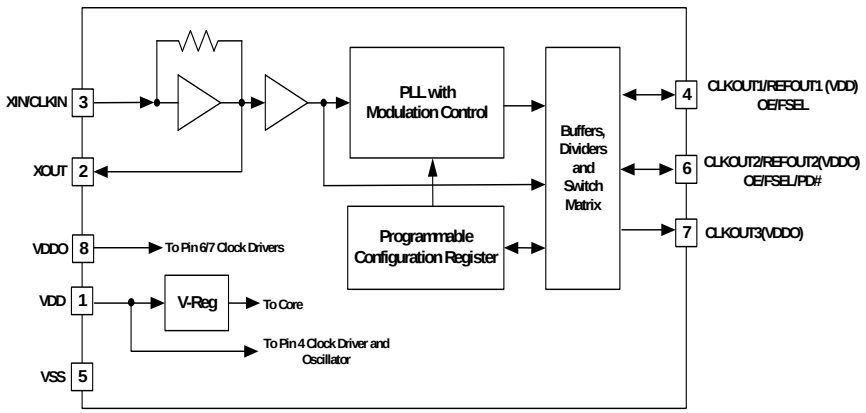
Applications

- Crystal / XO replacement
- Digital Media players
- Portable Devices
- DTV/IPTV

Description

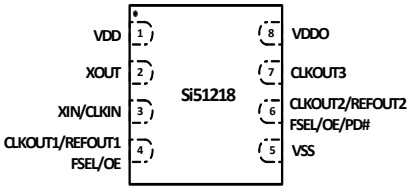
The factory programmable Si51218 is a low power, small footprint and frequency flexible programmable clock generator targeting low power, low cost and high volume consumer and embedded applications. The device operates from a single crystal or an external clock source and generates up to 3 clock outputs from 32.768 kHz to 200 MHz. They are factory programmed to provide customized output frequencies, control inputs and ac parameter tuning like output drive strength that are optimized for customer board condition and application requirements. A separate VDDO supply pin supports clock outputs at a different voltage level.

Functional Block Diagram



Ordering Information:
See page 10.

Pin Assignments



Patents pending

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1. Electrical Specifications

Table 1. DC Electrical Specifications

(V_{DD}=3.3 V ± 10% or V_{DD}=2.5 V ± 5%, T_A=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	V_{DD}=3.3 V ±10%	2.97	3.3	3.63	V
		V_{DD}=2.5 V ±5%	2.375	2.5	2.625	V
	V_{DDO}	$V_{DDO} \le V_{DD}$	1.71	—	3.6	V
Output High Voltage	V_{OH}	I_{OH}= –4 mA, V_{DDX}=V_{DD} or V_{DDO}	V_{DDX}-0.5	—	—	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA,	—	—	0.3	V
Input High Voltage	V_{IH}	CMOS level	0.7 V_{DD}	—	—	V
Input Low Voltage	V_{IL}	CMOS level	—	—	0.3 V_{DD}	V
Operating Supply Current	I_{DD}	F_{IN}=20 MHz, CLK-OUT1=32.768KHz, REFOUT2=20 MHz CLK-OUT3=26MHz, C_L=0, V_{DD}=V_{DDO}=3.3 V	—	6	—	mA
Nominal Output Impedance	Z_O		—	30	—	Ω
Internal Pull-up/Pull-down Resistor	R_{PUP}/R_{PD}	Pin 6	—	150k	—	Ω
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Load Capacitance	C_L	Clock outputs < 166 MHz	—	—	15	pF
		Clock outputs > 166 MHz	—	—	10	pF

Table 2. AC Electrical Specifications

(V_{DD}=3.3 V ± 10% or V_{DD}=2.5 V ± 5%, T_A=0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency Range	F_{IN1}	Crystal input	8	—	48	MHz
Input Frequency Range	F_{IN2}	Reference clock Input	3	—	166	MHz
Output Frequency Range	F_{OUT}		0.032768	—	200	MHz
Frequency Accuracy	F_{ACC}	Configuration dependent	—	0	—	ppm
Output Duty Cycle	DC_{OUT}	Measured at $V_{DD/2}$	45	50	55	%
Input Duty Cycle	DC_{IN}	CLKIN, CLKOUT through PLL	30	50	70	%
Output Rise Time	t_r	CLKOUT1/2/3 in MHz range C_L=15 pF, 20 to 80%	—	1	3.0	ns
Output Fall Time	t_f	CLKOUT1/2/3 in MHz range C_L=15 pF, 20 to 80%	—	1	3.0	ns
Period Jitter	PJ_1	CLKOUT1/2/3 in MHz range, V_{DD}=V_{DDO}=3.3 V, CL=15 pF	—	150*	—	ps
Period Jitter	PJ_2	CLKOUT1/3 at 32.768KHz, V_{DD}=V_{DDO}=3.3 V, CL=15 pF	—	1500*	—	ps
Cycle-to-Cycle Jitter	CCJ	CLKOUT1/2/3, in MHz range V_{DD}=V_{DDO}=3.3 V, CL=15 pF	—	100*	—	ps
Power-up Time	t_{PU}	Time from 0.9 V_{DD} to valid frequencies at all clock outputs	—	1.2	5.0	ms
Output Enable Time	t_{OE}	Time from OE raising edge to active at outputs (asynchronous)	—	15	—	ns
Output Disable Time	t_{OD}	Time from OE falling edge to active at outputs (asynchronous)	—	15	—	ns

***Note:** Jitter performance depends on configuration and programming parameters.

Table 3. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$		–0.5	—	4.2	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	V_{DD}+0.5	V
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional, C-Grade	0	—	70	°C
Temperature, Junction	T_J	Functional, power is applied	—	—	125	°C
Temperature, Soldering	T_{Sol}	Non-functional	—	—	260	°C
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	–4000	—	4000	V
ESD Protection (Charge Device Model)	ESD_{CDM}	JEDEC (JESD 22 - C101)	–1500	—	1500	V
ESD Protection (Machine Model)	ESD_{MM}	JEDEC (JESD 22 - A115)	–200	—	200	V

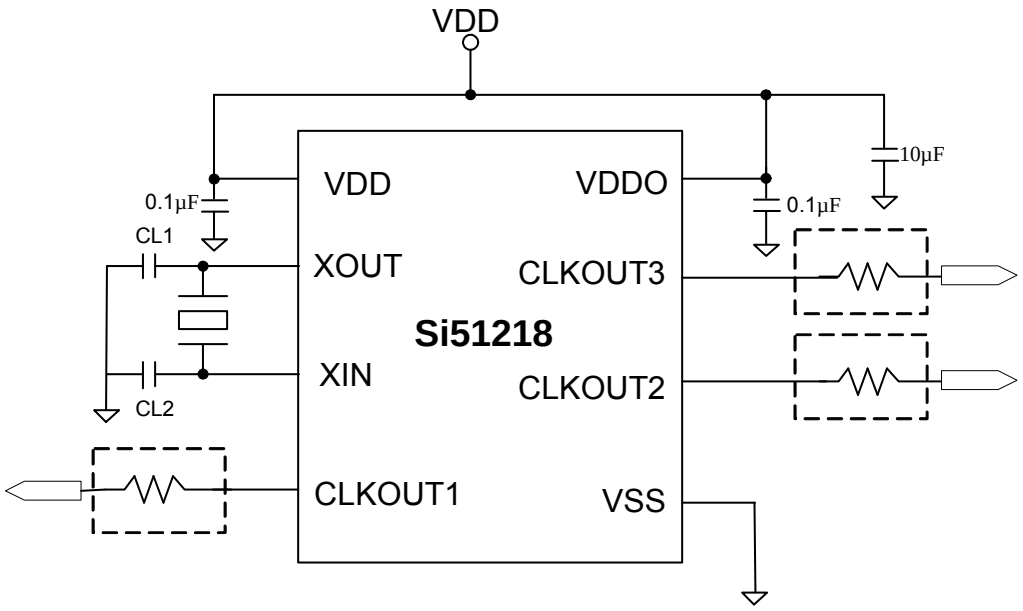
Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

Table 4. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still air	170.8	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still air	98.8	°C/W

2. Design Considerations

2.1. Typical Application Schematic



Dotted line shows the optional termination resistors

2.2. Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1 µF must be used between VDD and VSS on the pins 1 and 8. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD pin. In addition, a 10 µF capacitor should be placed between VDD and VSS.

Crystal and Crystal Load: Only use a parallel resonant fundamental AT cut crystal. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm) make sure that external crystal load capacitor is matched to crystal load specification. To determine the value of CL1 and CL2, use the following formula:

$$CL1 = CL2 = 2CL - (Cpin + Cp)$$

Where: CL is load capacitance stated by crystal manufacturer

Cpin is the Si51218 pin capacitance (4pF)

Cp is the parasitic capacitance of the PCB traces.

Example: If a crystal with CL=12 pF specification is used and Cp=1 pF (parasitic PCB capacitance on PCB), 19 pF external capacitors from pins XIN (pin 3) and XOUT (Pin 2) to VSS are required. Users must verify Cp value.

3. Functional Description

3.1. Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals and ceramic resonators. If an external clock is used, the input frequency range is from 8.0 to 166.0 MHz.

3.2. Output Frequency Range and Outputs

Up to three outputs can be programmed as CLKOUT or REFOUT. CLKOUT output can be synthesized to frequency value from 32.768 kHz to 200 MHz. REFOUT is the buffered output of the oscillator and is the same frequency as the input frequency. REFOUT2 (pin6) frequency can also be programmed to input frequency divided by 2 to 32. By using only low cost, fundamental mode crystals, the Si51218 can synthesize output frequency up to 200 MHz, eliminating the need for higher order crystals (Xtals) and crystal oscillators (XOs). The 32.768 kHz output can replace the 32.768 kHz crystal which is widely used in many embedded and mobile systems. This reduces the cost while improving the system clock accuracy, performance, and reliability.

3.3. Frequency Select (FSEL)

The Si51218 pin 4 and 6 can be programmed as frequency select input (FSEL). If FSEL function is used, one output pin can switch between two predefined frequencies by FSEL input. The set of frequencies in Table 5 is given as an example.

Table 5. Example Frequencies

FSEL (Pin 6)	CLKOUT3 (Pin 7)
0	66 MHz
1	33 MHz

3.4. Power Down ($\overline{PD}$) or Output Enable (OE)

The Si51218 pin 6 can be programmed as $\overline{PD}$ input. Pin 4 and pin 6 can be programmed as OE input. $\overline{PD}$ turns off both PLL and output buffers whereas OE only disables the output buffers to Hi-Z.

4. Pin Descriptions—8-Pin TDFN

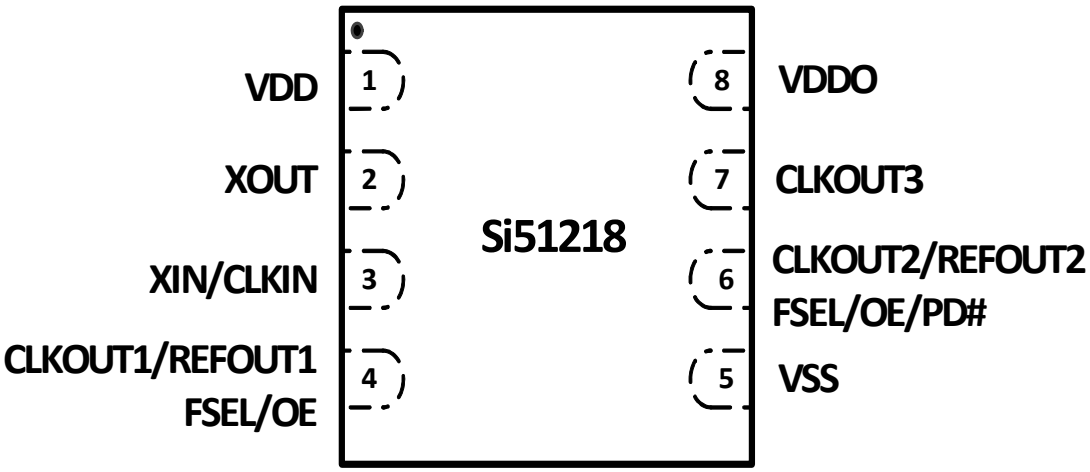
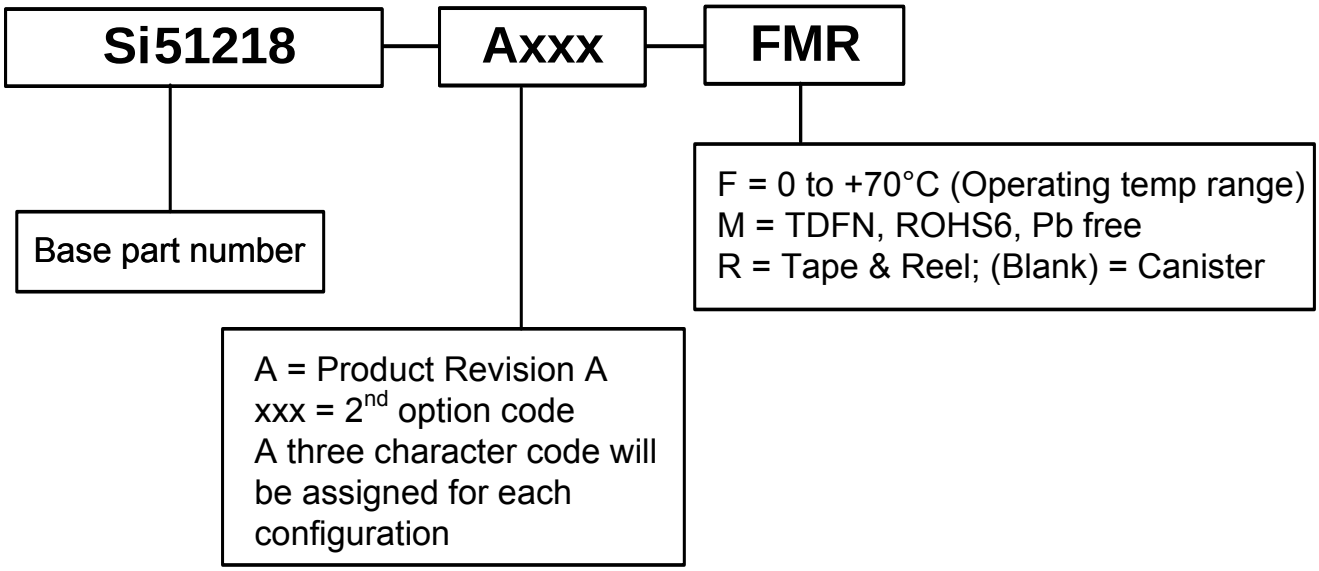


Table 6. Si51218 Pin Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	2.5 to 3.3 V power supply.
2	XOUT	O	Crystal output. Leave this pin unconnected (floating) if an external clock input is used.
3	XIN/CLKIN	I	External crystal and clock input.
4	CLKOUT1/REFOUT1/ FSEL/OE	I/O	Programmable CLKOUT1 or REFOUT1 output or MultiFunction control input. The frequency at this pin is synthesized by internal PLL if programmed as CLKOUT1. If programmed as REFOUT1, output clock is buffered output of crystal or reference clock input. If programmed as MultiFunction control input, it can be FSEL and OE.
5	VSS	GND	Ground.
6	CLKOUT2/REFOUT2/ FSEL/OE/$\overline{PD}$	I/O	Programmable CLKOUT2 or REFOUT2 output or MultiFunction control input. The frequency at this pin is synthesized by internal PLL if programmed as CLKOUT2. If programmed as REFOUT2, output clock is buffered output of crystal or reference clock input. If programmed as MultiFunction control input, it can be FSEL,OE and $\overline{PD}$. It is power by VDDO (pin 8).
7	CLKOUT3	O	Programmable CLKOUT3 output. The frequency at this pin is synthesized by internal PLL. It is power by VDDO (pin 8).
8	VDDO	PWR	1.8 to 3.3 V output power supply to CLKOUT2/3 (pin6/7).

5. Ordering Information

Part Number	Package Type	Temperature
Si51218-AxxxFM	8-pin TDFN	Commercial, 0 to 70 °C
Si51218-AxxxFMR	8-pin TDFN—Tape and Reel	Commercial, 0 to 70 °C



6. Package Outline: 8-pin TDFN

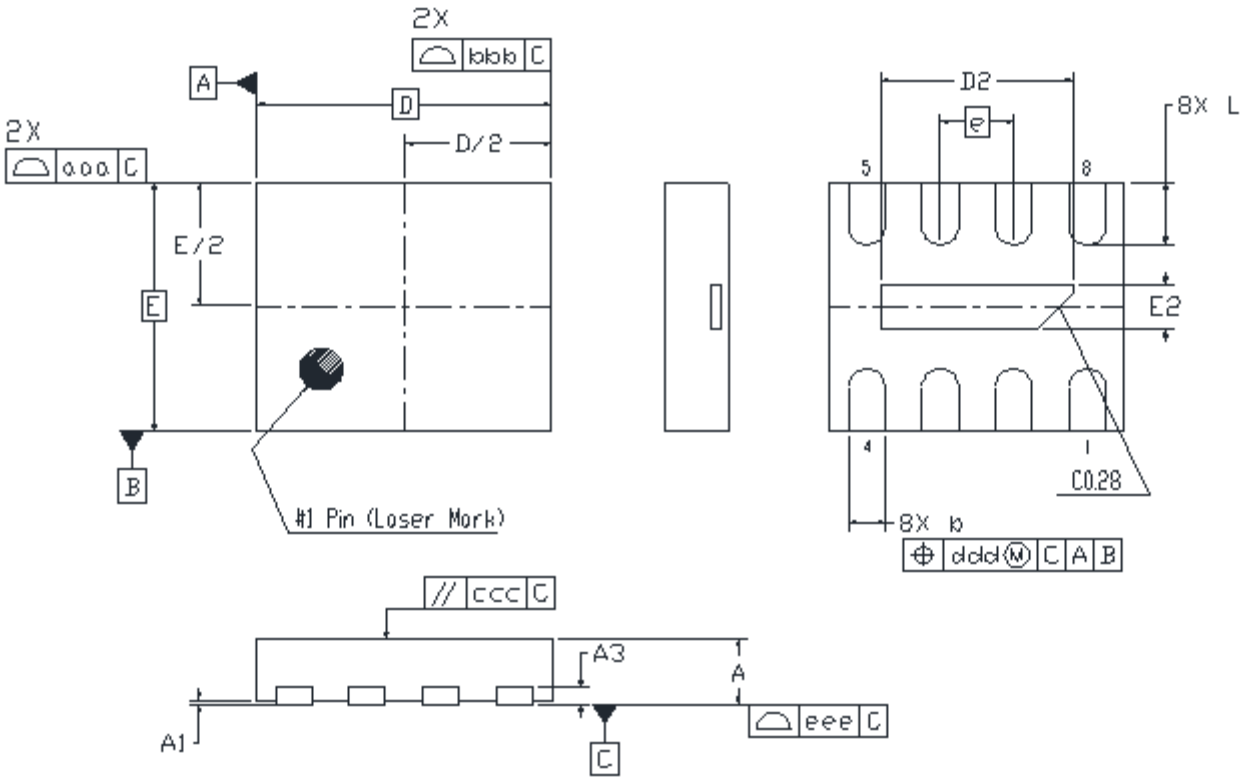


Figure 1. 8-Pin TDFN Package

Table 7. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		1.60 BSC	
D2	1.00	1.05	1.10
e		0.40 BSC	
E		1.40 BSC	
E2	0.20	0.25	0.30
L	0.30	0.35	0.40
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.07	
eee		0.08	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. PCB Land Pattern: 8-pin TDFN

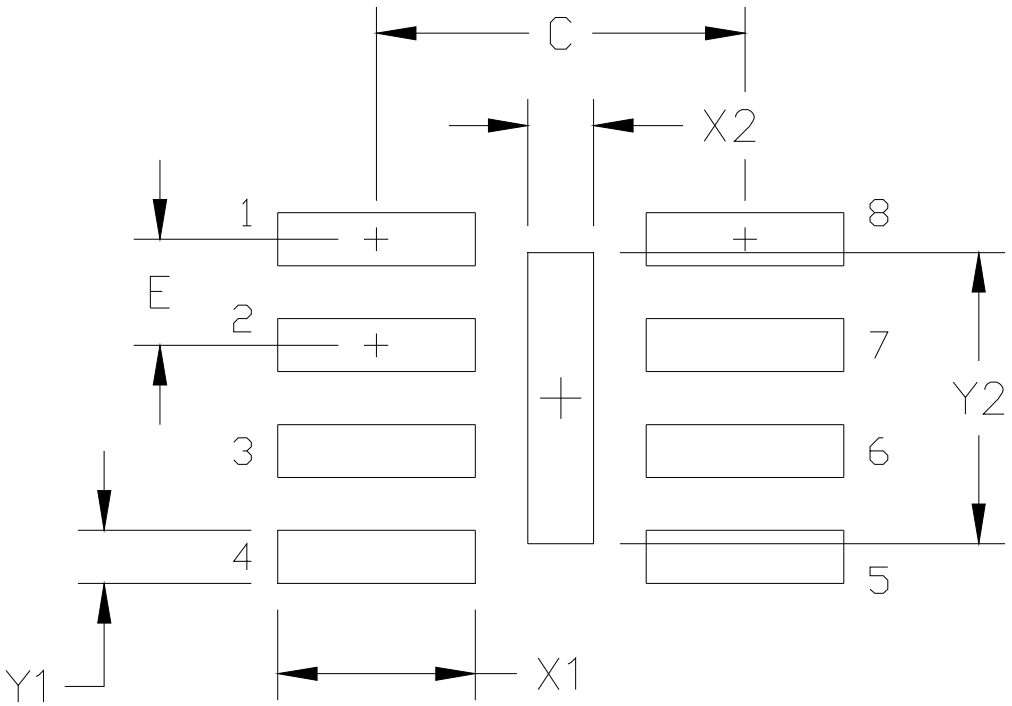


Figure 2. 8-Pin TDFN Land Pattern

Table 8. PCB Land Pattern Dimensions (mm)

Dimension	mm
C	1.40
E	0.40
X1	0.75
Y1	0.20
X2	0.25
Y2	1.10

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