

60V(D-S) N-Channel Enhancement Mode Power MOS FET

General Feature

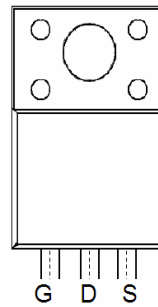
- $V_{DS} = 60V, I_D = 100A$
 $R_{DS(ON)} < 6.5m\Omega @ V_{GS} = 10V$ (Typ:5.7m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Lead Free

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

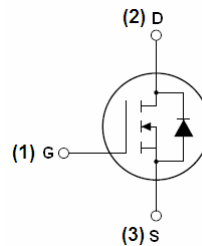


Marking and pin assignment

PIN Configuration



TO-220F top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN06B0F	MSN06B0F	TO-220F	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	70	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	45	W
Derating factor		0.3	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	550	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta jc}$	3.3	°C/W
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Electrical Characteristics (T_C=25°C unless otherwise noted)

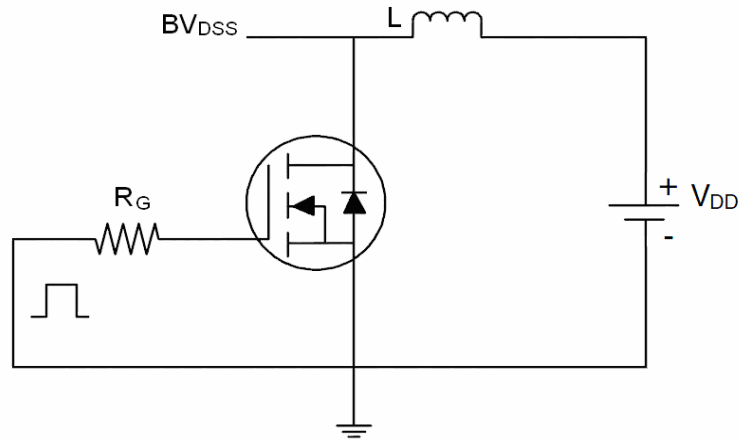
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	65	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	-	5.7	6.5	mΩ
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=40A$	-	50	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	4800	-	PF
Output Capacitance	C_{oss}		-	440	-	PF
Reverse Transfer Capacitance	C_{riss}		-	260	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=1A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	16.8	-	nS
Turn-on Rise Time	t_r		-	10.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	13.6	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$	-	85	-	nC
Gate-Source Charge	Q_{gs}		-	18	-	nC
Gate-Drain Charge	Q_{gd}		-	28	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S	-	-	-	90	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, I_F = 40A$ $di/dt = 100A/\mu s$ ^(Note 3)	-	38	-	nS
Reverse Recovery Charge	Q_{rr}		-	53	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

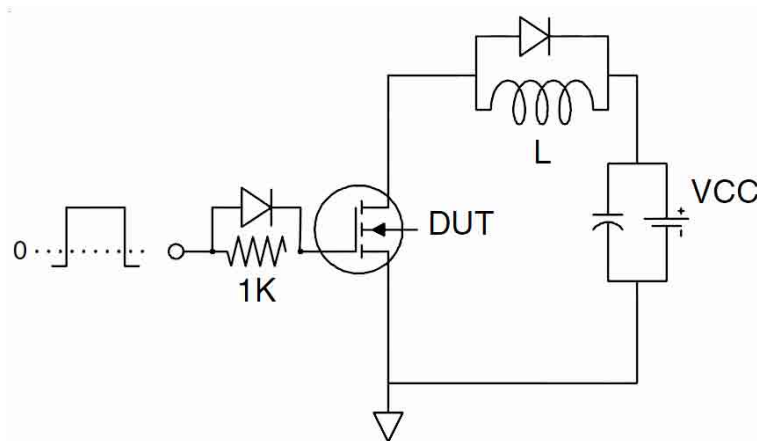
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T_J=25°C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25Ω

Test circuit

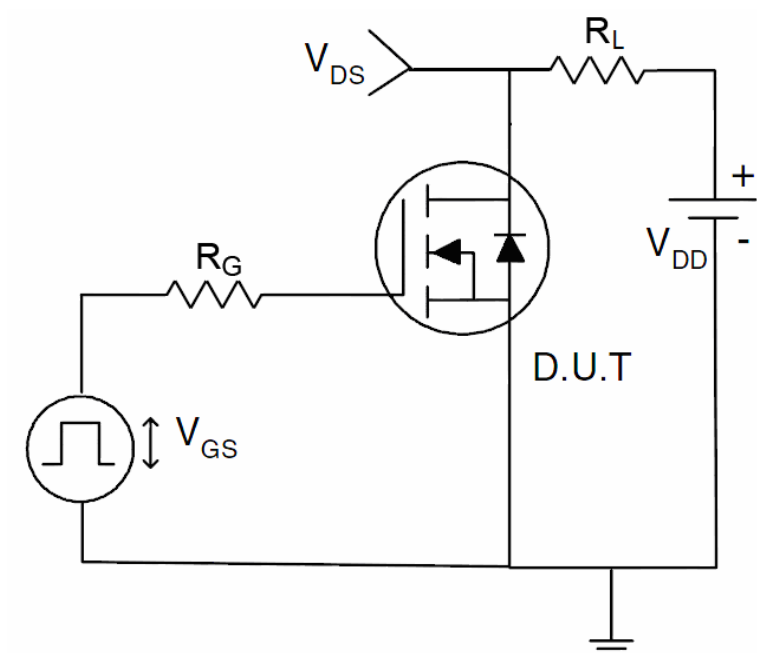
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

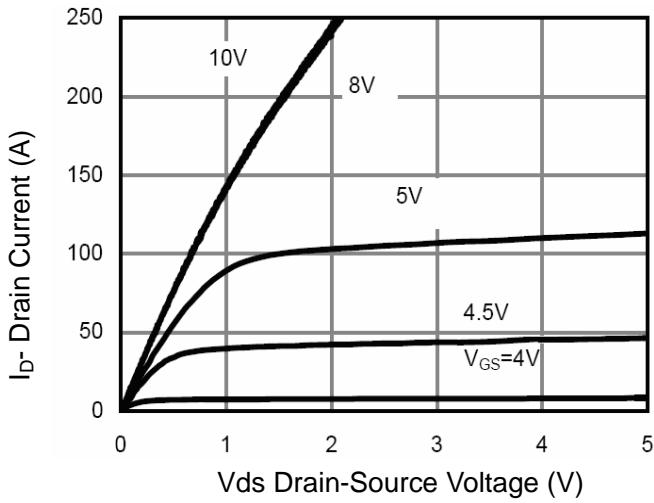


Figure 1 Output Characteristics

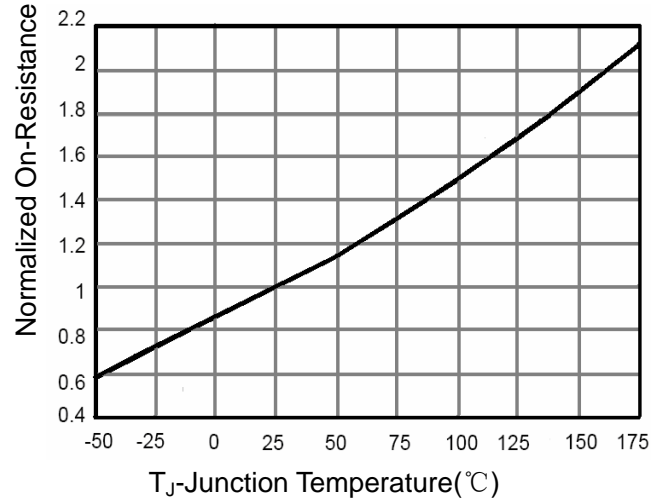


Figure 4 Rdson-Junction Temperature

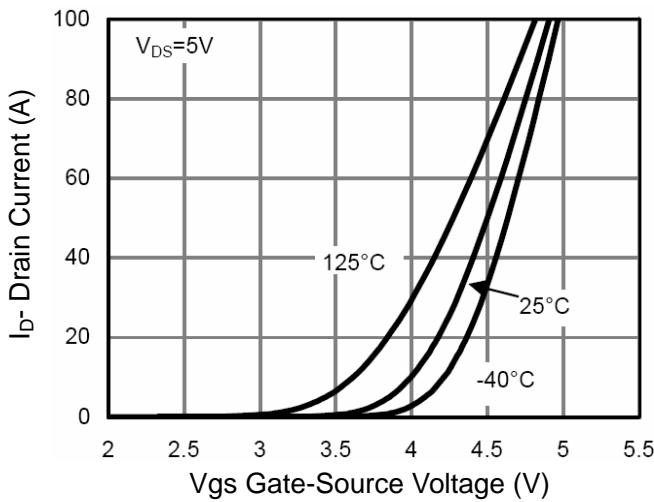


Figure 2 Transfer Characteristics

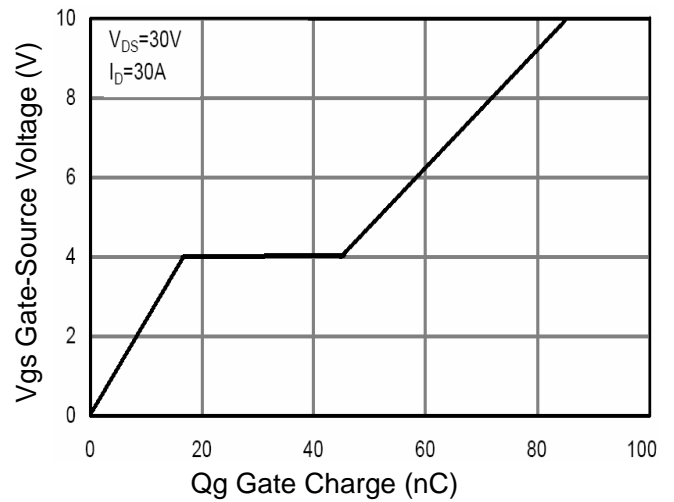


Figure 5 Gate Charge

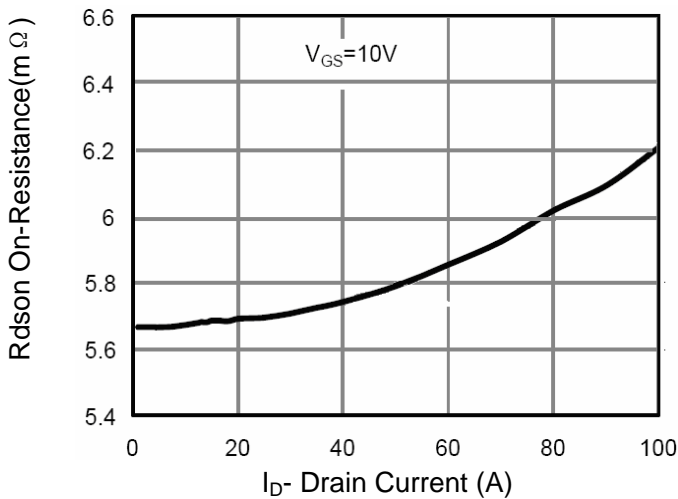


Figure 3 Rdson- Drain Current

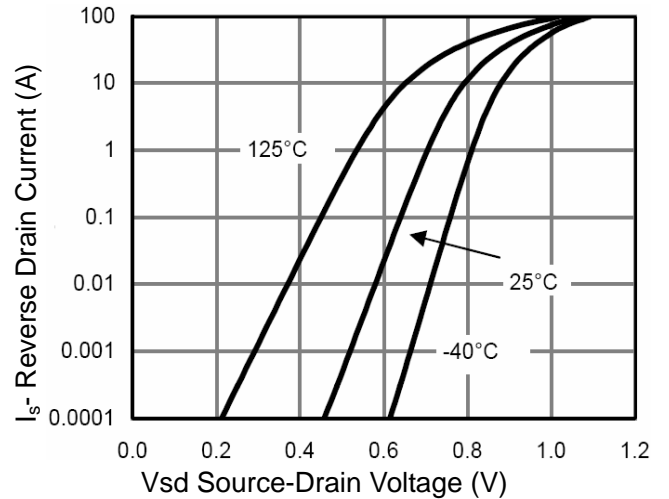


Figure 6 Source- Drain Diode Forward

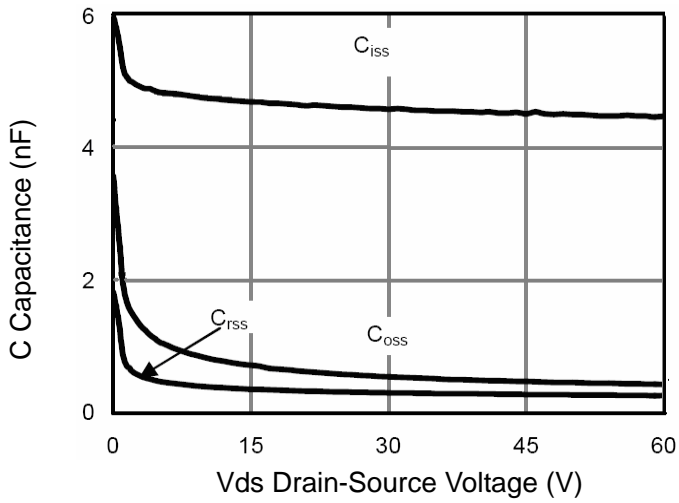


Figure 7 Capacitance vs Vds

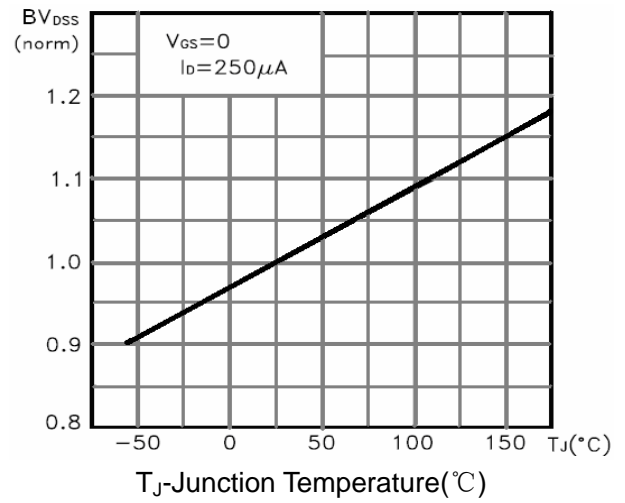


Figure 9 BV_{DSS} vs Junction Temperature

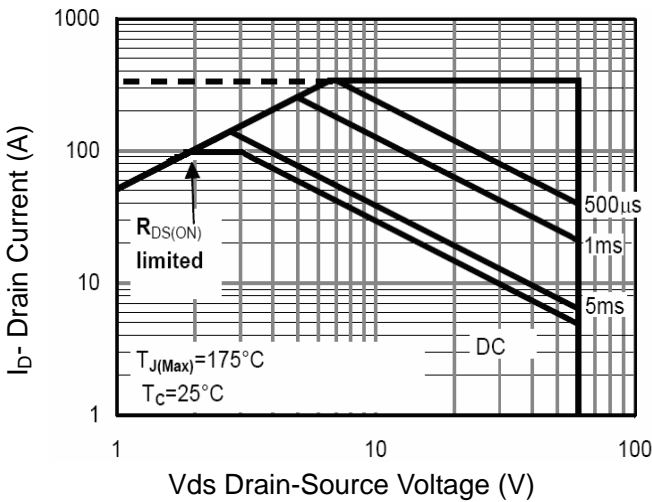


Figure 8 Safe Operation Area

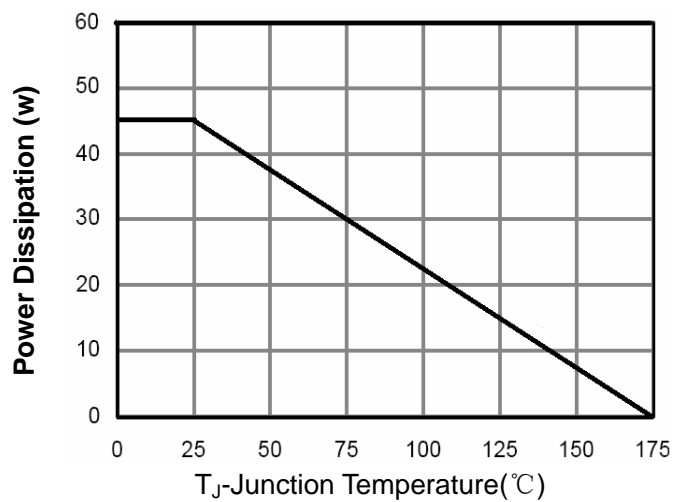


Figure 10 Power De-rating

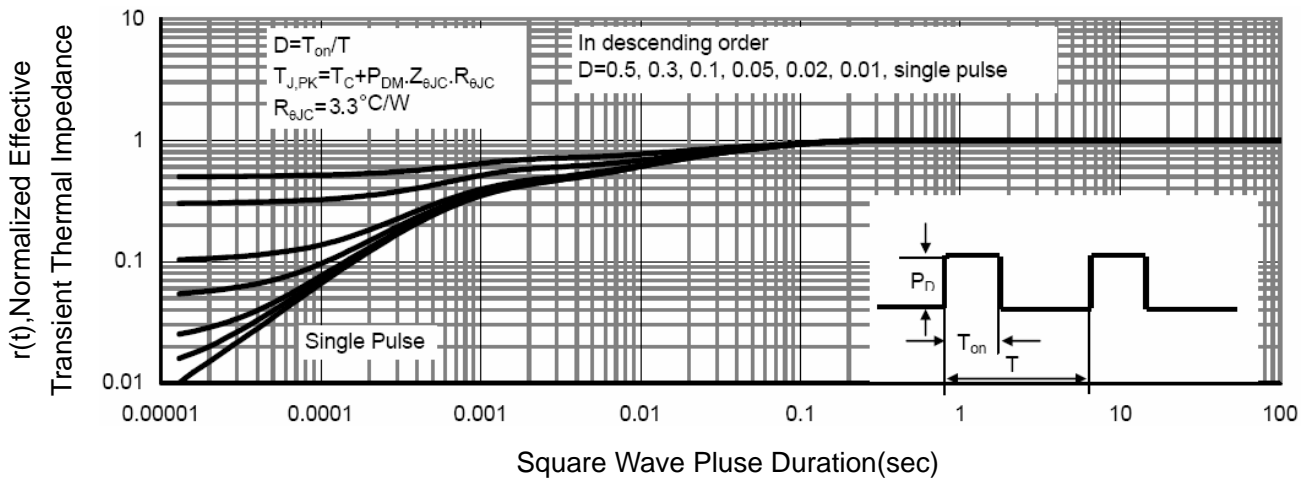
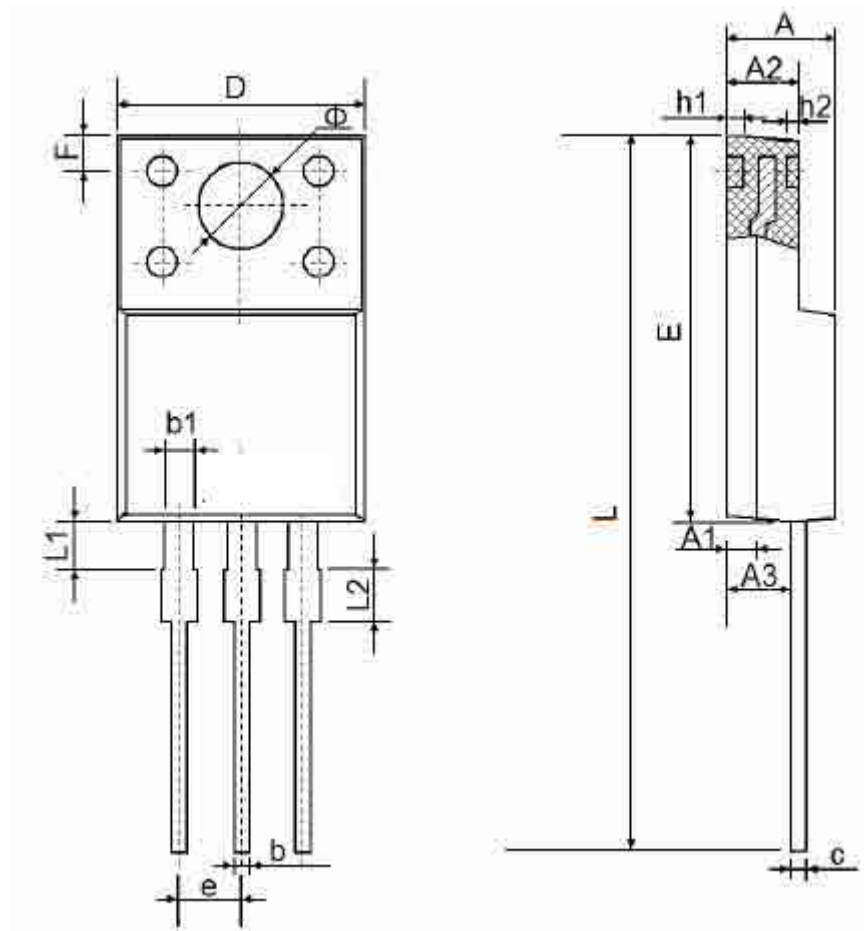


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220F Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	1.300REF		0.051REF	
A2	2.800	3.200	0.110	0.126
A3	2.500	2.900	0.098	0.114
b	0.500	0.750	0.020	0.030
b1	1.100	1.350	0.043	0.053
b2	1.500	1.750	0.059	0.069
c	0.500	0.750	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540TYP.		0.100TYP	
F	2.700REF		0.106REF	
φ	3.500REF		0.138REF	
h1	0.800REF		0.031REF	
h2	0.500REF		0.020REF	
L	28.000	28.400	1.102	1.118
L1	1.700	1.900	0.067	0.075
L2	1.900	2.100	0.075	0.083