RoHS Compliant

PNP Silicon Low-Power Transistor

Qualified per MIL-PRF-19500/485

Qualified Levels:
JAN, JANTX, JANTXV and JANS

DESCRIPTION

This family of 2N5415UA and 2N5416UA epitaxial planar transistors are military qualified up to a JANS level for high-reliability applications. The UA package is hermetically sealed and provides a low profile for minimizing board height. These devices are also available in the long-leaded TO-5, short-leaded TO-39 and low profile U4 packaging.

Important: For the latest information, visit our website http://www.microsemi.com.

FEATURES

- JEDEC registered 2N5415 through 2N5416 series
- JAN, JANTX, JANTXV, and JANS qualifications are available per MIL-PRF-19500/485. (See part nomenclature for all available options.)
- RoHS compliant

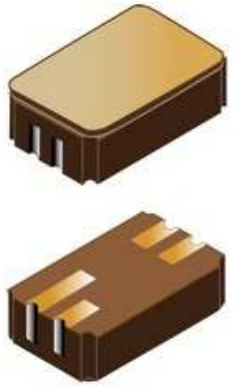
APPLICATIONS / BENEFITS

- General purpose transistors for low power applications requiring high frequency switching.
- Low package profile
- Military and other high-reliability applications

MAXIMUM RATINGS @ T_A = +25 °C unless otherwise noted

Parameters / Test Conditions	Symbol	2N5415UA	2N5416UA	Unit
Collector-Emitter Voltage	V_{CEO}	200	300	V
Collector-Base Voltage	V_{CBO}	200	350	V
Emitter-Base Voltage	V_{EBO}	6.0	6.0	V
Collector Current	I_C	1.0	1.0	A
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
Thermal Resistance Junction-to-Ambient	$R_{\Theta JA}$	234		°C/W
Thermal Resistance Junction-to-Solder Pad	$R_{\Theta JSP}$	80		°C/W
Total Power Dissipation @ T_A = +25 °C (1) @ T_{SP} = +25 °C (2)	P_T	0.75 2		W

Notes: 1. Derate linearly 4.29 mW/°C for T_A > +25°C
2. Derate linearly 12.5 mW/°C for T_{SP} > +25 °C



UA Package

Also available in:

TO-5 package
(long-leaded)
2N5415 – 2N5416

TO-39 (TO-205AD) package
(short-leaded)
2N5415S – 2N5416S

U4 package
(surface mount)
2N5415U4 – 2N5416U4

MSC – Lawrence
6 Lake Street,
Lawrence, MA 01841
Tel: 1-800-446-1158 or
(978) 620-2600
Fax: (978) 689-0803

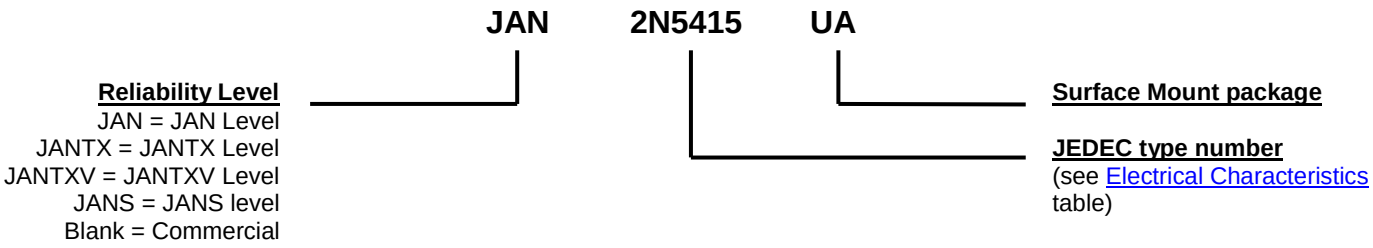
MSC – Ireland
Gort Road Business Park,
Ennis, Co. Clare, Ireland
Tel: +353 (0) 65 6840044
Fax: +353 (0) 65 6822298

Website:
www.microsemi.com

MECHANICAL and PACKAGING

- CASE: Hermetically sealed ceramic package
- TERMINALS: Gold plate over nickel
- MARKING: Manufacturer's ID, date code, part number
- POLARITY: PNP (see package outline)
- TAPE & REEL option: Per EIA-481 (consult factory for quantities)
- WEIGHT: Approximately 0.12 grams
- See Package Dimensions on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
C_{obo}	Common-base open-circuit output capacitance
I_{CEO}	Collector cutoff current, base open
I_{CEX}	Collector cutoff current, circuit between base and emitter
I_{EBO}	Emitter cutoff current, collector open
h_{FE}	Common-emitter static forward current transfer ratio
V_{CEO}	Collector-emitter voltage, base open
V_{CBO}	Collector-emitter voltage, emitter open
V_{EBO}	Emitter-base voltage, collector open

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted

OFF CHARACTERISTICS

Parameters / Test Conditions		Symbol	Min.	Max.	Unit
Collector-Emitter Breakdown Voltage I_C = 50 mA, I_B = 5 mA, L = 25 mH; f = 30 – 60 Hz	2N5415UA 2N5416UA	$V_{(BR)CEO}$	200 300		V
Emitter-Base Cutoff Current V_{EB} = 6.0 V		I_{EBO}		20	µA
Collector-Emitter Cutoff Current V_{CE} = 200 V, V_{BE} = 1.5 V V_{CE} = 300 V, V_{BE} = 1.5 V	2N5415UA 2N5416UA	I_{CEX}		50	µA
Collector-Emitter Cutoff Current V_{CE} = 150 V V_{CE} = 250 V	2N5415UA 2N5416UA	I_{CEO1}		50	µA
Collector-Emitter Cutoff Current V_{CE} = 200 V V_{CE} = 300 V	2N5415UA 2N5416UA	I_{CEO2}		1	mA
Collector-Base Cutoff Current V_{CB} = 175 V V_{CB} = 280 V	2N5415UA 2N5416UA	I_{CBO1}		50	µA
V_{CB} = 200 V V_{CB} = 350 V	2N5415UA 2N5416UA	I_{CBO2}		500	µA
V_{CB} = 175 V, T_A = +150 ºC V_{CB} = 280 V, T_A = +150 ºC	2N5415UA 2N5416UA	I_{CBO3}		1	mA

ON CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Forward-Current Transfer Ratio I_C = 50 mA, V_{CE} = 10 V I_C = 1 mA, V_{CE} = 10 V I_C = 50 mA, V_{CE} = 10 V, T_A = +150 ºC	h_{FE}	30 15 15	120	
Collector-Emitter Saturation Voltage I_C = 50 mA, I_B = 5 mA	$V_{CE(sat)}$		2.0	V
Base-Emitter Voltage Non-Saturation I_C = 50 mA, V_{CE} = 10 V	V_{BE}		1.5	V

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio I_C = 10 mA, V_{CE} = 10 V, f = 5 MHz	$\|h_{fe}\|$	3	15	
Small-signal short Circuit Forward-Current Transfer Ratio I_C = 5 mA, V_{CE} = 10 V, f ≤ 1 kHz	h_{fe}	25		
Output Capacitance V_{CB} = 10 V, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}		15	pF

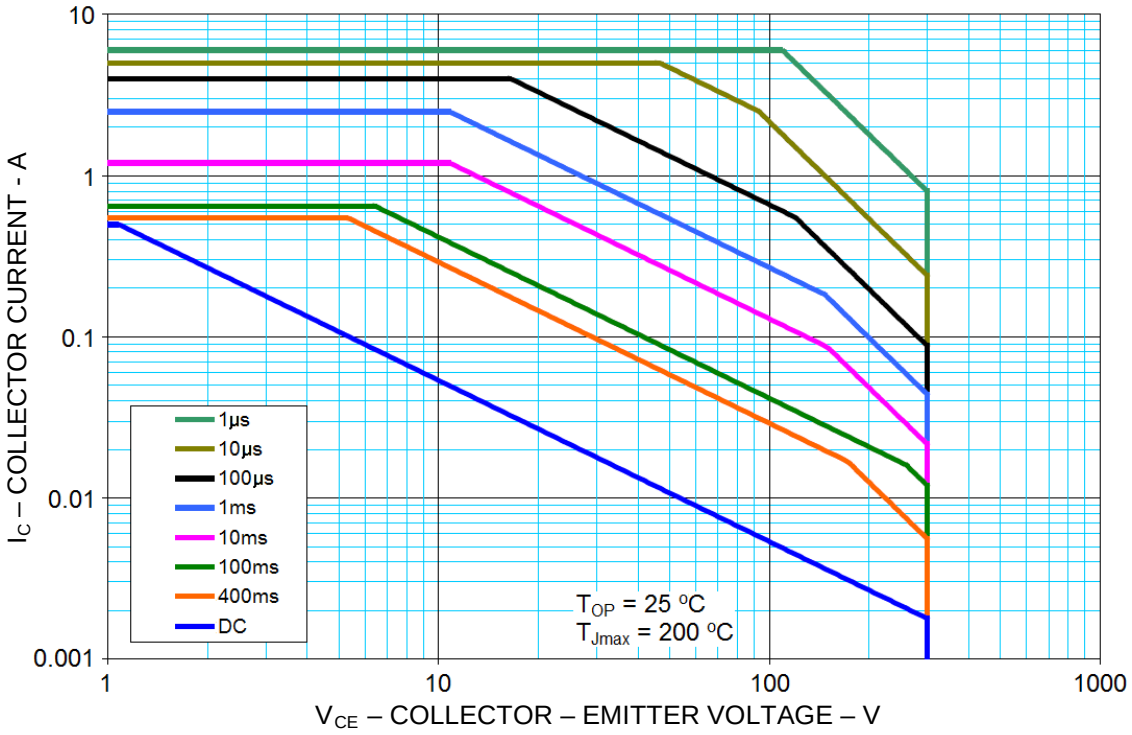
ELECTRICAL CHARACTERISTICS @ T_A = +25 °C unless otherwise noted. (continued)

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time V_{CC} = 200 V, I_C = 50 mA, I_{B1} = 5 mA	t_{on}		1	µs
Turn-Off Time V_{CC} = 200 V, I_C = 50 mA, I_{B1} = I_{B2} = 5 mA	t_{off}		10	µs

SAFE OPERATING AREA (See SOA graph below and MIL-STD-750, method 3053)

DC Tests
T_C = +25 °C, t_P = 0.4 s, 1 Cycle
Test 1
V_{CE} = 10 V, I_C = 0.3 A
Test 2
V_{CE} = 100 V, I_C = 30 mA
Test 3 (2N5415UA only)
V_{CE} = 200 V, I_C = 12 mA
Test 4 (2N5416UA only)
V_{CE} = 300 V, I_C = 5 mA



Maximum Safe Operating Area (T_J = 200 ºC)

GRAPHS

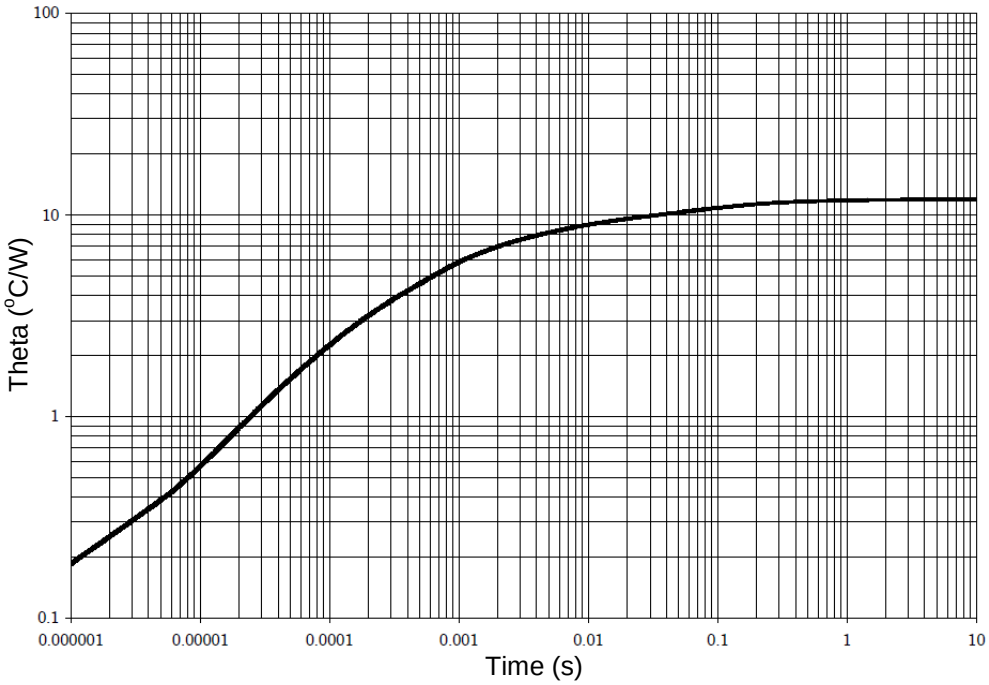
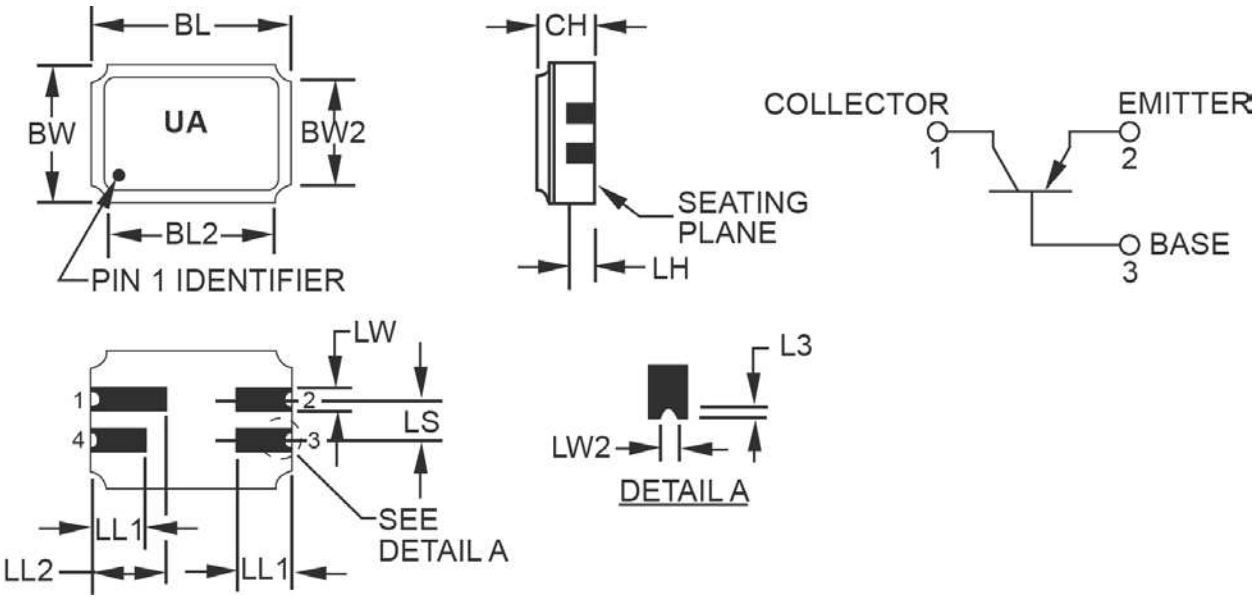


FIGURE 1
Thermal impedance graph ($R_{\Theta JA}$)

PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of 0.010 inch (0.254 mm) and a maximum of 0.040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions " LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension " LW2" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed 0.006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	0.215	0.225	5.46	5.71	
BL2	-	0.225	-	5.71	
BW	0.145	0.155	3.68	3.93	
BW2	-	0.155	-	3.93	
CH	0.061	0.075	1.55	1.90	3
L3	0.003	0.007	0.08	0.18	5
LH	0.029	0.042	0.74	1.07	
LL1	0.032	0.048	0.81	1.22	
LL2	0.072	0.088	1.83	2.23	
LS	0.045	0.055	1.14	1.39	
LW	0.022	0.028	0.56	0.71	
LW2	0.006	0.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C