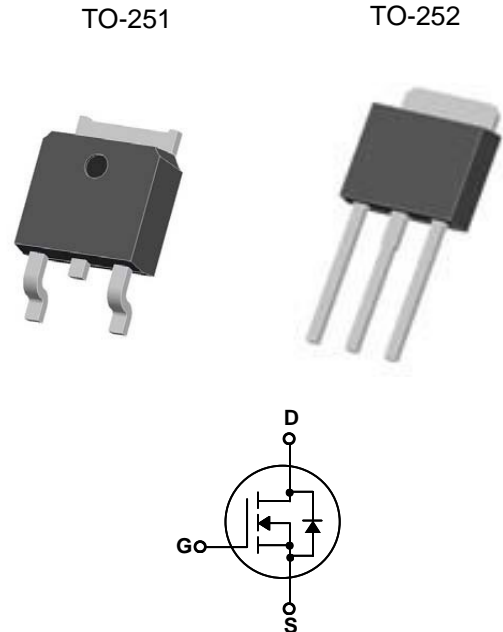# KSMD2N60C / KSMU2N60C

600V N-Channel MOSFET

Features

- 1.9A, 600V, $R_{DS(on)}$ = 4.7Ω @V_{GS} = 10 V
- Low gate charge (typical 8.5 nC)
- Low Crss (typical 4.3 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

General Description

These N-Channel enhancement mode power field effect transistors are produced using Kersemi proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

TO-251   TO-252

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		KSMD2N60C / KSMU2N60C	Units
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous (T_C = 25°C)		1.9	A
	- Continuous (T_C = 100°C)		1.14	A
I_{DM}	Drain Current - Pulsed	(Note 1)	7.6	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I_{AR}	Avalanche Current	(Note 1)	1.9	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)*		2.5	W
	Power Dissipation (T_C = 25°C)		44	W
	- Derate above 25°C		0.35	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.87	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ μA	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250$ μA, Referenced to 25°C	--	0.6	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600$ V, $V_{GS} = 0$ V	--	--	1	μA
		$V_{DS} = 480$ V, $T_C = 125°C$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 0.95$ A	--	3.6	4.7	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40$ V, $I_D = 0.95$ A (Note 4)	--	5.0	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	180	235	pF
C_{oss}	Output Capacitance		--	20	25	pF
C_{rss}	Reverse Transfer Capacitance		--	4.3	3	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300$ V, $I_D = 2$ A, $R_G = 25$ Ω	--	9	28	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	24	58	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	28	66	ns
Q_g	Total Gate Charge	$V_{DS} = 480$ V, $I_D = 2$ A, $V_{GS} = 10$ V	--	8.5	12	nC
Q_{gs}	Gate-Source Charge		--	1.3	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	4.1	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	7.6	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 1.9$ A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 2$ A,	--	230	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F / dt = 100$ A/μs (Note 4)	--	1.0	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 56mH, $I_{AS} = 2$A, $V_{DD} = 50$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 2$A, di/dt ≤ 200A/μs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

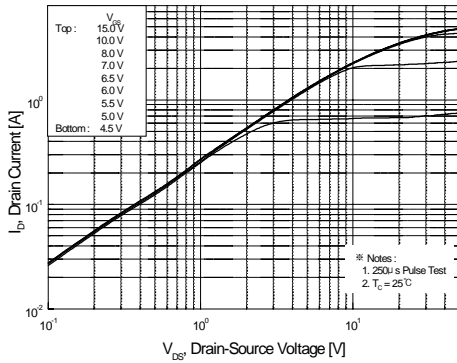## Typical Characteristics

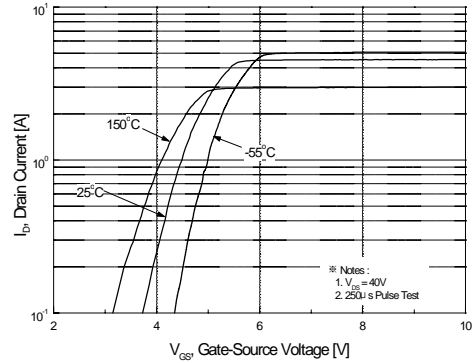Figure 1. On-Region Characteristics
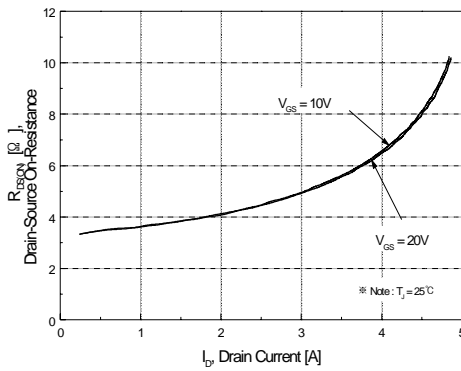

Figure 2. Transfer Characteristics

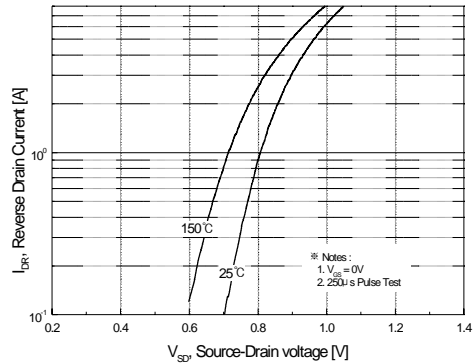Figure 3. On-Resistance Variation vs
Drain Current and Gate Voltage

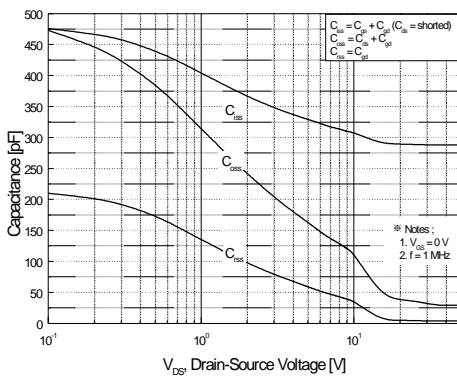Figure 4. Body Diode Forward Voltage
Variation with Source Current
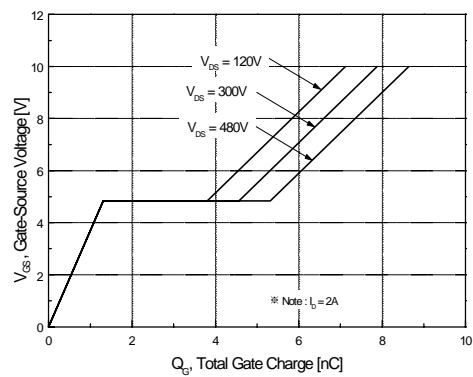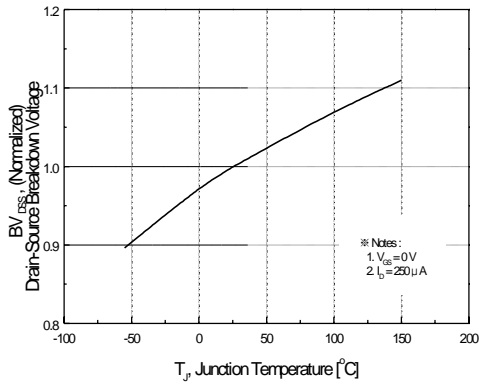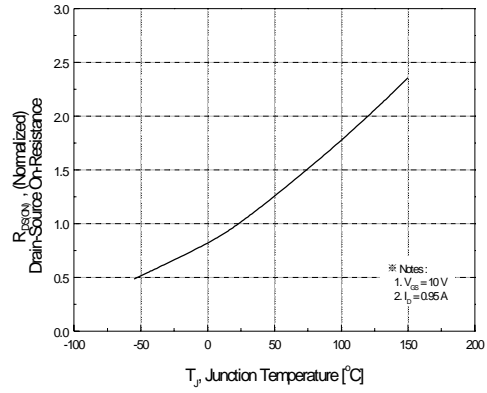and Temperature

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation
vs Temperature**

**Figure 8. On-Resistance Variation
vs Temperature**
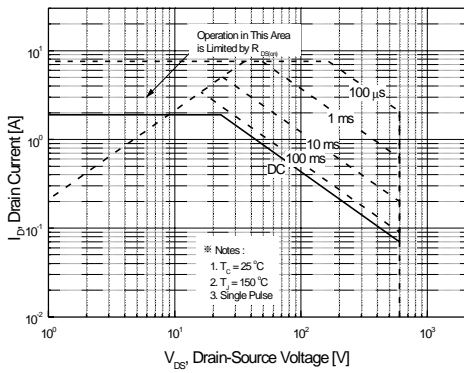
Figure 9. Maximum Safe Operating Area
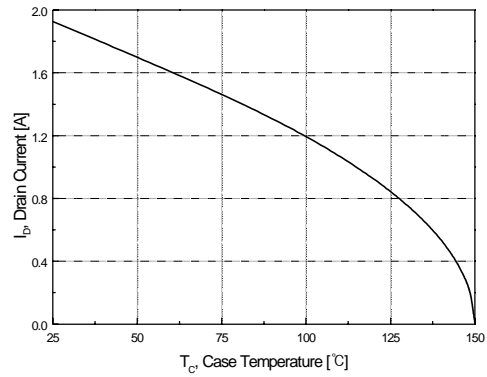
**Figure 10. Maximum Drain Current
vs Case Temperature**
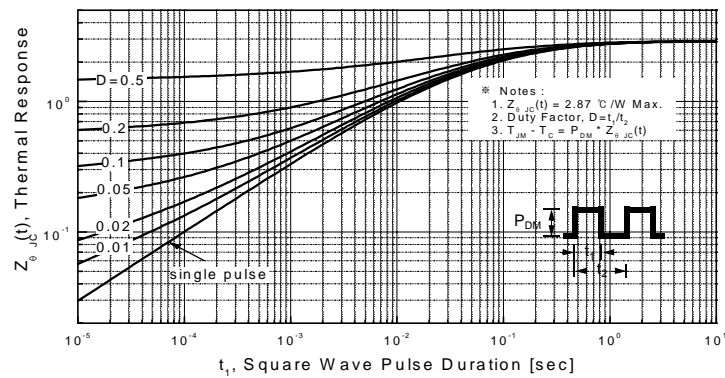
Figure 11. Transient Thermal Response Curve

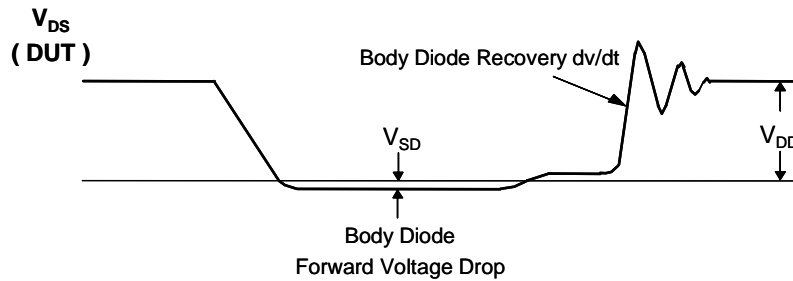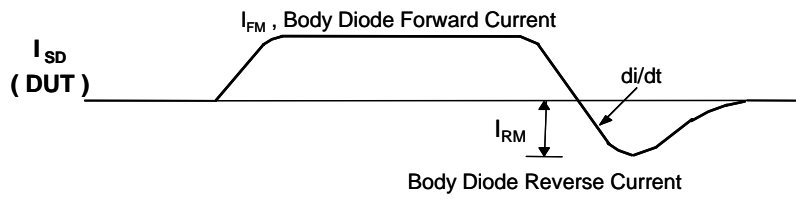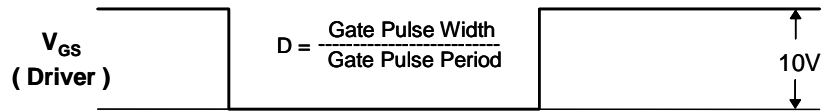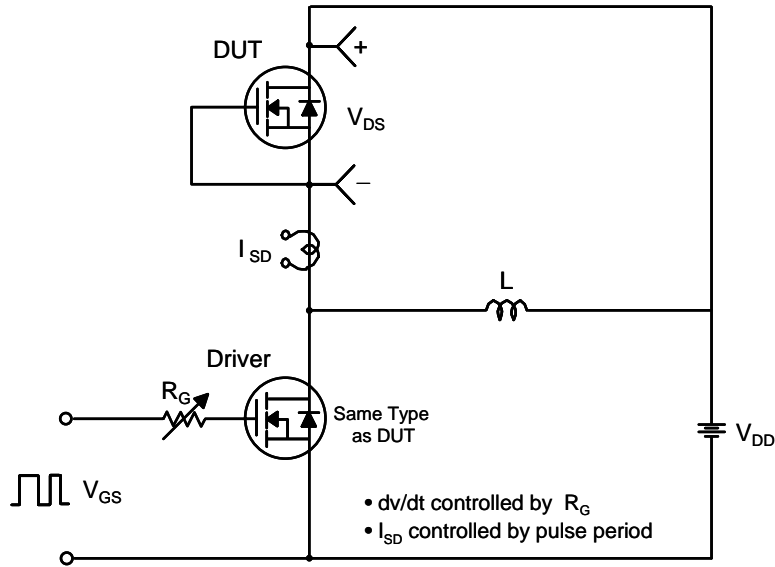**Gate Charge Test Circuit & Waveform**

Same Type as DUT

V_{GS}

DUT

3mA

12V

200nF

50KΩ

300nF

V_{DS}

V_{GS}

10V

Q_g

Q_{gs}

Q_{gd}

Charge

Resistive Switching Test Circuit & Waveforms

V_{DS}

V_{GS}

R_G

R_L

V_{DD}

10V

DUT

V_{DS}

90%

V_{GS}

10%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
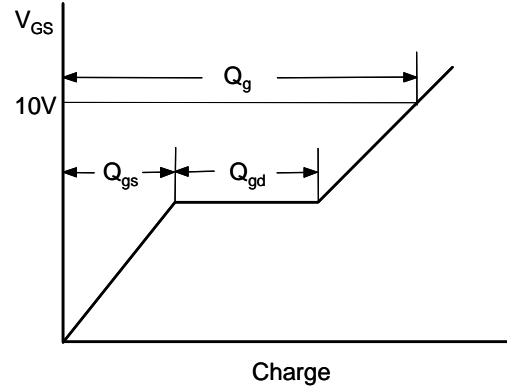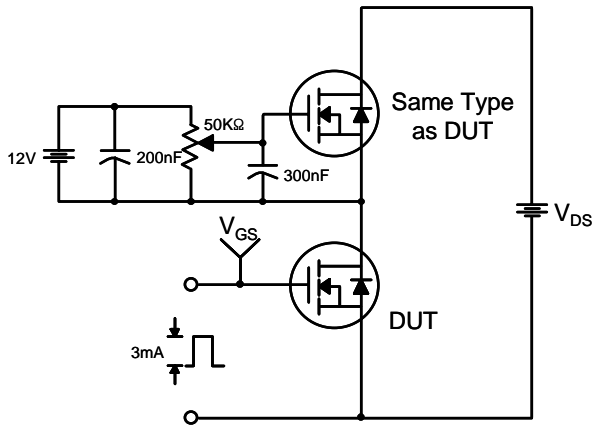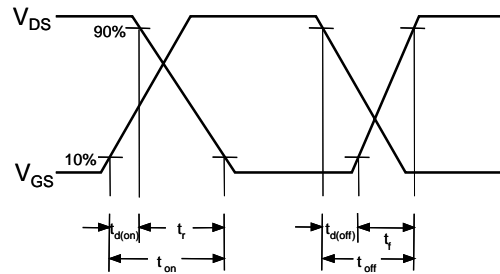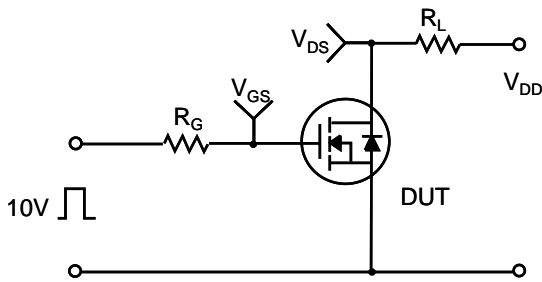
Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS}

L

I_D

R_G

V_{DD}

10V

t_p

DUT

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D(t)$

V_{DD}

$V_{DS}(t)$

t_p

Time
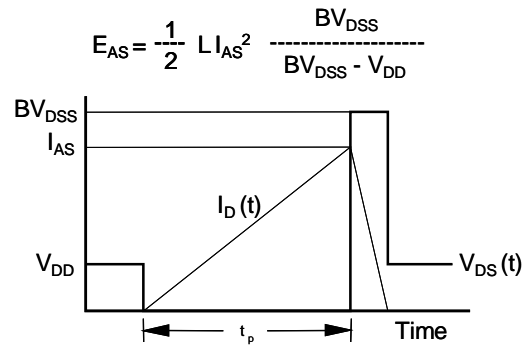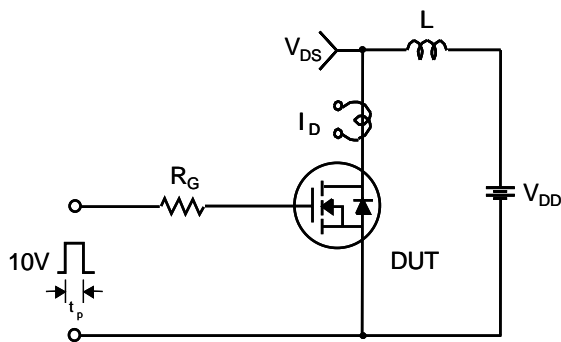
Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type as DUT

V_{GS}

V_{DD}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS} (Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD} (DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS} (DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

D-PAK
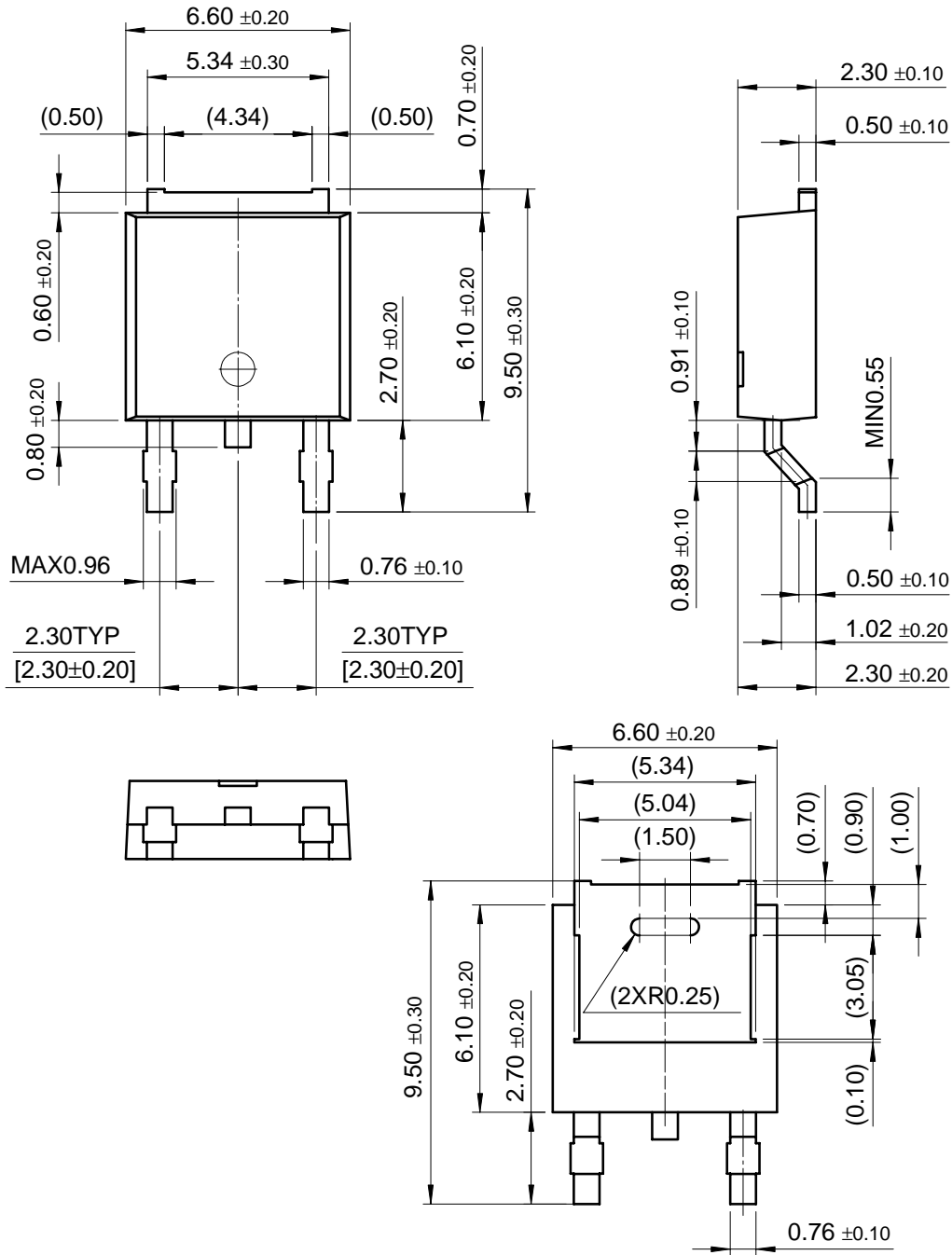
Package Dimensions (Continued)

I-PAK