

MMF80R650P

800V 0.65Ω N-channel MOSFET

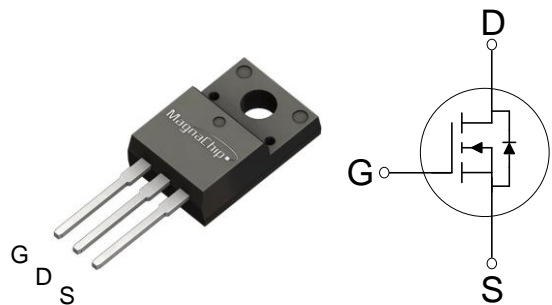
■ Description

MMF80R650P is power MOSFET using magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

■ Key Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	850	V
$R_{DS(on),max}$	0.65	Ω
$V_{TH,typ}$	3	V
I_D	8	A
$Q_{g,typ}$	25.8	nC

■ Package & Internal Circuit



■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

■ Applications

- PFC Power Supply Stages
- Switching Applications
- Adapter
- Motor Control
- DC – DC Converters

■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMF80R650PTH	80R650P	-55 ~ 150°C	TO-220F	Tube	Halogen Free

■ Absolute Maximum Rating (T_c=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	V _{DSS}	800	V	
Gate – Source voltage	V _{GSS}	±30	V	
Continuous drain current ⁽¹⁾	I _D	8	A	T _C =25°C
		5.05	A	T _C =100°C
Pulsed drain current ⁽²⁾	I _{DM}	24	A	
Power dissipation	P _D	32	W	
Single - pulse avalanche energy	E _{AS}	340	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness ⁽³⁾	dv/dt	15	V/ns	
Isolation withstand voltage for TO-220F	V _{ISO}	4500	V	V _{DC} , t=0.3s, T _C =25°C
Storage temperature	T _{stg}	-55 ~150	°C	
Maximum operating junction temperature	T _j	150	°C	

- 1) I_D limited by maximum junction temperature.
- 2) Pulse width t_p limited by T_{j,max}
- 3) I_{SD} ≤ I_D, V_{DS peak} ≤ V_{(BR)DSS}

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R _{thjc}	3.9	°C/W
Thermal resistance, junction-ambient max	R _{thja}	62.5	°C/W

■ Static Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS} = 0V, I_D=0.25mA$
Gate Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D=0.25mA$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 800V, V_{GS} = 0V$
Gate Leakage Current	I_{GSS}	-	-	100	nA	$V_{GS} = \pm 30V, V_{DS} = 0V$
Drain-Source On State Resistance	$R_{DS(ON)}$	-	0.56	0.65	Ω	$V_{GS} = 10V, I_D = 5.1A$

■ Dynamic Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{iss}	-	823	-	pF	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$
Output Capacitance	C_{oss}	-	689	-		
Reverse Transfer Capacitance	C_{rss}	-	29	-		
Effective Output Capacitance Energy Related ⁽⁴⁾	$C_{o(er)}$	-	23.7	-		$V_{DS} = 0V \text{ to } 640V, V_{GS} = 0V, f = 1.0MHz$
Turn On Delay Time	$t_{d(on)}$	-	15.2	-	ns	$V_{GS} = 10V, R_G = 25\Omega, V_{DS} = 400V, I_D = 8.0A$
Rise Time	t_r	-	29.6	-		
Turn Off Delay Time	$t_{d(off)}$	-	76.4	-		
Fall Time	t_f	-	28.0	-		
Total Gate Charge	Q_g	-	25.8	-	nC	$V_{GS} = 10V, V_{DS} = 640V, I_D = 8.0A$
Gate – Source Charge	Q_{gs}	-	5.0	-		
Gate – Drain Charge	Q_{gd}	-	11.1	-		
Gate Resistance	R_G	-	2.25	-	Ω	$V_{GS} = 0V, f = 1.0MHz$

4) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	I_{SD}	-	-	8	A	
Diode Forward Voltage	V_{SD}	-	-	1.4	V	$I_{SD} = 8.0\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}	-	354	-	ns	$I_{SD} = 8.0\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$
Reverse Recovery Charge	Q_{rr}	-	3.7	-	μC	
Reverse Recovery Current	I_{rrm}	-	20.9	-	A	

■ Characteristic Graph

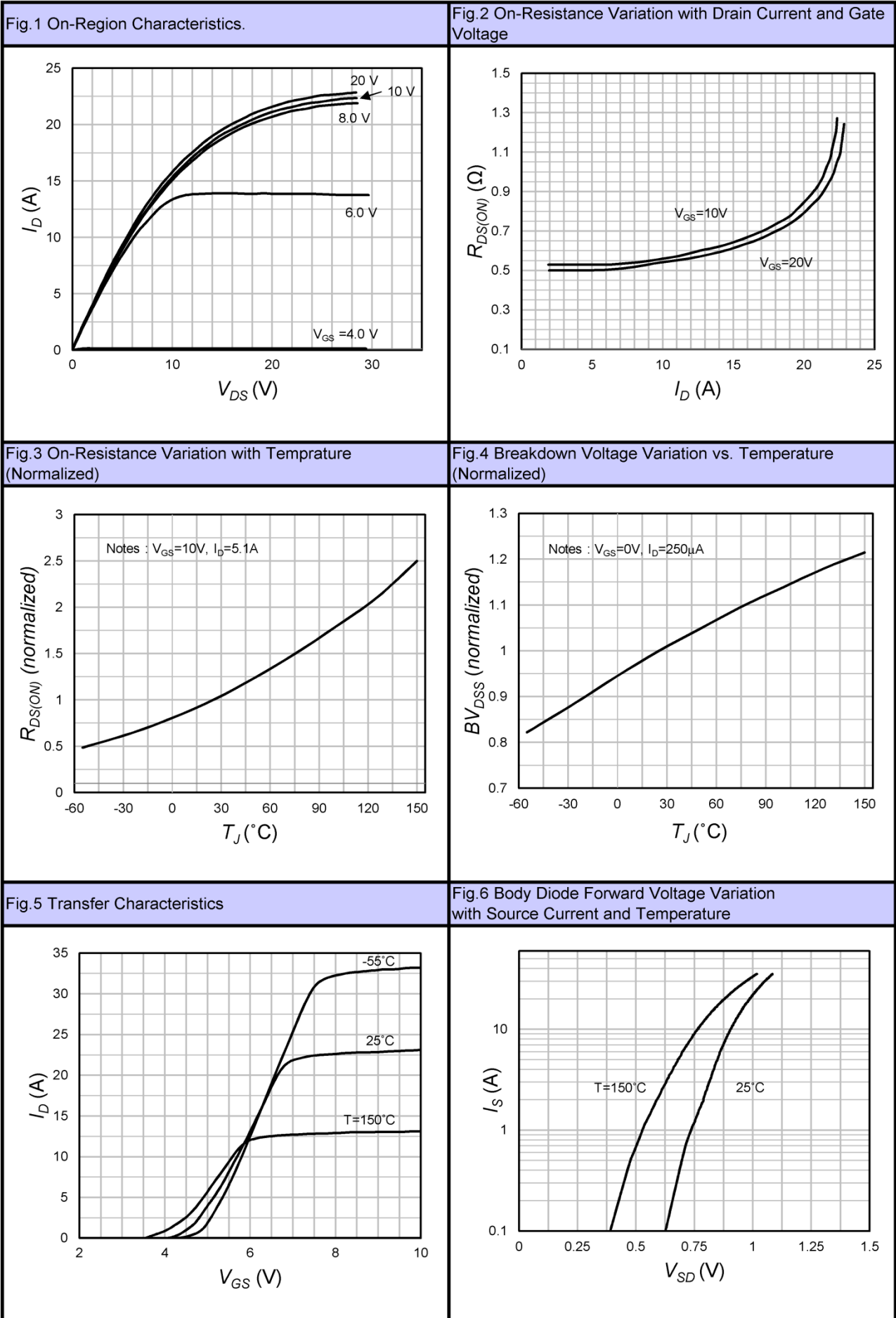


Fig.7 Gate Charge Characteristics

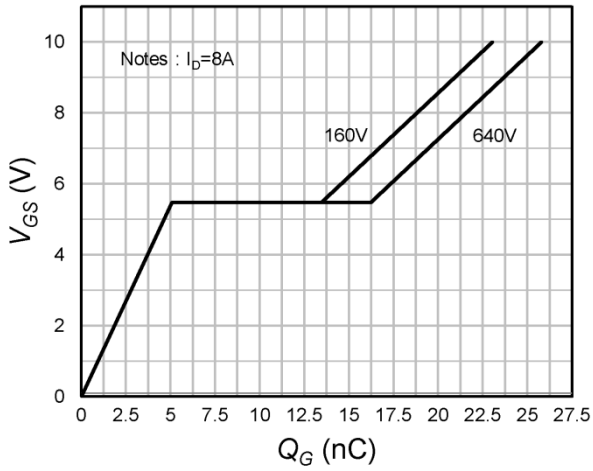


Fig.8 Capacitance Characteristics

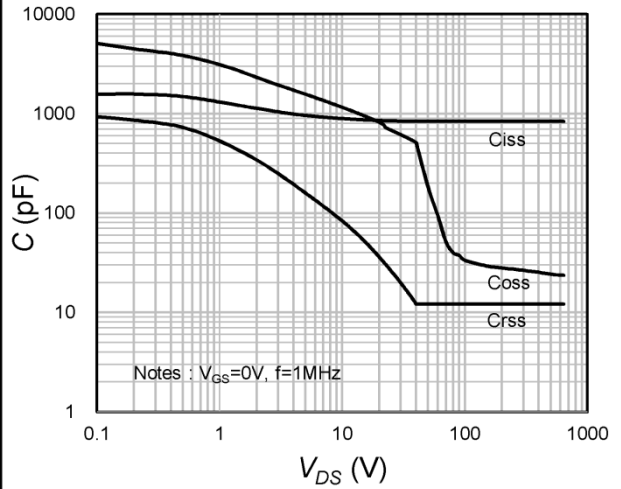


Fig.9 $V_{GS(th)}$ Variation with Temperature (Normalized)

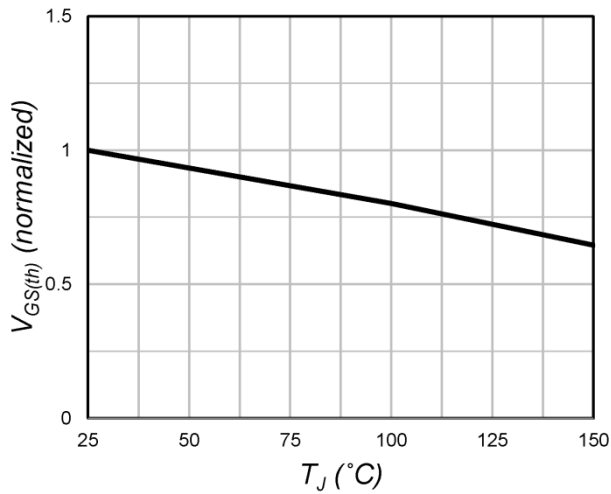


Fig.10 Maximum Drain Current vs. Case Temperature

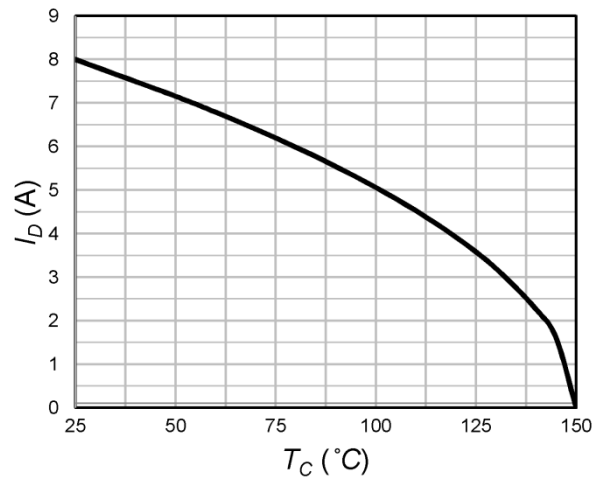


Fig.11 Single Pulse Maximum Power Dissipation

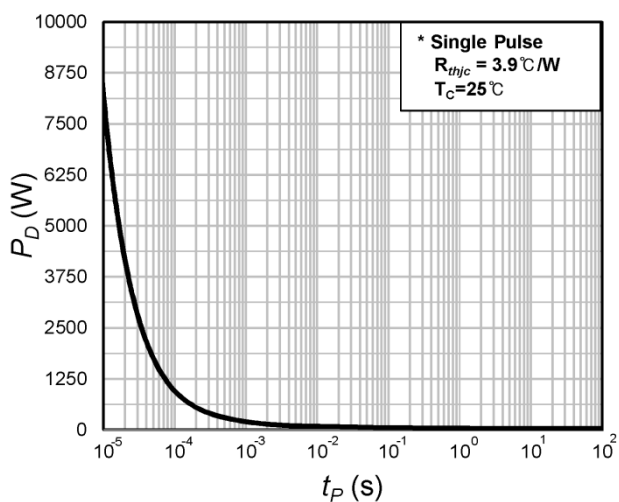


Fig.12 Output Capacitance Stored Energy

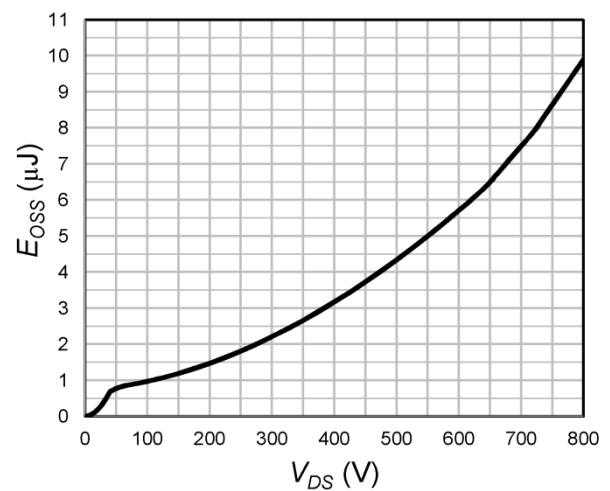


Fig.13 Transient Thermal Response Curve

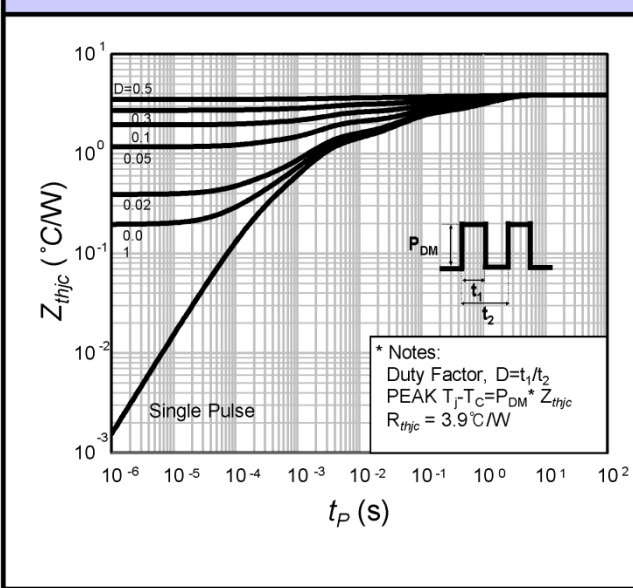
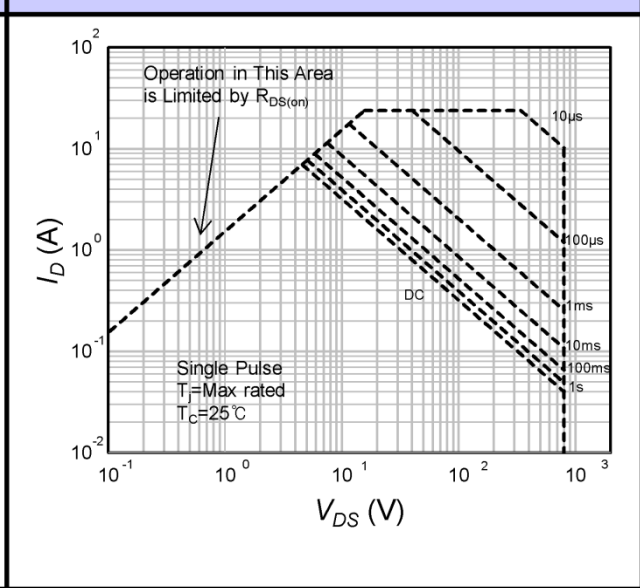


Fig.14 Maximum Safe Operating Area



■ Test Circuit

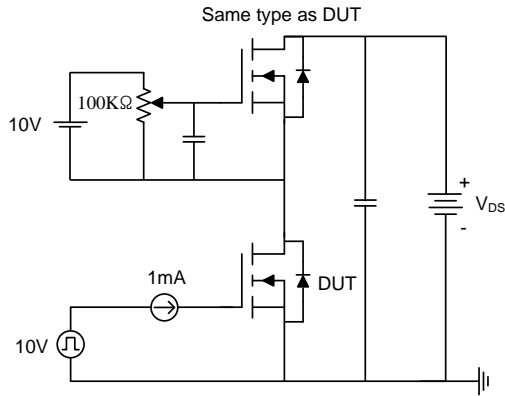


Fig15-1. Gate charge measurement circuit

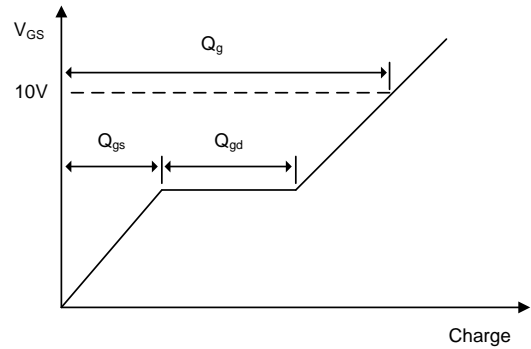


Fig15-2. Gate charge waveform

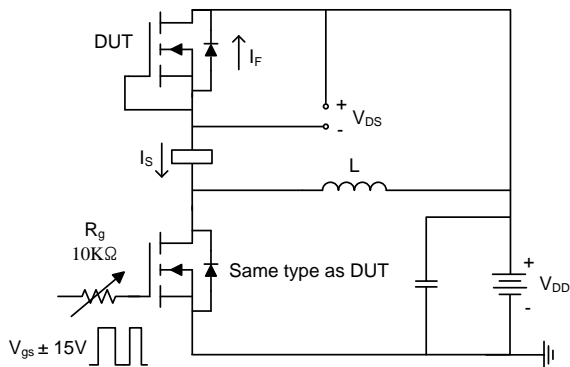


Fig16-1. Diode reverse recovery test circuit

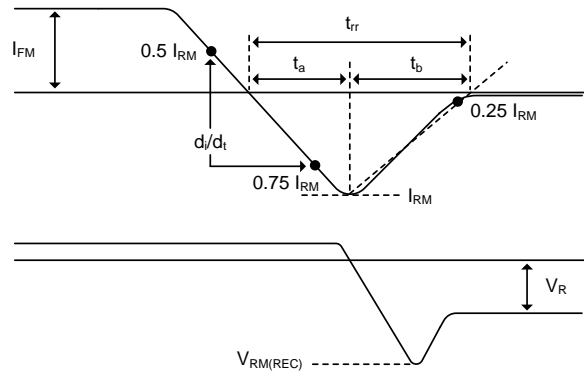


Fig16-1. Diode reverse recovery test waveform

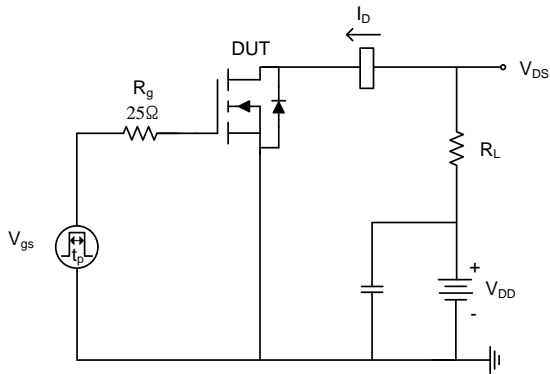


Fig17-1. Switching time test circuit for resistive load

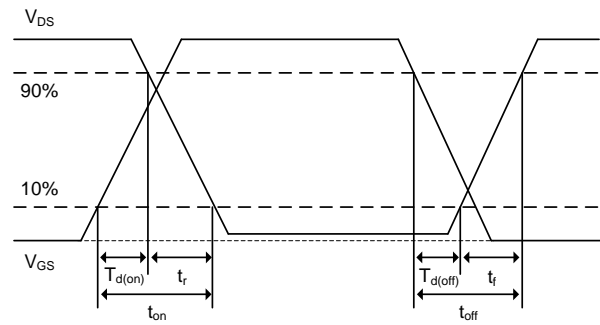


Fig17-2. Switching time waveform

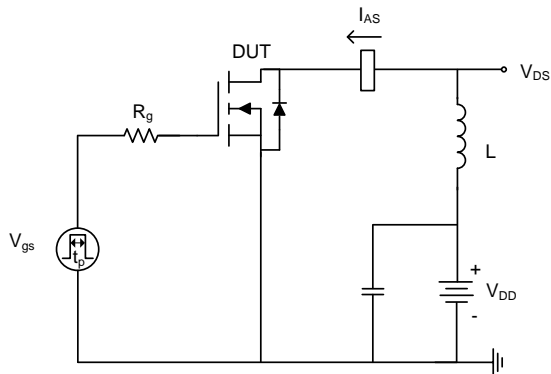


Fig18-1. Unclamped inductive load test circuit

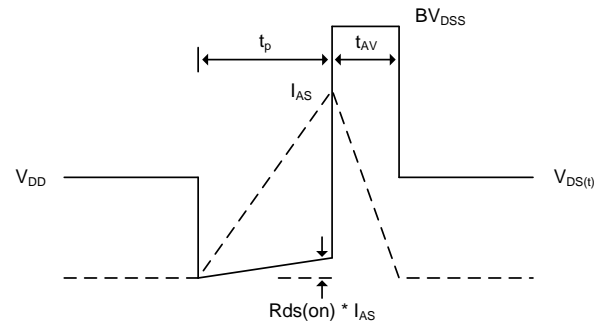
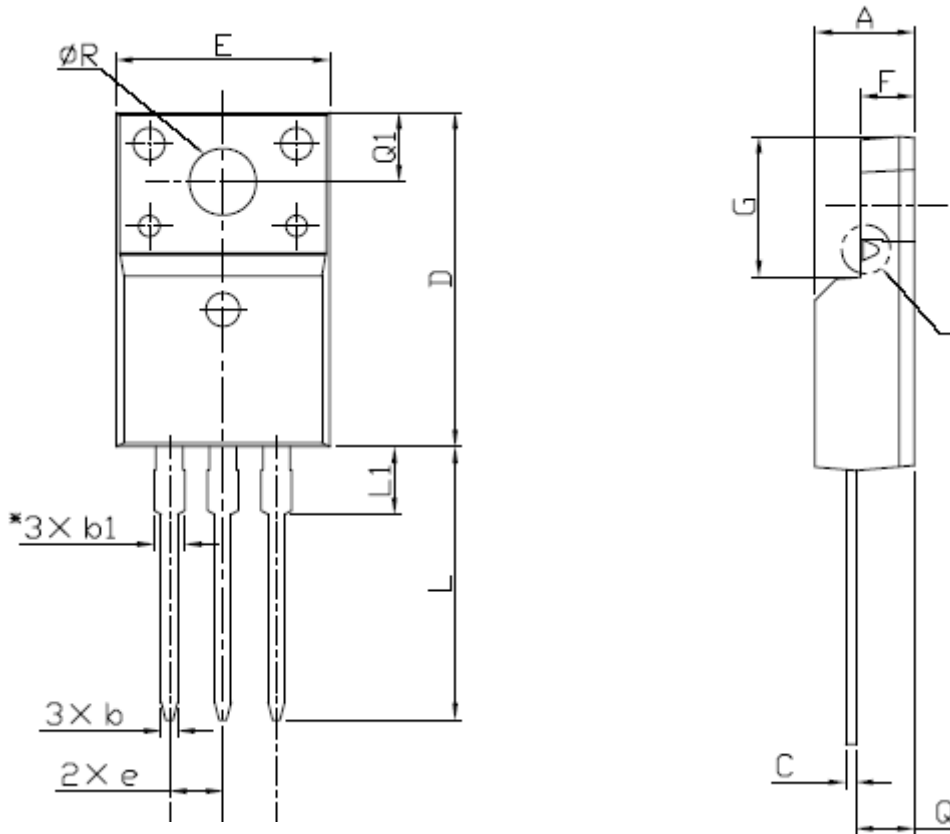


Fig18-2. Unclamped inductive waveform

Physical Dimension
3 Leads, TO-220F

Dimensions are in millimeters unless otherwise specified



Symbol	Min	Nom	Max
A	4.50		4.93
b	0.63		0.91
b1	1.15		1.47
C	0.33		0.63
D	15.47		16.13
E	9.60		10.71
e		2.54	
F	2.34		2.84
G	6.48		6.90
L	12.24		13.72
L1	2.79		3.67
Q	2.52		2.96
Q1	3.10		3.50
ϕR	3.00		3.55

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

MagnaChip reserves the right to change the specifications and circuitry without notice at any time. MagnaChip does not consider responsibility for use of any circuitry other than circuitry entirely included in a MagnaChip product. [MagnaChip](#) is a registered trademark of MagnaChip Semiconductor Ltd.