LF48410
1024 x 24-bit Video Histogrammer

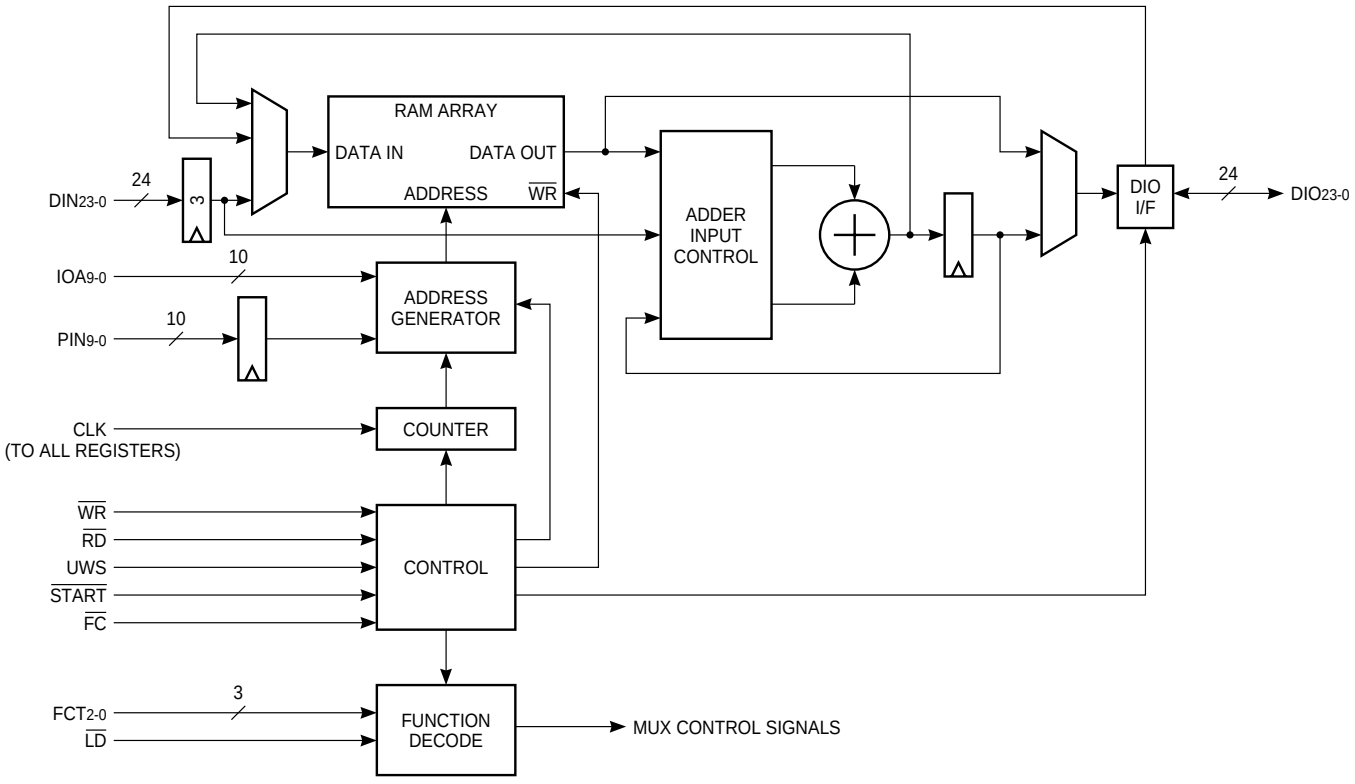
FEATURES

- 40 MHz Data Input and Computation Rate
- 1024 x 24-bit Memory Array
- Histograms of Images up to 4K x 4K with 10-bit Pixel Resolution
- Memory Array Flash Clear
- User-Programmable Modes: Histogram, Histogram Accumulate, Look Up Table, Bin Accumulate, Delay Memory, Delay and Subtract, Single Port RAM
- Replaces Harris HSP48410
- 84-pin PLCC, J-Lead

DESCRIPTION

The **LF48410** is capable of generating histograms and Cumulative Distribution Functions of video images. It may also be used as a look up table, a bin accumulator, a delay memory (delay and subtract also possible), or a single port RAM. The on-chip 1024 x 24-bit memory array facilitates histograms of images up to 4K x 4K pixels with a 10-bit pixel resolution. Once the histogram of a video image is stored in the memory array, the Cumulative Distribution Function can be calculated by putting the device in Histogram Accumulate Mode. Transformation functions can be performed on pixel values when the device is in Look Up Table Mode. If the Cumulative Distribution Function is the desired transformation function, the LF48410 can calculate it and have it available for Look Up Table Mode. When the device is in Delay Memory Mode, it functions as a video row buffer. In this mode, the LF48410 can buffer video lines as long as 1029 pixels. The device can also function as an asynchronous single port RAM. During asynchronous modes, the device can be configured as a 1024 x 24, 1024 x 16, or 1024 x 8-bit RAM. A Flash Clear function is provided which sets all memory array locations and data path registers to "0".

LF48410 Block Diagram



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

When operating in a synchronous mode, the rising edge of CLK strobes all enabled registers. CLK has no effect when operating in an asynchronous mode.

Inputs

PIN9-0 — Pixel Data Input

PIN9-0 provides address information to the memory array in Histogram, Bin Accumulate, and Look Up Table Modes. Data is latched on the rising edge of CLK.

DIN23-0 — Data Input

In Bin Accumulate Mode, DIN23-0 provides data to the internal summer to be added to data already in the memory array. In Look Up Table Mode, DIN23-0 is used to load the memory array with the desired values. In Delay Memory Mode, the data to be delayed is input to the memory array using DIN23-0, and in Delay and Subtract Mode it also provides data to be subtracted from the delayed data. In all four modes, DIN23-0 is latched on the rising edge of CLK.

IOA9-0 — Asynchronous Address Input

IOA9-0 provides address information to the memory array in Asynchronous 16 and 24 Modes.

FCT2-0 — Function Input

FCT2-0 is used to put the LF48410 into one of its eight modes of operation (Table 1). Data is latched on the rising edge of $\overline{LD}$. To ensure proper operation of the device, $\overline{START}$ must be HIGH while changing modes, and there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

Inputs/Outputs

DIO23-0 — Data Input/Output

In all synchronous modes, DIO23-0 is the 24-bit registered data output port. In all asynchronous modes, DIO23-0 is both the data input and data output port for the memory array.

Controls

$\overline{START}$ — Device Enable

$\overline{START}$ is used to enable and disable the synchronous modes of operation (except for the Delay Memory and Delay and Subtract Modes). The synchronous mode sections explain how $\overline{START}$ functions in each mode. $\overline{START}$ has no effect in asynchronous modes. Data is latched on the rising edge of CLK. $\overline{START}$ must be held HIGH when changing from one mode to another. To ensure proper operation of the device, there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

$\overline{RD}$ — Read/Output Enable

In all synchronous modes, $\overline{RD}$ is used as an output enable for DIO23-0. When $\overline{RD}$ is LOW, DIO23-0 is enabled for output. When $\overline{RD}$ is HIGH, DIO23-0 is placed in a high-impedance state. In all asynchronous modes, $\overline{RD}$ is used as a read enable for the memory array (see asynchronous mode sections for details).

$\overline{WR}$ — Write Enable

In all asynchronous modes, $\overline{WR}$ is used as a write enable for the memory array (see asynchronous mode sections for details). $\overline{WR}$ has no effect in the synchronous modes.

UWS — Upper Word Select

UWS is only used in Asynchronous 16 Mode. If UWS is LOW and a memory write is performed, data on DIO15-0 is written to the lower 16 bits of the addressed 24-bit word. If UWS is LOW and a memory read is performed, the lower 16 bits of the addressed 24-bit word will be output on DIO15-0. If UWS is HIGH and a memory write is performed, data on DIO7-0 is written to the upper 8 bits of the addressed 24-bit word. If UWS is HIGH and a memory read is performed, the upper 8 bits of the addressed 24-bit word will be output on DIO7-0.

$\overline{FC}$ — Flash Clear

When $\overline{FC}$ is LOW, all memory array locations and data path registers are set to "0". To ensure that Flash Clear functions properly, $\overline{FC}$ should not be set LOW until $\overline{START}$ is HIGH (synchronous modes) or $\overline{WR}$ is HIGH (asynchronous modes).

$\overline{LD}$ — Function Load Strobe

Data present on FCT2-0 is latched into the LF48410 on the rising edge of $\overline{LD}$. To ensure proper operation of the device, there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

TABLE 1. LF48410 MODES

FCT2-0			MODE
0	0	0	Histogram
0	0	1	Histogram Accumulate
0	1	0	Delay and Subtract
0	1	1	Look Up Table
1	0	0	Bin Accumulate
1	0	1	Delay Memory
1	1	0	Asynchronous 24
1	1	1	Asynchronous 16

HISTOGRAM MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 1. The memory array keeps track of how many times a particular pixel value is used in a video image. The pixel value is input on PIN9-0 and is latched on the rising edge of CLK. Data at the address defined by PIN9-0 is read out of the memory array and incremented by one. The data is then written back to the memory array, in the same location it was read from, and is also output on DIO23-0 (if $\overline{RD}$ is LOW). As long as $\overline{START}$ is LOW, the device will be enabled for Histogram Mode. When $\overline{START}$ is HIGH, the device will still read pixel values, but the addres-sed data will not be incremented. The unchanged data is output on DIO23-0 and is not written back to the memory array (writing is disabled). $\overline{START}$ is delayed internally three clock cycles to match the latency of the address generator.

FIGURE 1. HISTOGRAM MODE

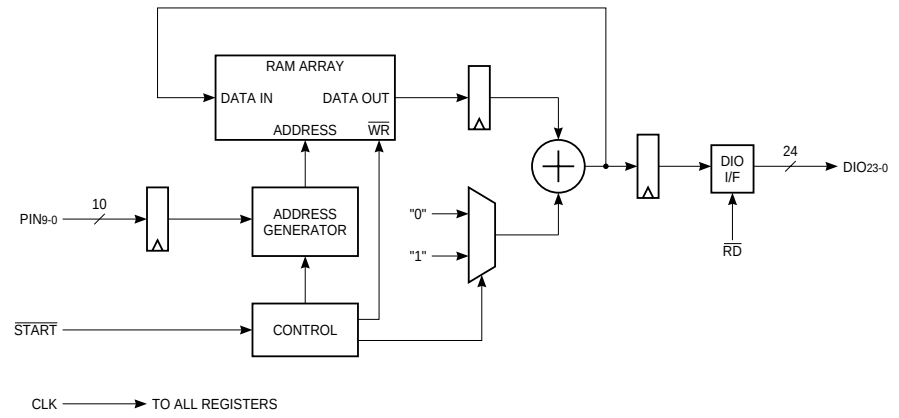
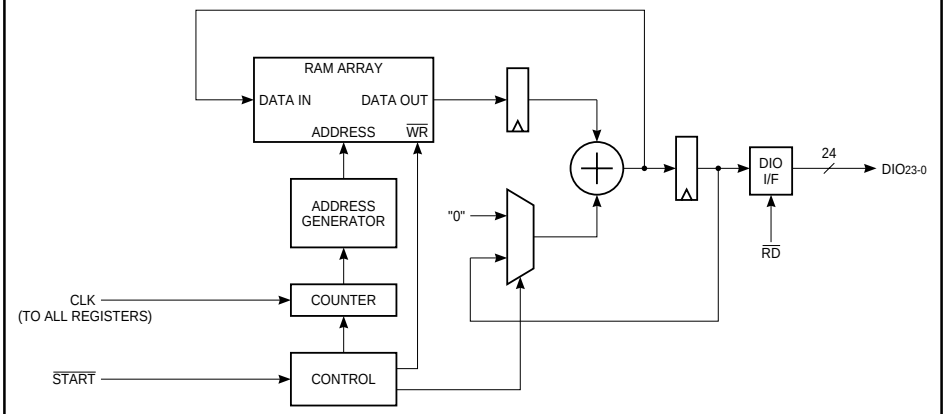


FIGURE 2. HISTOGRAM ACCUMULATE MODE



HISTOGRAM ACCUMULATE MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 2. This mode is used to calculate the Cumulative Distribution Function of a video image. Before this can be done, the histogram of the image must already be in the memory array. The internal counter is used to generate address data for the memory array. Data at the address defined by the counter is read out of the memory array and added to the sum of the data from all previous address locations. This new value is written back to the memory array, in the same location where the last read occurred, and is also output on DIO23-0 (if $\overline{RD}$ is LOW). After all memory locations with histogram data are accumulated, the memory array will contain the Cumulative Distribution Function.

After this mode is selected, the internal counter and all data path registers are reset to zero when $\overline{START}$ is set LOW. Every rising edge of CLK causes the counter to increment its output by one until the counter reaches a value of 1023. At this point, the counter will hold the value of 1023 and writing to the memory array will be disabled. As long as $\overline{START}$ is LOW, the device will be enabled for Histogram Accumulate Mode. When $\overline{START}$ is HIGH, the counter will still increment its address values, but the addressed data will not be added to anything. The unchanged data is output on DIO23-0 and is not written back to the memory array (writing is disabled). $\overline{START}$ is delayed internally three clock cycles to match the latency of the address generator.

LOOK UP TABLE MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 3. This mode is used to perform fixed transformation functions on pixel values. The transformation function can be loaded into the memory array in Look Up Table Write Mode, Asynchronous 16/24 Mode, or Histogram Accumulate Mode. In Look Up Table Write Mode, data is loaded into the memory array using DIN23-0, CLK, and $\overline{START}$. The internal counter is used to generate address data for the memory array. When $\overline{START}$ goes LOW, the counter is reset to zero. As long as $\overline{START}$ is LOW, data on DIN23-0 is latched on the rising edge of CLK and loaded

FIGURE 3. LOOK UP TABLE MODE

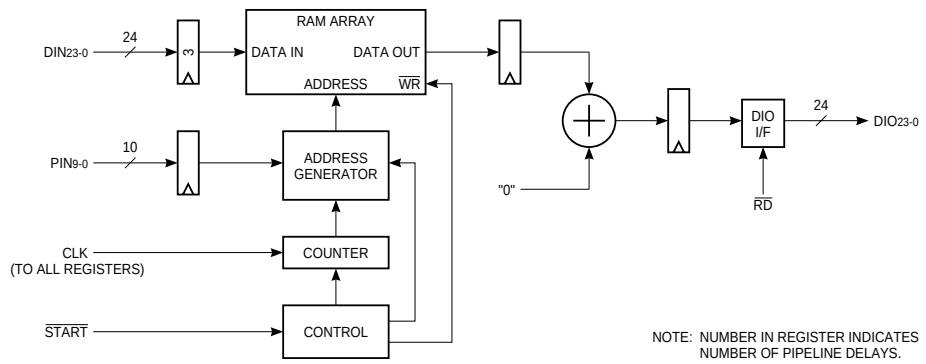
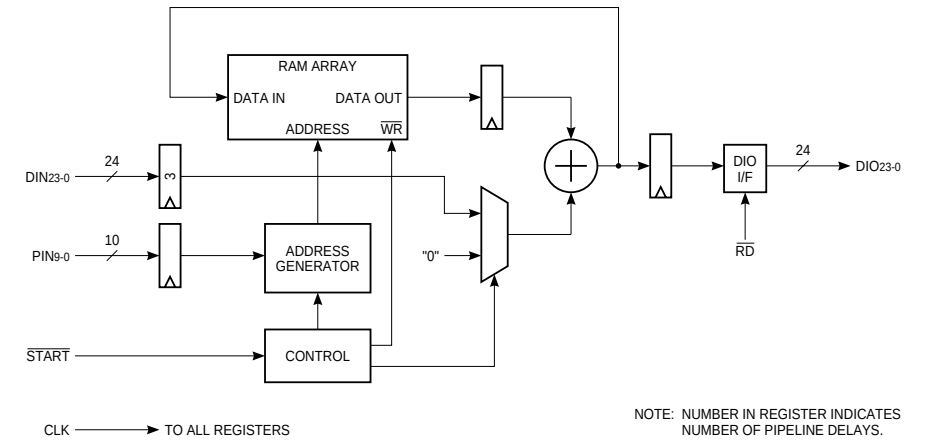


FIGURE 4. BIN ACCUMULATE MODE



into the memory array at the address defined by the counter. The value already in the memory array at that address is output on DIO23-0 (if $\overline{RD}$ is LOW). Every rising edge of CLK causes the counter to increment its output by one until the counter reaches a value of 1023. At this point, the counter will hold the value of 1023 and writing to the memory array will be disabled. DIN23-0 is delayed internally three clock cycles to match the latency of the address generator. In Asynchronous 16/24 Mode, data is loaded into the memory array as detailed in the asynchronous mode sections. If the Cumulative Distribution Function is the desired transformation function, the memory array will contain this data as soon as the Histogram Accumulate function has been completed.

Once the memory array contains the desired data, the device needs to be put in Look Up Table Read Mode by setting $\overline{START}$ HIGH. In Look Up Table Read Mode, pixel values are input on PIN9-0 and are latched on the rising edge of CLK. Data at the address defined by PIN9-0 is read out of the memory array and output on DIO23-0 (if $\overline{RD}$ is LOW). If Look Up Table Write Mode was used to load the memory array, it is important to wait until the third clock cycle after $\overline{START}$ goes HIGH to input data on PIN9-0 to insure that all data is written into the memory array before any reading is done.

BIN ACCUMULATE MODE

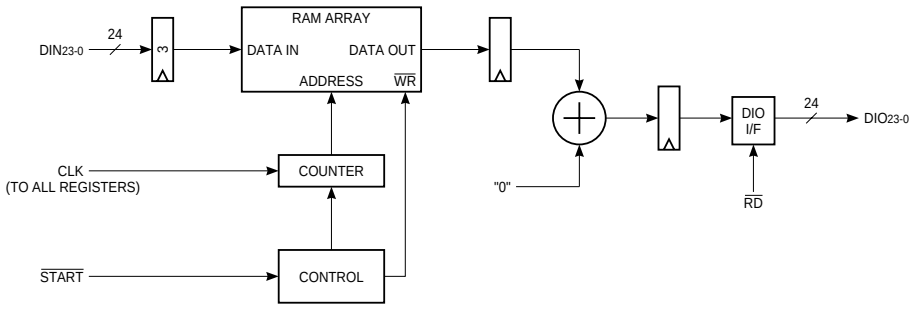
When the LF48410 is in this mode, the chip is configured as shown in Figure 4. PIN9-0 provides address data for the memory array and is latched on the rising edge of CLK. Data at the address defined by PIN9-0 is read out of the memory array and added to the data on DIN23-0. This new value is written back to the memory array, in the same location where the last read occured, and is also output on DIO23-0 (if $\overline{RD}$ is LOW). As long as $\overline{START}$ is LOW, the device will be enabled for Bin Accumulate Mode. When $\overline{START}$ is HIGH, the device will still read address values on PIN9-0, but the addressed data will not be added to anything. The unchanged data will be output on DIO23-0 and is not written back to the memory array (writing is disabled). $\overline{START}$ and DIN23-0 are delayed internally three clock cycles to match the latency of the address generator.

DELAY MEMORY MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 5. This mode allows the device to function as a row buffer. The internal counter is used to generate address data for the memory array. When $\overline{START}$ goes LOW, the counter is reset to zero. Delay length (row length) is determined by reseting the counter every N–4 clock cycles, where N is the number of delays. For

example, to set the number of delays to 10, $\overline{START}$ would have to be set LOW every 6 cycles. The maximum delay length is 1029 and the minimum delay length is 6. Data on DIN23-0 is latched on the rising edge of CLK and loaded into the memory array at the address defined by the counter. Data is output on DIO23-0 (if $\overline{RD}$ is LOW). If the counter reaches the value of 1023, the counter will hold this value and writing to the memory array will be disabled.

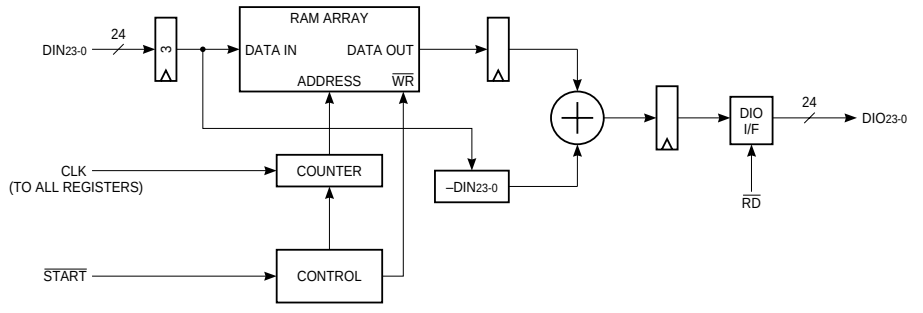
FIGURE 5. DELAY MEMORY MODE



DELAY AND SUBTRACT MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 6. The internal counter is used to generate address data for the memory array. When $\overline{START}$ goes LOW, the counter is reset to zero. Delay length (row length) is determined by reseting the counter every N–4 clock cycles, where N is the number of delays. The maximum delay length is 1029 and the minimum delay length is 6. Data on DIN23-0 is latched on the rising edge of CLK and loaded into the memory array at the address defined by the counter. Data is output on DIO23-0 (if $\overline{RD}$ is LOW). Before data read from the memory array is output to DIO23-0, input data is subtracted from it according to the following formula: $OUT_C = D_{(C-N+1)} - D_{(C-3)}$. OUT_C is the data sent to the output port (DIO23-0) on clock cycle C. $D_{(C-N+1)}$ is the data latched into the device on clock cycle C–N+1, and $D_{(C-3)}$ is the data latched into the device on clock cycle C–3. N is the number of delays. For example, to determine what will be output on DIO23-0 on clock cycle 12 when the device is set for 10 delays, set C=12 and N=10 to obtain: $OUT_{12} = D_3 - D_9$. If the counter reaches the value of 1023, the counter will hold this value and writing to the memory array will be disabled.

FIGURE 6. DELAY AND SUBTRACT MODE



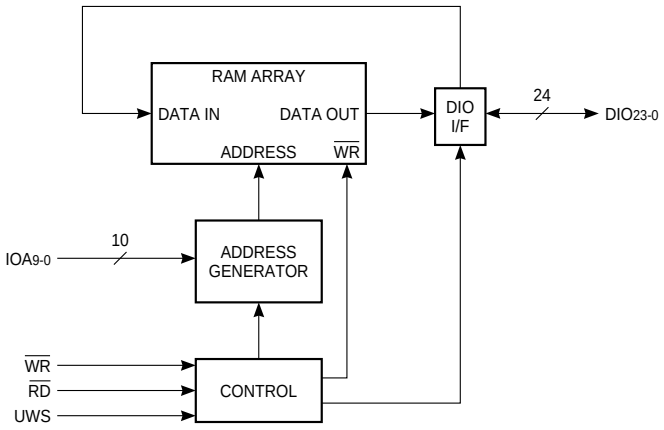
ASYNCHRONOUS 16 MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 7. This mode allows the device to function as an asynchronous single port RAM. Each 24-bit memory location is split into two parts, the lower 16 bits and the upper 8 bits. IOA9-0 addresses the 24-bit memory locations, and UWS addresses the lower 16 or upper 8 bits of those locations. If UWS is LOW, the lower 16 bits of the 24-bit memory location are addressed. If UWS is HIGH, the upper 8 bits are addressed. Address data on IOA9-0 and UWS is latched into the device on the falling edge of $\overline{RD}$ or $\overline{WR}$. If $\overline{RD}$ latches the address data, a memory read is performed. Data at the specified address is output on DIO15-0 (if UWS was latched LOW) or DIO7-0 (if UWS was latched HIGH). If UWS was latched LOW/HIGH, DIO16-23/DIO8-23 will output zeros during a memory read. If $\overline{WR}$ latches the address data, a memory write is performed. After the falling edge of $\overline{WR}$ latches the address, data on DIO15-0 (if UWS was latched LOW) or DIO7-0 (if UWS was latched HIGH) is written to the RAM on the rising edge of $\overline{WR}$.

ASYNCHRONOUS 24 MODE

When the LF48410 is in this mode, the chip is configured as shown in Figure 7. In this mode, the device functions the same as when in Asynchronous 16 Mode except that the 24-bit memory locations are not split into two parts. All 24 bits are used during a read or write operation. When reading, data is output on DIO23-0. When writing, data is input on DIO23-0. UWS is not used in this mode.

FIGURE 7. ASYNCHRONOUS 16/24 MODE



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to VCC + 0.5 V
Signal applied to high impedance output	–0.5 V to VCC + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ **V**CC ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	**V**CC = Min., **I**OH = –2.0 mA	2.6			V
VOL	Output Low Voltage	**V**CC = Min., **I**OL = 4.0 mA			0.4	V
VIH	Input High Voltage		2.2		**V**CC	V
VIL	Input Low Voltage	(Note 3)	0.0		0.8	V
IIX	Input Current	Ground ≤ **V**IN ≤ **V**CC (Note 12)			±10	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC (Note 12)			±10	µA
ICC1	**V**CC Current, Dynamic	(Notes 5, 6)			310	mA
ICC2	**V**CC Current, Quiescent	(Note 7)			500	µA
CIN	Input Capacitance	**T**A = 25°C, f = 1 MHz			12	pF
COUT	Output Capacitance	**T**A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF48410–					
		30		25		15*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	30		25		15	
t_{PWL}	Clock Pulse Width Low	12		10		10	
t_{PWH}	Clock Pulse Width High	12		10		10	
t_{PS}	PIN_{9-0} Setup Time	13		12		5	
t_{PH}	PIN_{9-0} Hold Time	2		2		2	
t_{DS}	DIN_{23-0} Setup Time	13		12		5	
t_{DH}	DIN_{23-0} Hold Time	2		2		2	
t_{SS}	$\overline{START}$ Setup Time	13		12		5	
t_{SH}	$\overline{START}$ Hold Time	2		2		2	
t_{CY}	Read/Write Cycle Time	65		55		35	
t_{AS}	Address Setup Time	15		13		5	
t_{AH}	Address Hold Time	2		2		2	
t_{WL}	$\overline{WR}$ Pulse Width Low	15		12		7	
t_{WH}	$\overline{WR}$ Pulse Width High	15		12		5	
t_{WDS}	DIO_{23-0} Setup Time	15		12		5	
t_{WDH}	DIO_{23-0} Hold Time	2		2		2	
t_{RL}	$\overline{RD}$ Pulse Width Low	43		35		25	
t_{RH}	$\overline{RD}$ Pulse Width High	17		15		8	
t_{RD}	$\overline{RD}$ Low to DIO_{23-0} Valid		43		35		25
t_{OH}	$\overline{RD}$ High to DIO_{23-0} Valid		0		0		0
t_{LL}	$\overline{LD}$ Pulse Width	12		10		7	
t_{LS}	$\overline{LD}$ Setup to $\overline{START}$	30		25		15	
t_{FS}	FCT_{2-0} Setup Time	10		10		5	
t_{FH}	FCT_{2-0} Hold Time	2		2		2	
t_{FL}	$\overline{FC}$ Pulse Width	35		35		15	
t_D	Output Delay		19		15		11
t_{ENA}	Three-State Output Enable Delay (Note 11)		19		18		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		19		18		15

***DISCONTINUED SPEED GRADE**

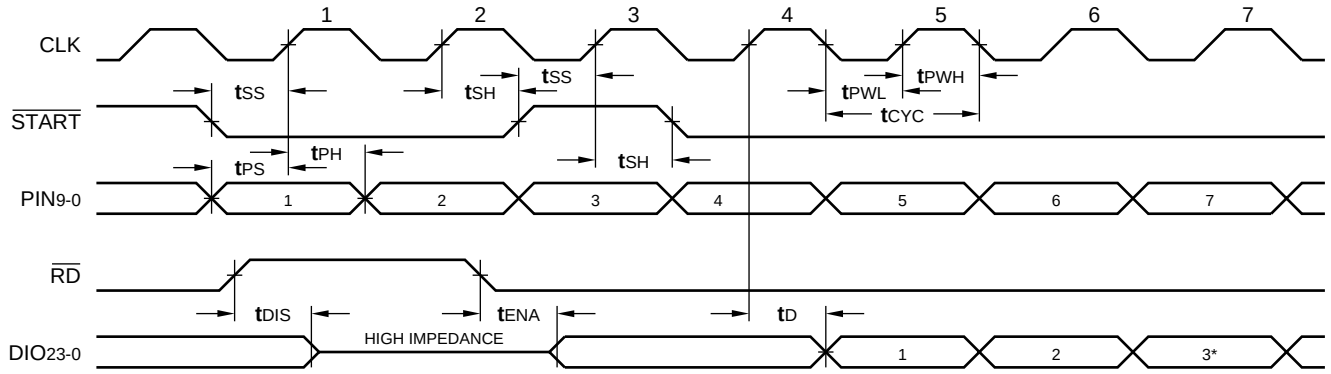
SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF48410–					
		39*		30*		25*	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	39		30		25	
t_{PWL}	Clock Pulse Width Low	15		12		12	
t_{PWH}	Clock Pulse Width High	15		12		12	
t_{PS}	PIN_{9-0} Setup Time	16		15		12	
t_{PH}	PIN_{9-0} Hold Time	2		2		2	
t_{DS}	DIN_{23-0} Setup Time	16		15		12	
t_{DH}	DIN_{23-0} Hold Time	2		2		2	
t_{SS}	$\overline{START}$ Setup Time	16		15		12	
t_{SH}	$\overline{START}$ Hold Time	2		2		2	
t_{CY}	Read/Write Cycle Time	80		65		55	
t_{AS}	Address Setup Time	20		16		13	
t_{AH}	Address Hold Time	2		2		2	
t_{WL}	$\overline{WR}$ Pulse Width Low	20		15		12	
t_{WH}	$\overline{WR}$ Pulse Width High	20		15		10	
t_{WDS}	DIO_{23-0} Setup Time	20		16		12	
t_{WDH}	DIO_{23-0} Hold Time	2		2		2	
t_{RL}	$\overline{RD}$ Pulse Width Low	55		43		35	
t_{RH}	$\overline{RD}$ Pulse Width High	20		17		15	
t_{RD}	$\overline{RD}$ Low to DIO_{23-0} Valid		55		43		35
t_{OH}	$\overline{RD}$ High to DIO_{23-0} High Z	0		0		0	
t_{LL}	$\overline{LD}$ Pulse Width	15		12		10	
t_{LS}	$\overline{LD}$ Setup to $\overline{START}$	39		30		25	
t_{FS}	FCT_{2-0} Setup Time	15		12		10	
t_{FH}	FCT_{2-0} Hold Time	2		2		2	
t_{FL}	$\overline{FC}$ Pulse Width	35		35		35	
t_{D}	Output Delay		24		19		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		24		19		18
t_{DIS}	Three-State Output Disable Delay (Note 11)		27		27		18

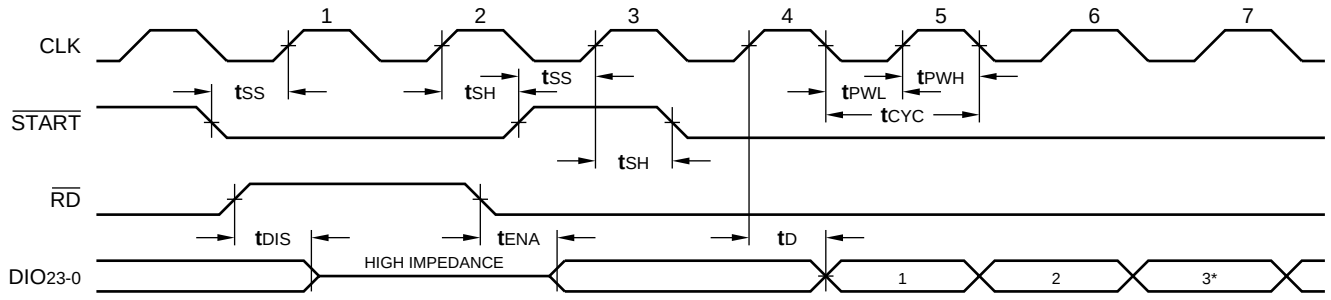
***DISCONTINUED SPEED GRADE**

SWITCHING WAVEFORMS: HISTOGRAM MODE



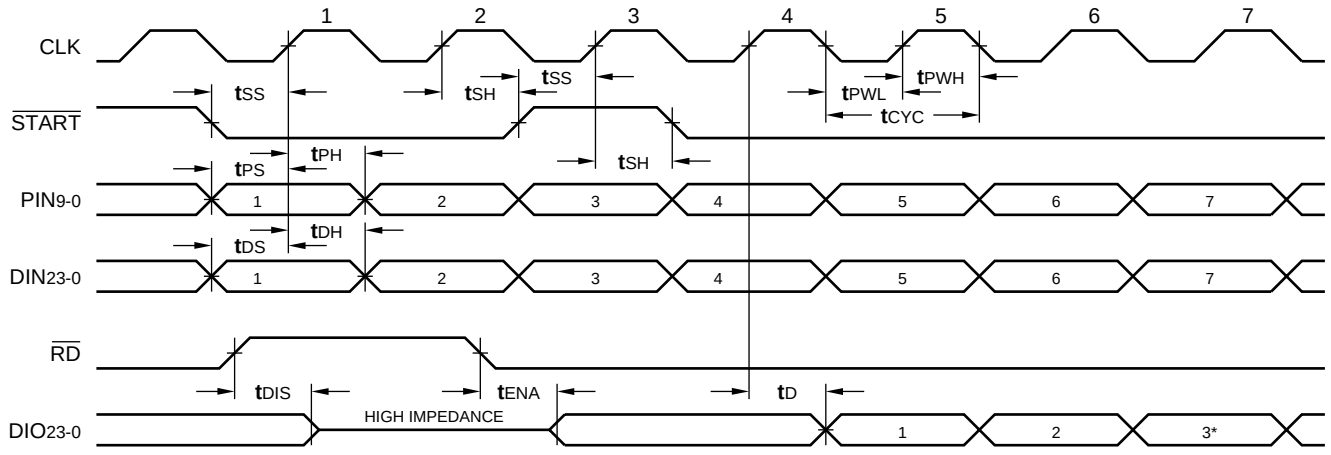
*RAM contents not changed.

SWITCHING WAVEFORMS: HISTOGRAM ACCUMULATE MODE



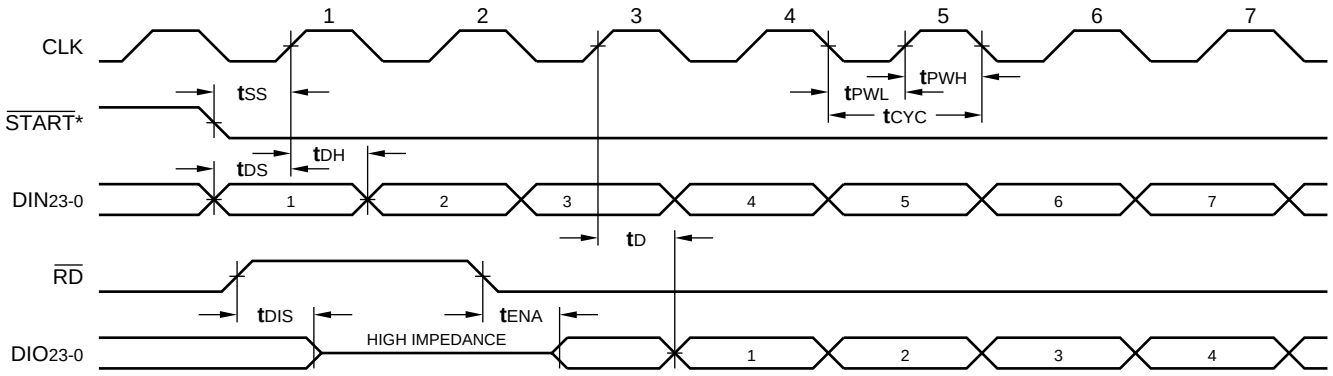
*RAM contents not changed.

SWITCHING WAVEFORMS: BIN ACCUMULATE MODE



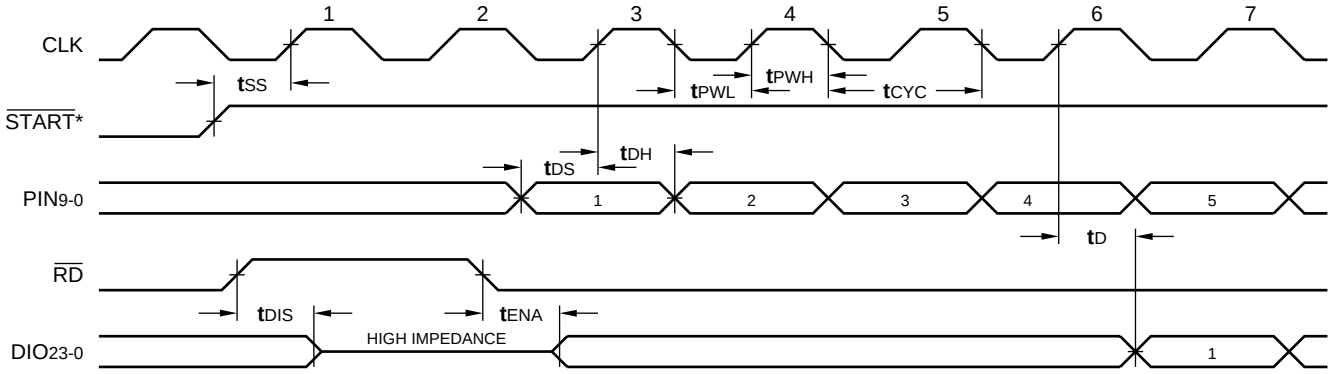
*RAM contents not changed.

Switching Waveforms: Look Up Table Write Mode



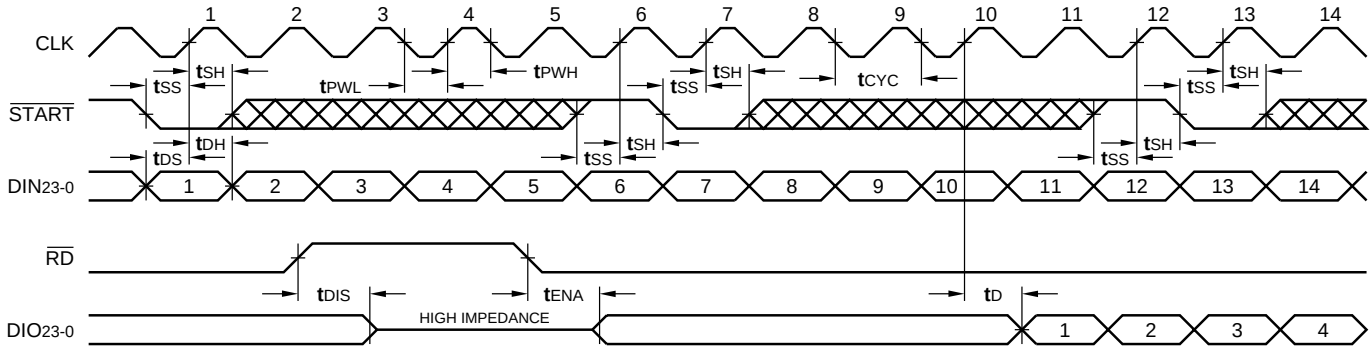
*$\overline{START}$ must be held LOW a minimum of t_{SH} after the rising edge of CLK that loads the last value of DIN_{23-0}.

Switching Waveforms: Look Up Table Read Mode



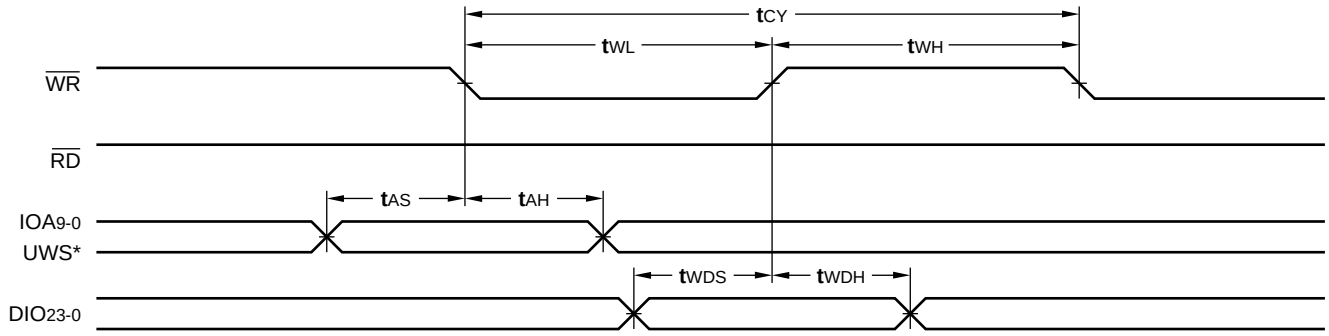
*$\overline{START}$ must be held HIGH a minimum of t_{SH} after the rising edge of CLK that loads the last value of PIN_{9-0}.

Switching Waveforms: Delay Memory/Delay And Subtract Mode



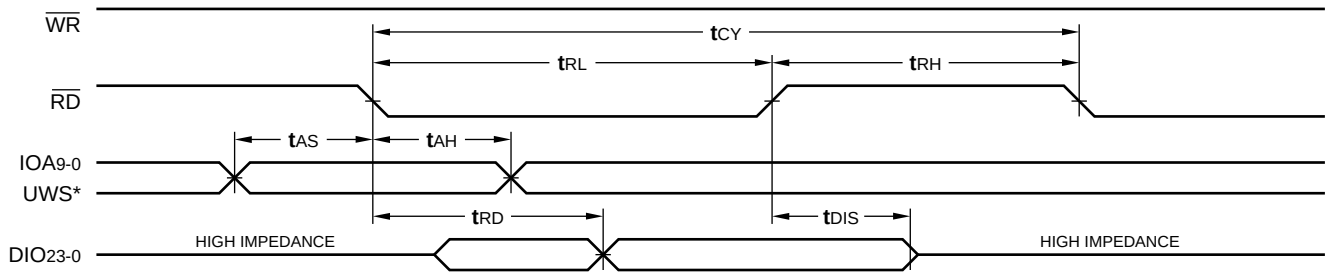
Shown are the waveforms for a delay length of 10.

Switching Waveforms: Asynchronous Write 16/24 Mode



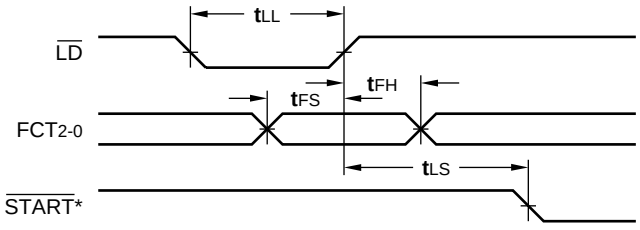
*applies only to 16-bit Asynchronous Mode.

Switching Waveforms: Asynchronous Read 16/24 Mode



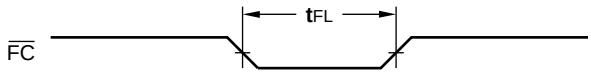
*applies only to 16-bit Asynchronous Mode.

Switching Waveforms: Fucntion Load



*there must be at least one rising edge of CLK between the rising edge of $\overline{LD}$ and the falling edge of $\overline{START}$.

Switching Waveforms: Flash Clear



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

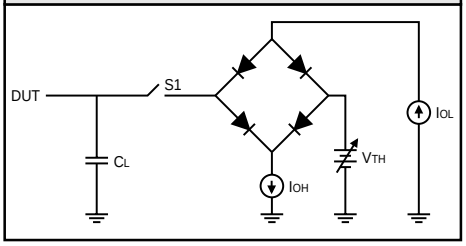
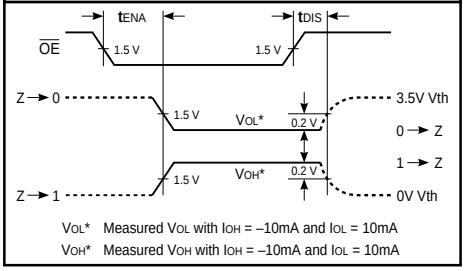
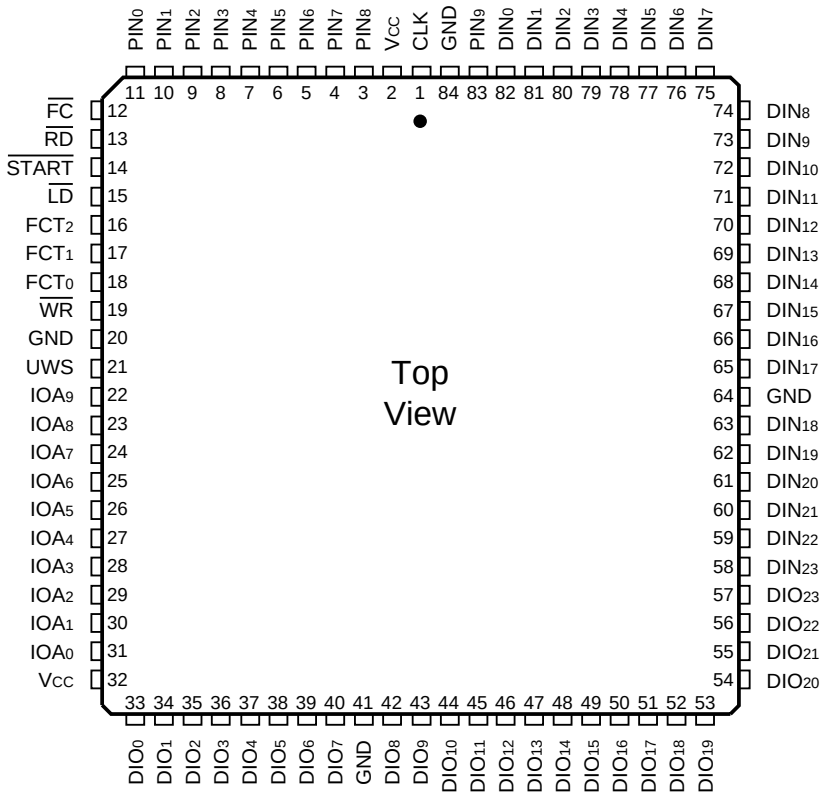


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

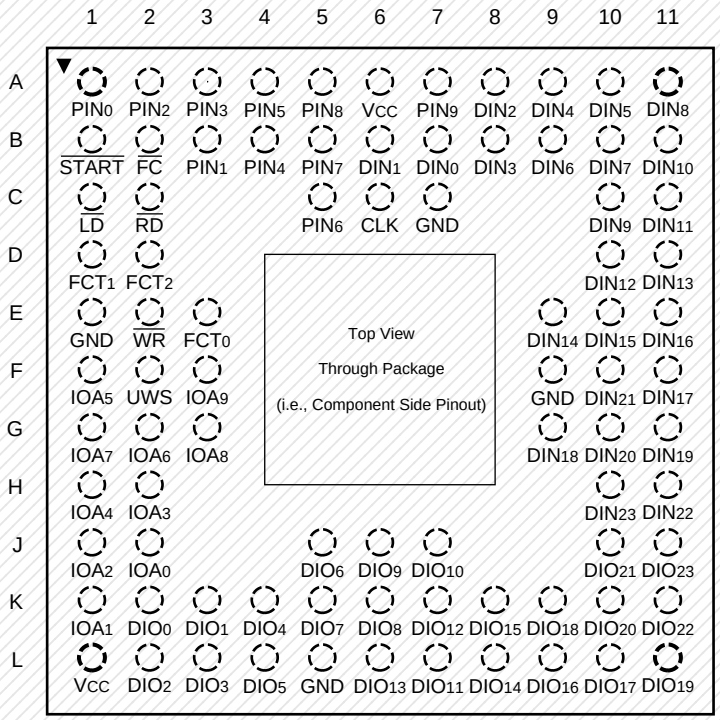
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
30 ns	LF48410JC30
25 ns	LF48410JC25
	–40°C to +85°C — COMMERCIAL SCREENING

ORDERING INFORMATION

84-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G6)
	0°C to +70°C — Commercial Screening
	–55°C to +125°C — Commercial Screening
	–55°C to +125°C — MIL-STD-883 Compliant