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Product List

SM59R02G1W28KP, SM59R02G1W28SP,
SM59R02G1W40PP, SM59R02G1W44JP,
SM59R02G1W44QP, SM59R02G1W44UP,
SM59R02G1W48VP

Description

The SM59R02G1 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 8K-byte embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51.
SM59R02G1 contains 256B on-chip RAM, more than 42 GPIOs (PLCC 44, QFP 44 and LQFP 48), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage. The high performance of SM59R02G1 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

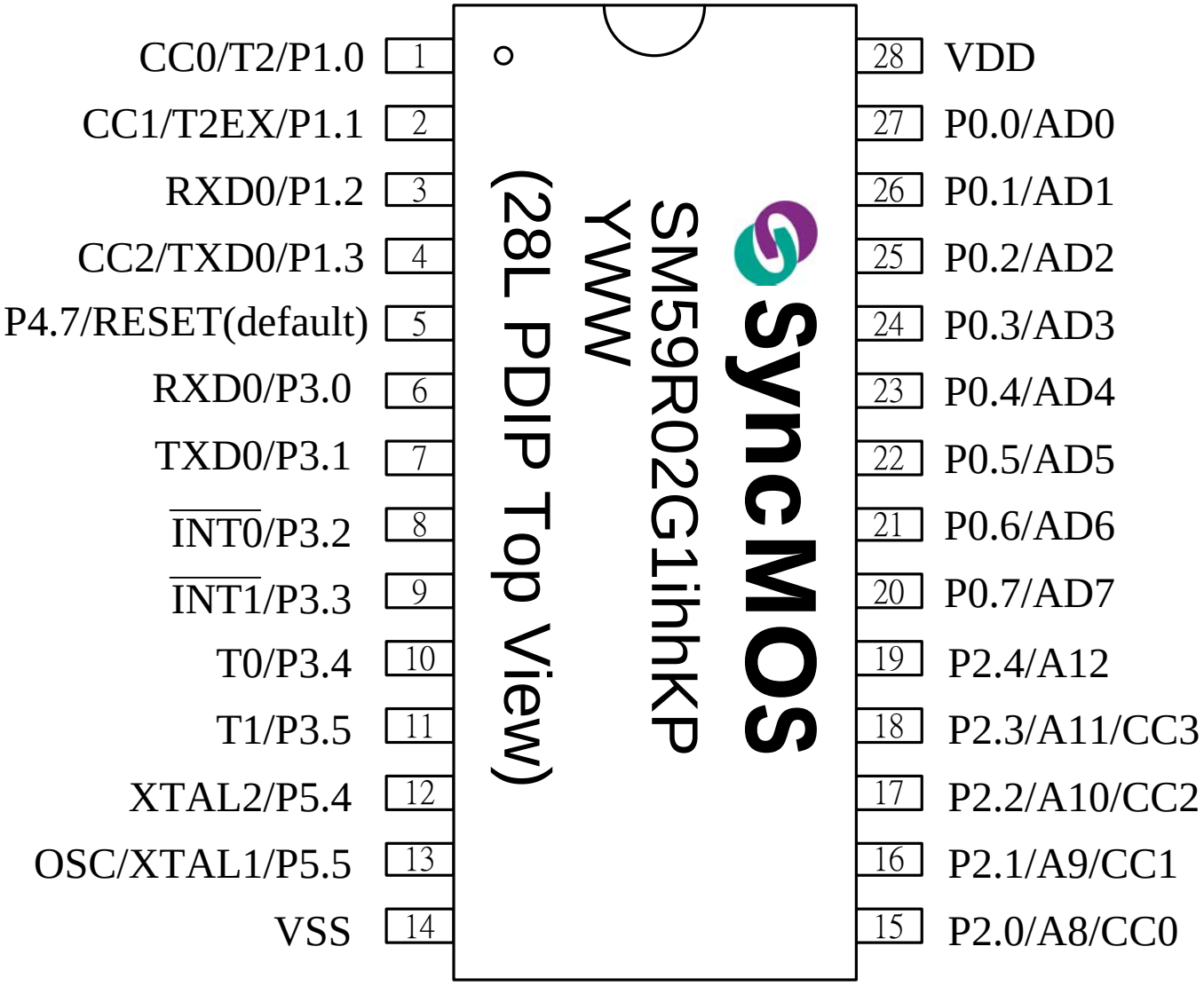
SM59R02G1ihhkL YWW
i: process identifier {W = 2.7V ~ 5.5V}
hh: Pin Count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: Year Code
WW: Week Code (01-52)

Postfix	Package	Pin / Pad Configuration
K	28L PDIP	Page 4
S	28L SOP	Page 5
P	40L PDIP	Page 6
J	44L PLCC	Page 7
Q	44L PQFP	Page 8
V	48L LQFP	Page 9

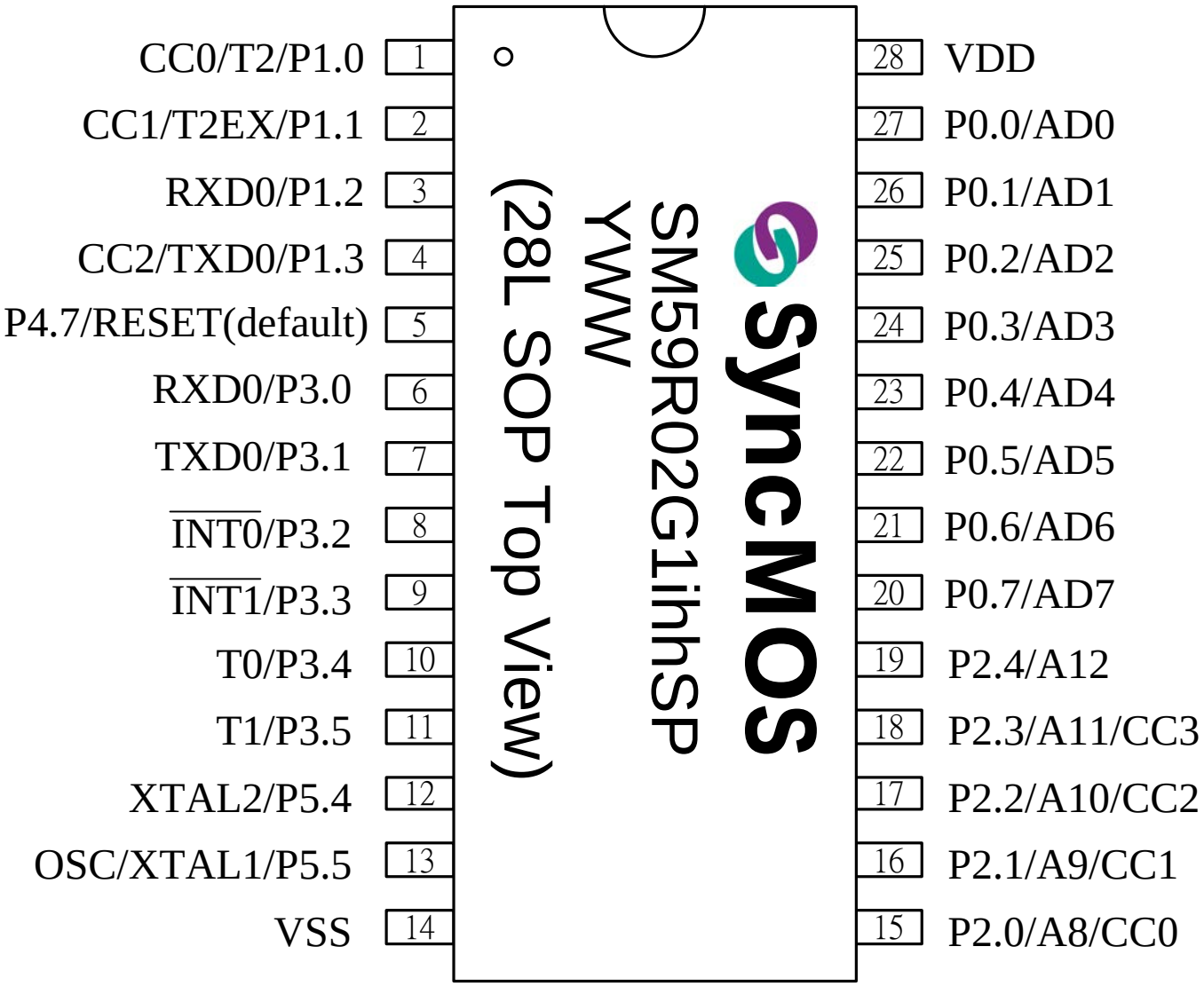
Features

- Operating Voltage: 2.7V ~ 5.5V
- High speed architecture of 1 clock/machine cycle (1T), runs up to 25MHz
- 1T/2T can be switched on the fly
- Instruction-set compatible with MCS-51
- 8K Bytes on-chip program memory.
- External RAM addresses up to 64K bytes.
  Standard 12T interface for external RAM access.
- 256 bytes RAM as standard 8052
- Dual 16-bit Data Pointers (DPTR0 & DPTR1)
- One serial peripheral interfaces in full duplex mode (UART0),
  Additional Baud Rate Generator for Serial 0.
- Three 16-bit Timers/Counters. (Timer 0 , 1, 2)
- 38 GPIOs(PDIP 40), 42 GPIOs(PLCC 44/PQFP 44/LQFP 48),GPIOs can select four Type(quasi-bidirectional, push-pull, open drain, input-only), default is quasi-bidirectional(pull-up)
- External interrupt 0,1 with four priority levels
- Programmable watchdog timer (WDT)
- 4-channel 16-bit compare /capture /load functions
- 22.1184MHz Internal RC oscillator, with programmable clock divider
- Configurable Oscillator pin
- ISP/IAP functions.
- ISP service program space configurable in N*256 byte (N=0 to 4) size.
- EEPROM function
- ALE output select.
- LVR (LVR deglitch 500ns)
- Enhanced user code protection
- Power management unit for idle and power down modes

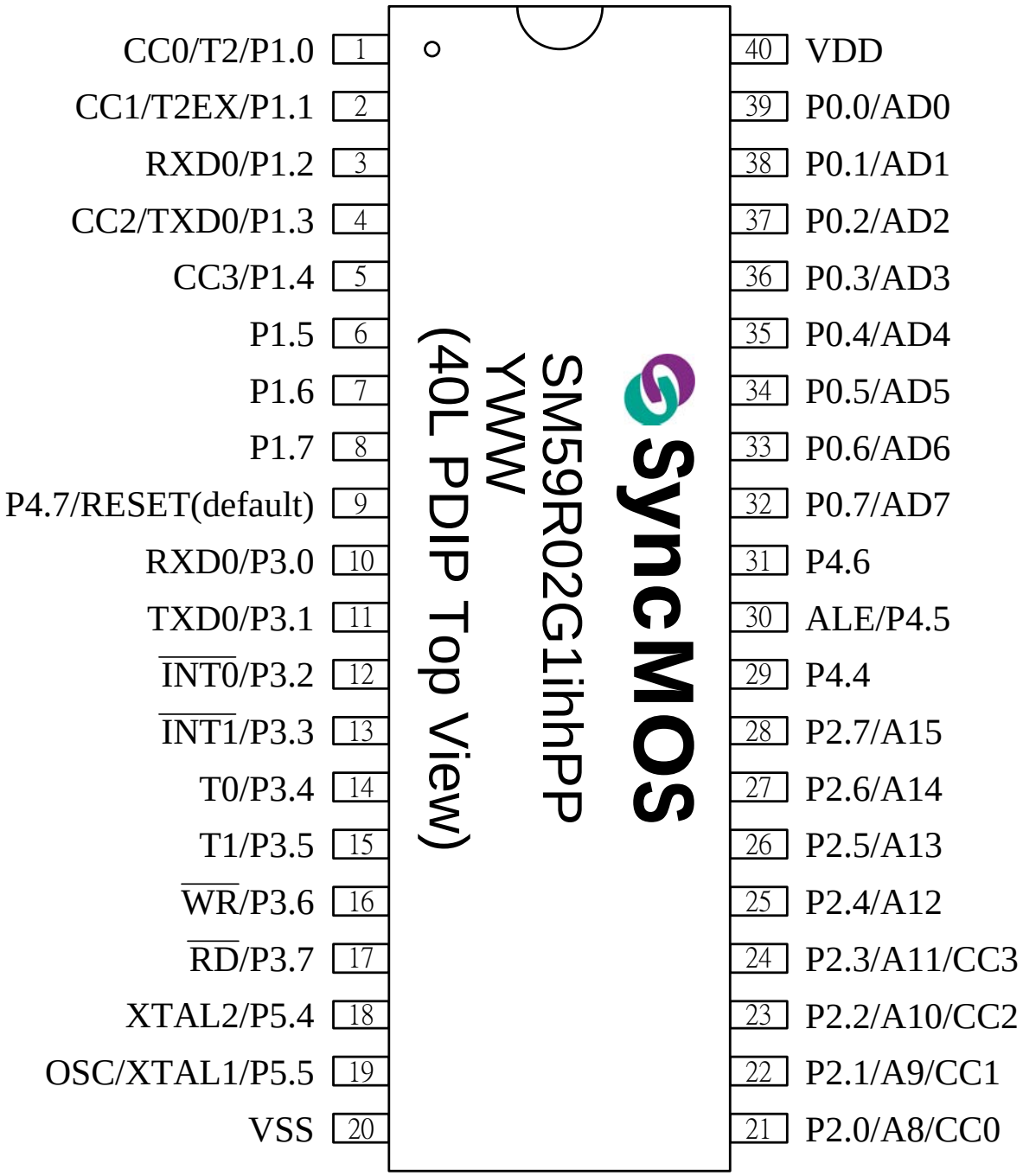
Pin Configuration



Notes：
The pin Reset/P4.7 factory default is Reset, user must keep this pin at low during power-up. User can configure it to GPIO (P4.7) by a flash programmer.

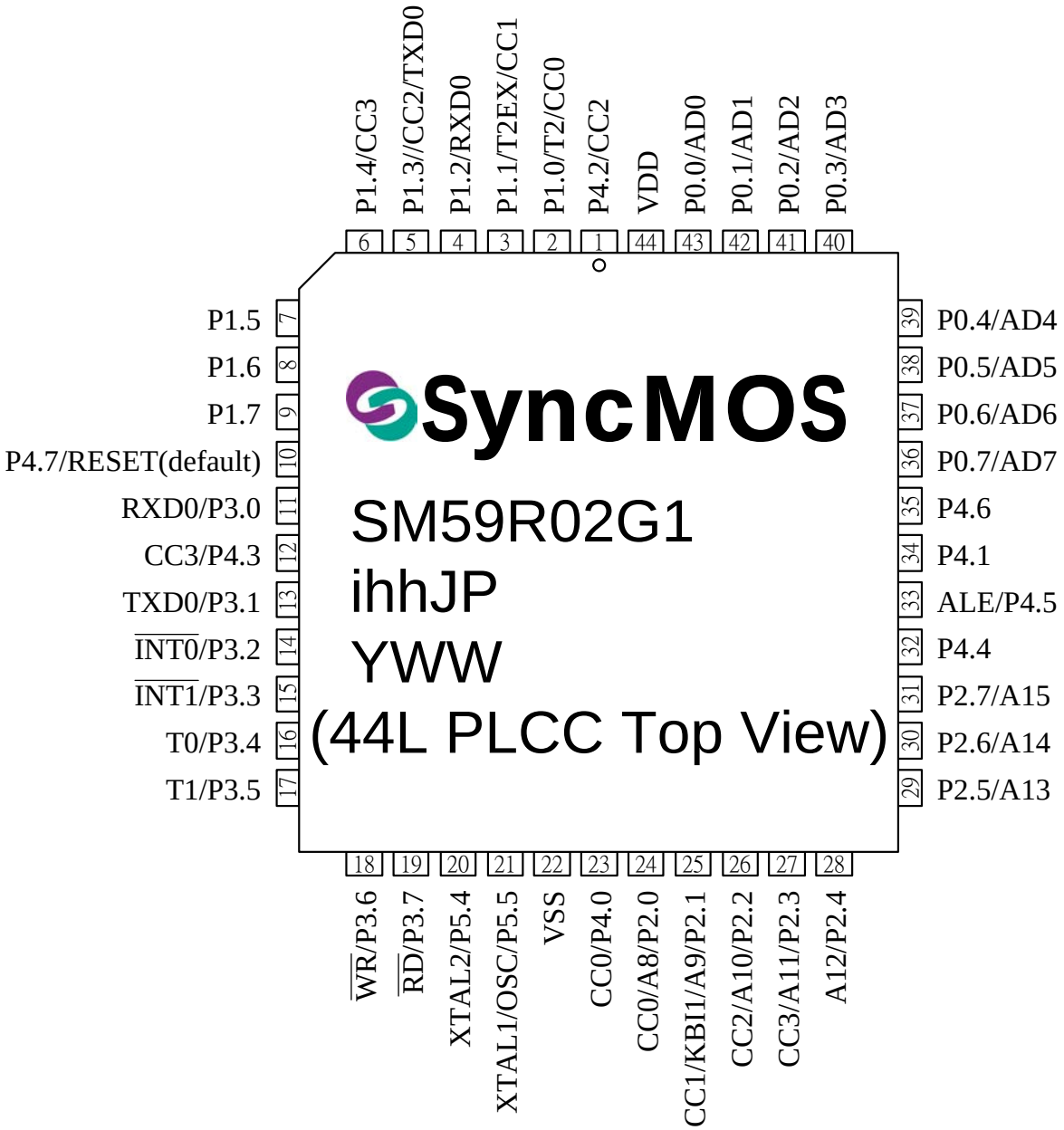


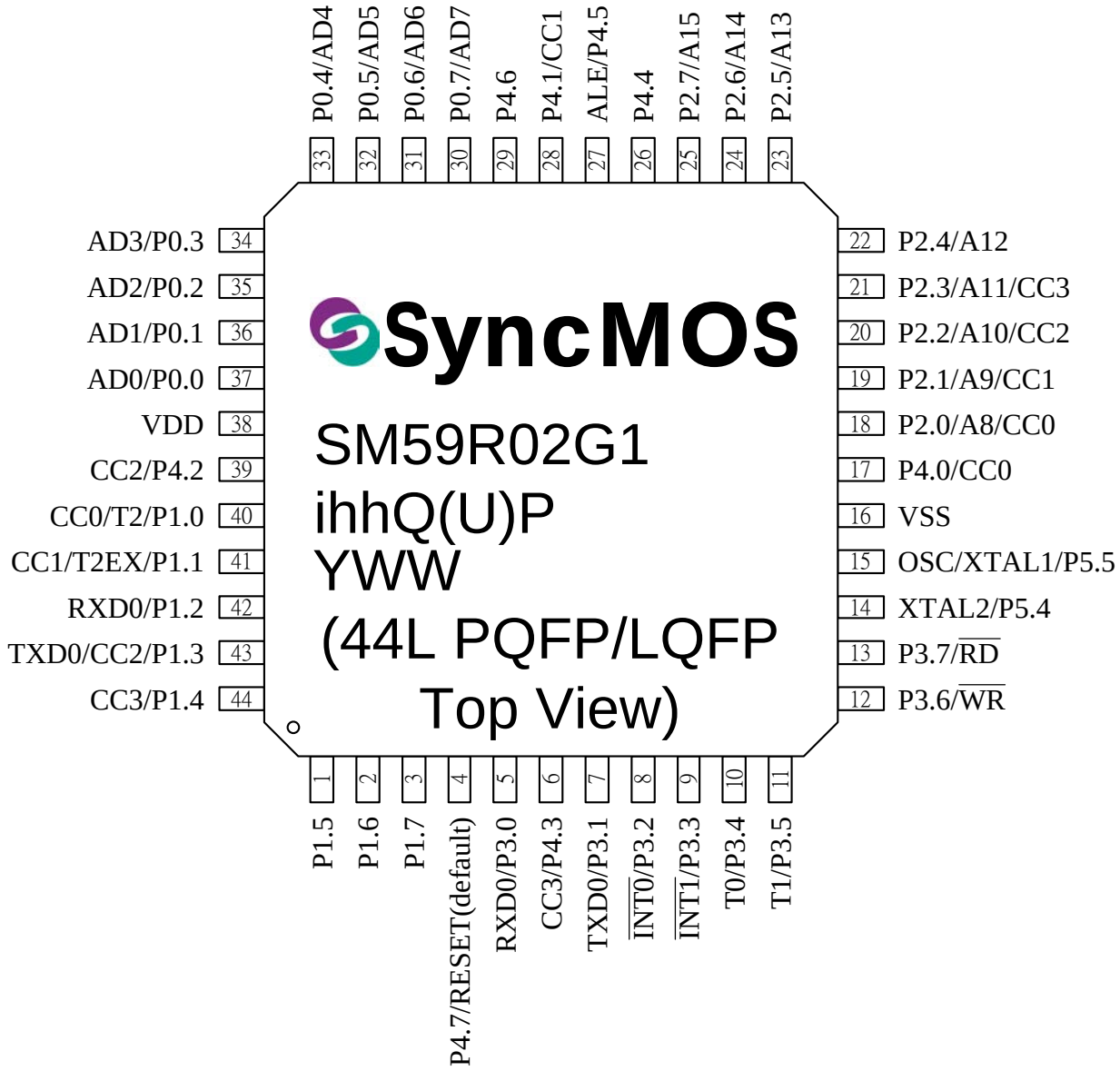
Notes：
The pin Reset/P4.7 factory default is Reset, user must keep this pin at low during power-up. User can configure it to GPIO (P4.7) by a flash programmer.

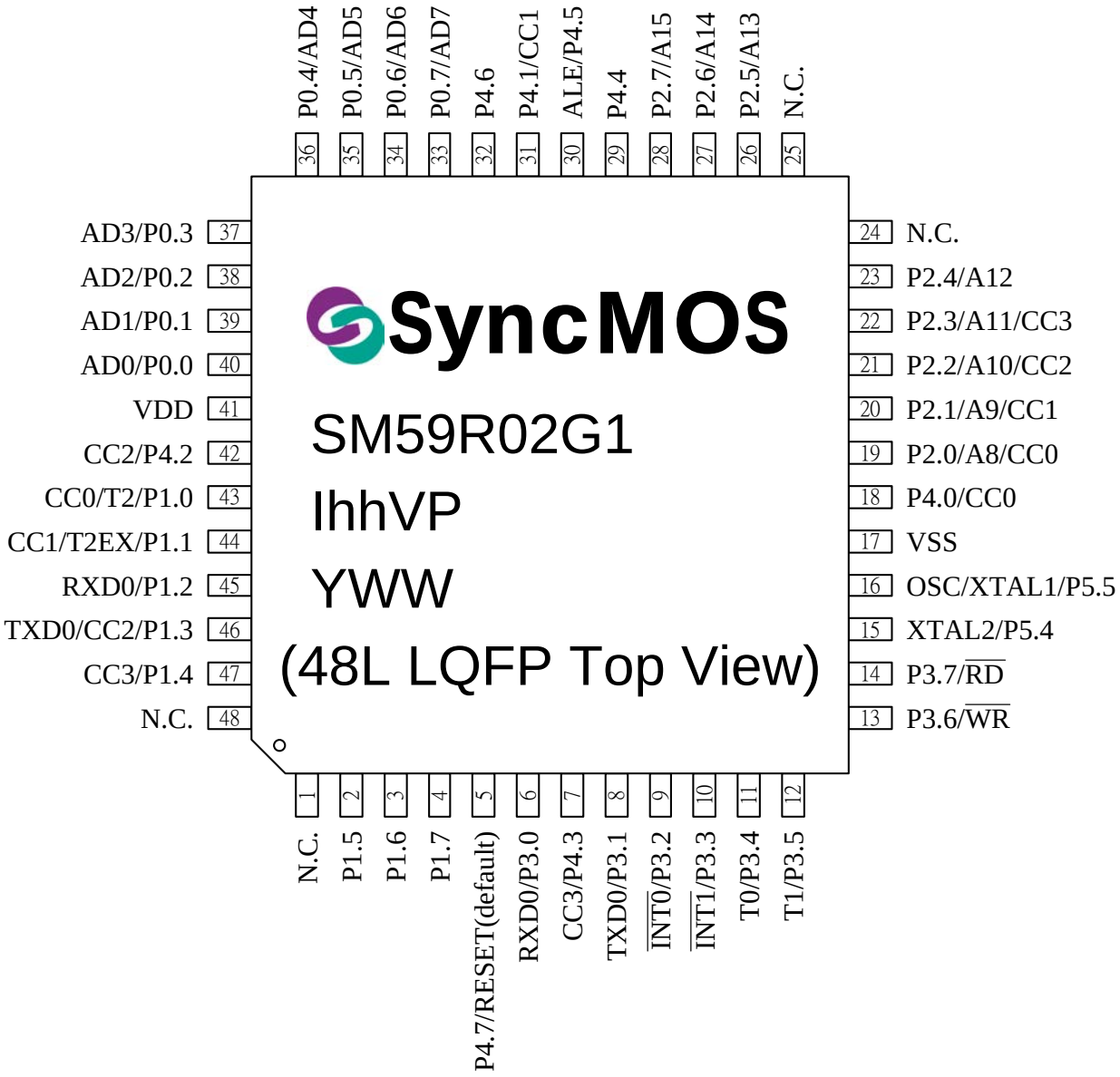


Notes：

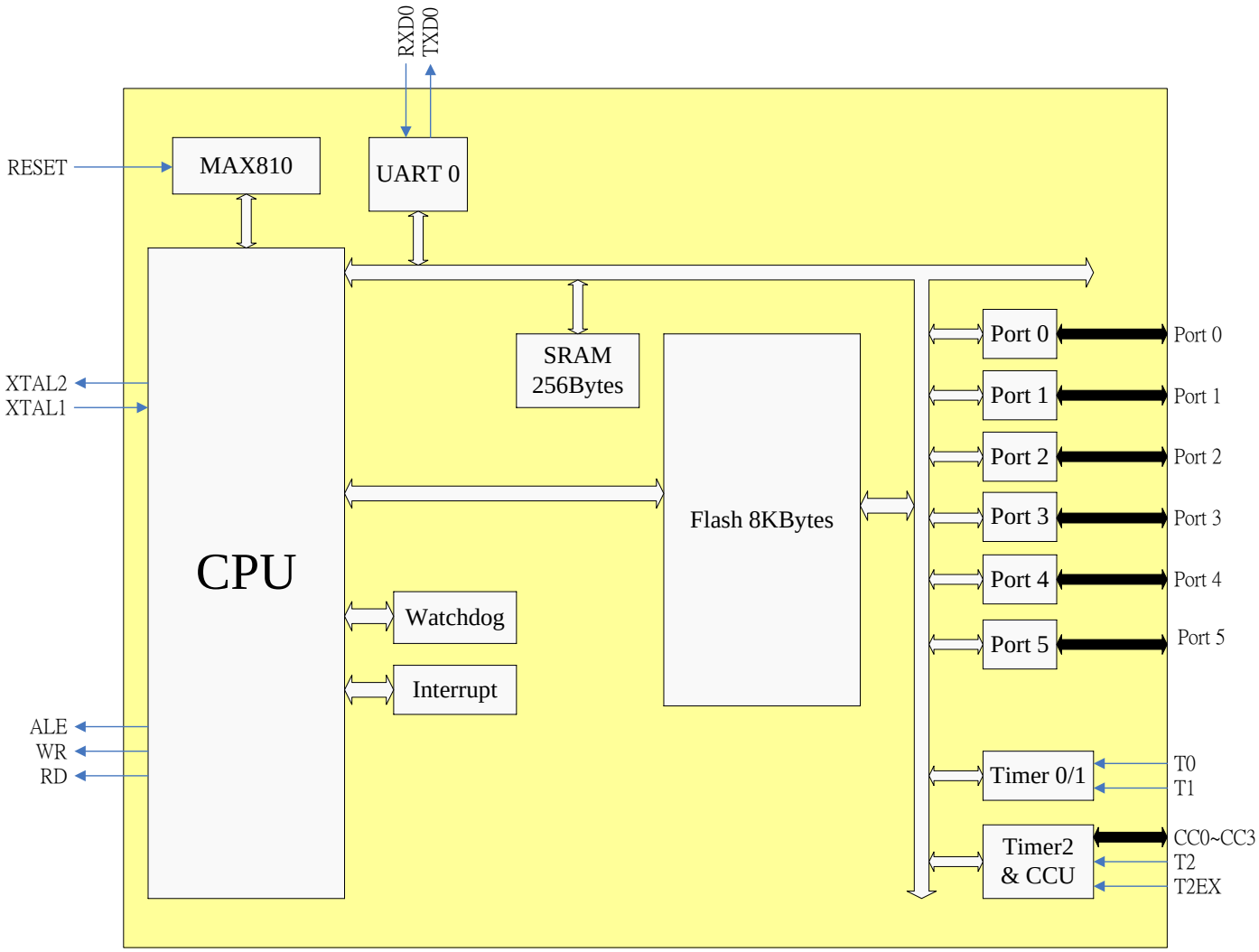
1. The pin Reset/P4.7 factory default is Reset, user must keep this pin at low during power-up. User can configure it to GPIO (P4.7) by a flash programmer.
2. To avoid accidentally entering ISP-Mode(refer to section 13.4), care must be taken not asserting pulse signal at P3.0 during power-up while P2.6, P2.7, P4.3 are set to high.


P1.4/CC3
P1.3//CC2/TXD0
P1.2/RXD0
P1.1/T2EX/CC1
P1.0/T2/CC0
P4.2/CC2
VDD
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
6
5
4
3
2
1
44
43
42
41
40
P1.5 7
P1.6 8
P1.7 9
P4.7/RESET(default) 10
RXD0/P3.0 11
CC3/P4.3 12
TXD0/P3.1 13
INT0/P3.2 14
INT1/P3.3 15
T0/P3.4 16
T1/P3.5 17
39 P0.4/AD4
38 P0.5/AD5
37 P0.6/AD6
36 P0.7/AD7
35 P4.6
34 P4.1
33 ALE/P4.5
32 P4.4
31 P2.7/A15
30 P2.6/A14
29 P2.5/A13
SyncMOS
SM59R02G1
ihhJP
YWW
(44L PLCC Top View)
18
19
20
21
22
23
24
25
26
27
28
WR/P3.6
RD/P3.7
XTAL2/P5.4
XTAL1/OSC/P5.5
VSS
CC0/P4.0
CC0/A8/P2.0
CC1/KBI1/A9/P2.1
CC2/A10/P2.2
CC3/A11/P2.3
A12/P2.4


P0.4/AD4 33
P0.5/AD5 32
P0.6/AD6 31
P0.7/AD7 30
P4.6 29
P4.1/CC1 28
ALE/P4.5 27
P4.4 26
P2.7/A15 25
P2.6/A14 24
P2.5/A13 23
AD3/P0.3 34
AD2/P0.2 35
AD1/P0.1 36
AD0/P0.0 37
VDD 38
CC2/P4.2 39
CC0/T2/P1.0 40
CC1/T2EX/P1.1 41
RXD0/P1.2 42
TXD0/CC2/P1.3 43
CC3/P1.4 44
SyncMOS
SM59R02G1
ihhQ(U)P
YWW
(44L PQFP/LQFP
Top View)
22 P2.4/A12
21 P2.3/A11/CC3
20 P2.2/A10/CC2
19 P2.1/A9/CC1
18 P2.0/A8/CC0
17 P4.0/CC0
16 VSS
15 OSC/XTAL1/P5.5
14 XTAL2/P5.4
13 P3.7/RD
12 P3.6/WR
1 P1.5
2 P1.6
3 P1.7
4 P4.7/RESET(default)
5 RXD0/P3.0
6 CC3/P4.3
7 TXD0/P3.1
8 INT0/P3.2
9 INT1/P3.3
10 T0/P3.4
11 T1/P3.5


P0.4/AD4 36
P0.5/AD5 35
P0.6/AD6 34
P0.7/AD7 33
P4.6 32
P4.1/CC1 31
ALE/P4.5 30
P4.4 29
P2.7/A15 28
P2.6/A14 27
P2.5/A13 26
N.C. 25
AD3/P0.3 37
AD2/P0.2 38
AD1/P0.1 39
AD0/P0.0 40
VDD 41
CC2/P4.2 42
CC0/T2/P1.0 43
CC1/T2EX/P1.1 44
RXD0/P1.2 45
TXD0/CC2/P1.3 46
CC3/P1.4 47
N.C. 48
SyncMOS
SM59R02G1
IhhVP
YWW
(48L LQFP Top View)
24 N.C.
23 P2.4/A12
22 P2.3/A11/CC3
21 P2.2/A10/CC2
20 P2.1/A9/CC1
19 P2.0/A8/CC0
18 P4.0/CC0
17 VSS
16 OSC/XTAL1/P5.5
15 XTAL2/P5.4
14 P3.7/RD
13 P3.6/WR
1 N.C.
2 P1.5
3 P1.6
4 P1.7
5 P4.7/RESET(default)
6 RXD0/P3.0
7 CC3/P4.3
8 TXD0/P3.1
9 INT0/P3.2
10 INT1/P3.3
11 T0/P3.4
12 T1/P3.5

Block Diagram



Pin Description

28L	40L PDIP	44L PLCC	44L QFP	48L LQFP	Symbol	I/O	Description
		1	39	42	P4.2/CC2	I/O	Bit 2 of port 4 & Timer 2 compare/capture Channel 2
1	1	2	40	43	P1.0/T2/CC0	I/O	Bit 0 of port 1 & Timer 2 external input clock & Timer 2 compare/capture Channel 0
2	2	3	41	44	P1.1/T2EX/CC1	I/O	Bit 1 of port 1 & Timer 2 capture trigger & Timer 2 compare/capture Channel 1
3	3	4	42	45	P1.2/RXD0	I/O	Bit 2 of port 1 & Serial interface channel 0 receive data
4	4	5	43	46	P1.3/TXD0/CC2	I/O	Bit 3 of port 1 & Serial interface channel 0 transmit data & Timer 2 compare/capture Channel 2
	5	6	44	47	P1.4/CC3	I/O	Bit 4 of port 1 & Timer 2 compare/capture Channel 3
				48	NC		
				1	NC		
	6	7	1	2	P1.5	I/O	Bit 5 of port 1
	7	8	2	3	P1.6	I/O	Bit 6 of port 1
	8	9	3	4	P1.7	I/O	Bit 7 of port 1
5	9	10	4	5	RESET(default)/P 4.7	I/O	Reset pin(default)& Bit 7 of port 4
6	10	11	5	6	P3.0/RXD0	I/O	Bit 0 of port 3 & Serial interface channel 0 receive/transmit data
		12	6	7	P4.3/CC3	I/O	Bit 3 of port 4 & Timer 2 compare/capture Channel 3
7	11	13	7	8	P3.1/TXD0	I/O	Bit 1 of port 3 & Serial interface channel 0 transmit data or receive clock in mode 0
8	12	14	8	9	P3.2/#INT0	I/O	Bit 2 of port 3 & External interrupt 0
9	13	15	9	10	P3.3/#INT1	I/O	Bit 3 of port 3 & External interrupt 1
10	14	16	10	11	P3.4/T0	I/O	Bit 4 of port 3 & Timer 0 external input
11	15	17	11	12	P3.5/T1	I/O	Bit 5 of port 3 & Timer 1 external input
	16	18	12	13	P3.6/#WR	I/O	Bit 6 of port 3 & external memory write signal
	17	19	13	14	P3.7/#RD	I/O	Bit 7 of port 3 & external memory read signal
12	18	20	14	15	XTAL2/P5.4	O	Crystal output & bit4 of port 5
13	19	21	15	16	XTAL1/OSC/P5.5	I	Crystal input& Oscillator input& bit5 of port 5
14	20	22	16	17	VSS	I	Ground line
		23	17	18	P4.0/CC0	I/O	Bit 0 of port 4 & Timer 2 compare/capture Channel 0
15	21	24	18	19	P2.0 /A8/CC0	I/O	Bit 0 of port 2 & Bit 8 of external memory address& Timer 2 compare/capture Channel 0
16	22	25	19	20	P2.1 /A9/CC1	I/O	Bit 1 of port 2 & Bit 9 of external memory address& Timer 2 compare/capture Channel 1
17	23	26	20	21	P2.2 /A10/CC2	I/O	Bit 2 of port 2 & Bit 10 of external memory address & Timer 2 compare/capture Channel 2
18	24	27	21	22	P2.3 /A11/CC3	I/O	Bit 3 of port 2 & Bit 11 of external memory address & Timer 2 compare/capture Channel 3
19	25	28	22	23	P2.4 /A12	I/O	Bit 4 of port 2 & Bit 12 of external memory address
				24	NC		
				25	NC		
	26	29	23	26	P2.5 /A13	I/O	Bit 5 of port 2 & Bit 13 of external memory address
	27	30	24	27	P2.6 /A14	I/O	Bit 6 of port 2 & Bit 14 of external memory address
	28	31	25	28	P2.7 /A15	I/O	Bit 7 of port 2 & Bit 15 of external memory address
	29	32	26	29	P4.4	I/O	Bit 4 of port 4
	30	33	27	30	ALE/P4.5	I/O	Address latch enable & Bit 5 of port 4
		34	28	31	P4.1CC1	I/O	Bit 1 of port 4 & Timer 2 compare/capture Channel 1
	31	35	29	32	P4.6	I/O	Bit 6 of port 4
20	32	36	30	33	P0.7/AD7	I/O	Bit 7 of port 0 & Bit 7 of external memory address/ data

28L	40L PDIP	44L PLCC	44L QFP	48L LQFP	Symbol	I/O	Description
21	33	37	31	34	P0.6/AD6	I/O	Bit 6 of port 0 & Bit 6 of external memory address/ data
22	34	38	32	35	P0.5/AD5	I/O	Bit 5 of port 0 & Bit 5 of external memory address/ data
23	35	39	33	36	P0.4/AD4	I/O	Bit 4 of port 0 & Bit 4 of external memory address/ data
24	36	40	34	37	P0.3/AD3	I/O	Bit 3 of port 0 & Bit 3 of external memory address/ data
25	37	41	35	38	P0.2/AD2	I/O	Bit 2 of port 0 & Bit 2 of external memory address/ data
26	38	42	36	39	P0.1/AD1	I/O	Bit 1 of port 0 & Bit 1 of external memory address/ data
27	39	43	37	40	P0.0/AD0	I/O	Bit 0 of port 0 & Bit 0 of external memory address/ data
28	40	44	38	41	VDD	I	Power supply

Special Function Register (SFR)

A map of the Special Function Registers is shown as below:

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8							-	-	**FF**
F0	B						-	TAKEY	**F7**
E8	P4	-	-	-	-	-	-	-	**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC	-	LVC	SWRES	**E7**
D8	P5	PFCON	P3M0	P3M1	P4M0	P4M1	P5M0	P5M1	**DF**
D0	PSW	CCEN2	P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	**D7**
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2	-	-	**CF**
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	**C7**
B8	IEN1	IP1	S0RELH	-	-	-	-	-	**BF**
B0	P3	-	-	-	-	-	WDTC	WDTK	**B7**
A8	IEN0	IP0	S0RELL	-	-	-	-	-	**AF**
A0	P2	RSTS	-	-	-	-	-	-	**A7**
98	S0CON	S0BUF	IEN2	-	-	-	-	-	**9F**
90	P1	AUX	AUX2	-	-	-	-	IRCON2	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1		IFCON	**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	-	PCON	**87**
Hex\Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/Hex**

Note: Special Function Registers reset values and description for SM59R02G1

Register	Location	Reset value	Description
P0	80h	FFh	Port 0
SP	81h	07h	Stack Pointer
DPL	82h	00h	Data Pointer 0 low byte
DPH	83h	00h	Data Pointer 0 high byte
DPL1	84h	00h	Data Pointer 1 low byte
DPH1	85h	00h	Data Pointer 1 high byte
PCON	87h	40h	Power Control
TCON	88h	00h	Timer/Counter Control
TMOD	89h	00h	Timer Mode Control
TL0	8Ah	00h	Timer 0, low byte
TL1	8Bh	00h	Timer 1, low byte
TH0	8Ch	00h	Timer 0, high byte
TH1	8Dh	00h	Timer 1, high byte
IFCON	8Fh	00h	Interface control register
P1	90h	FFh	Port 1
AUX	91h	00h	Auxiliary register

Register	Location	Reset value	Description
AUX2	92h	00h	Auxiliary 2 register
IRCON2	97H	00h	Interrupt Request Control Register
S0CON	98h	00h	Serial Port 0, Control Register
S0BUF	99h	00h	Serial Port 0, Data Buffer
IEN2	9Ah	00h	Interrupt Enable Register 2
P2	A0h	FFh	Port 2
RSTS	A1h	00h	Reset Status Flag Register
IEN0	A8h	00h	Interrupt Enable Register 0
IP0	A9h	00h	Interrupt Priority Register 0
S0RELL	AAh	00h	Serial Port 0, Reload Register, low byte
P3	B0h	FFh	Port 3
WDTC	B6h	04h	Watchdog timer control register
WDTK	B7h	00h	Watchdog timer refresh key.
IEN1	B8h	00h	Interrupt Enable Register 1
IP1	B9h	00h	Interrupt Priority Register 1
S0RELH	BAh	00h	Serial Port 0, Reload Register, high byte
IRCON	C0h	00h	Interrupt Request Control Register
CCEN	C1h	00h	Compare/Capture Enable Register
CCL1	C2h	00h	Compare/Capture Register 1, low byte
CCH1	C3h	00h	Compare/Capture Register 1, high byte
CCL2	C4h	00h	Compare/Capture Register 2, low byte
CCH2	C5h	00h	Compare/Capture Register 2, high byte
CCL3	C6h	00h	Compare/Capture Register 3, low byte
CCH3	C7h	00h	Compare/Capture Register 3, high byte
T2CON	C8h	00h	Timer 2 Control
CCCON	C9h	00h	Compare/Capture Control
CRCL	CAh	00h	Compare/Reload/Capture Register, low byte
CRCH	CBh	00h	Compare/Reload/Capture Register, high byte
TL2	CCh	00h	Timer 2, low byte
TH2	CDh	00h	Timer 2, high byte
PSW	D0h	00h	Program Status Word
CCEN2	D1h	00h	Compare/Capture Enable 2 register
P0M0	D2h	00h	Port 0 output mode 0
P0M1	D3h	00h	Port 0 output mode 1
P1M0	D4h	00h	Port 1 output mode 0
P1M1	D5h	00h	Port 1 output mode 1
P2M0	D6h	00h	Port 2 output mode 0
P2M1	D7h	00h	Port 2 output mode 1
P5	D8h	FFh	Port 5
PFCON	D9h	00h	Peripheral Frequency control register
P3M0	DAh	00h	Port 3 output mode 0
P3M1	DBh	00h	Port 3 output mode 1

Register	Location	Reset value	Description
P4M0	DCh	00h	Port 4 output mode 0
P4M1	DDh	00h	Port 4 output mode 1
P5M0	DEh	00h	Port 5 output mode 0
P5M1	DFh	00h	Port 5 output mode 1
ACC	E0h	00h	Accumulator
ISPFAH	E1h	FFh	ISP Flash Address-High register
ISPFAL	E2h	FFh	ISP Flash Address-Low register
ISPFD	E3h	FFh	ISP Flash Data register
ISPFC	E4h	00h	ISP Flash control register
LVC	E6h	20h	Low voltage control register
SWRES	E7h	00h	Software Reset register
P4	E8h	FFh	Port 4
B	F0h	00h	B Register
TAKEY	F7h	00h	Time Access Key register

Function Description

1. General Features

SM59R02G1 is an 8-bit micro-controller。All of its functions and the detailed meanings of SFR will be given in the following sections.

1.1. Embedded Flash

The program can be loaded into the embedded 8KB Flash memory via its writer or In-System Programming (ISP).

1.2. IO Pads

The SM59R02G1 has six I/O ports: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 3, 4 are 8-bit ports and Port 5 is a 2-bit port (Only Bit 4 and Bit 5). These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. As description in section 5.

The XTAL2 and XTAL1 can define as P5.4 and P5.5 by writer or ISP. When user use external OSC as system clock and input into XTAL1, Only XTAL2 can be defined as P5.4.

All the pads for P0 ~ P5 are with slew rate to reduce EMI. The other way to reduce EMI is to disable the ALE output if unused. This is selected by its SFR. The IO pads can withstand 4KV ESD in human body mode guaranteeing the SM59R02G1's quality in high electro-static environments.

1.3. 2T/1T Selection

The conventional 52-series MCUs are 12T, i.e., 12 oscillator clocks per machine cycle. SM59R02G1 is a 2T or 1T MCU, i.e., its machine cycle is two-clock or one-clock. In the other words, it can execute one instruction within two clocks or only one clock. The difference between 2T mode and 1T mode are given in the example in Fig. 1-1.

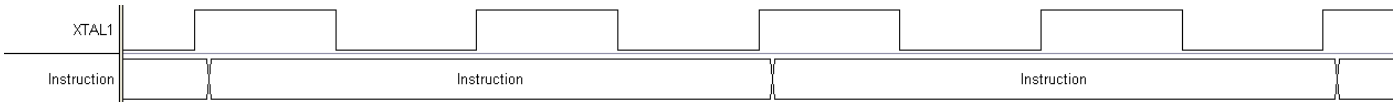


Fig. 1-1(a): The waveform of internal instruction signal in 2T mode

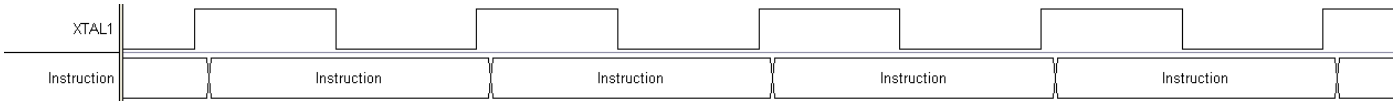


Fig. 1-1(b): The waveform of internal instruction signal in 1T mode

The default is in 2T mode, and it can be changed to 1T mode if IFCON [7] (at address 8Fh) is set to high any time. Not every instruction can be executed with one machine cycle. The exact machine cycle number for all the instructions are given in the next section.

1.4. RESET

1.4.1. Hardware RESET function

SM59R02G1 provides Internal reset circuit inside，the Internal reset time can set by writer or ISP。

Internal Reset time
25ms (default)
200ms
100ms
50ms
16ms
8ms
4ms

1.4.2. Software RESET function

SM59R02G1 provides one software reset mechanism to reset whole chip. To perform a software reset, the firmware must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the Software Reset register (SWRES) write attribute. After SWRES register obtain the write authority, the firmware can write FFh to the SWRES register. The hardware will decode a reset signal that “OR” with the other hardware reset. The SWRES register is self-reset at the end of the software reset procedure.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Software Reset function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
SWRES	Software Reset register	E7h	SWRES [7:0]								00H
RSTS	Reset Status Flag register	A1h	-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

1.4.3. Time Access Key register (TAKEY)

Mnemonic: TAKEY **Address: F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Software reset register (SWRES) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SWRES register write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

1.4.4. Software Reset register (SWRES)

Mnemonic: SWRES **Address: E7H**

7	6	5	4	3	2	1	0	Reset
SWRES [7:0]								00H

SWRES [7:0]: Software reset register bit. These 8-bit is self-reset at the end of the reset procedure.
SWRES [7:0] = FFh, software reset.
SWRES [7:0] = 00h ~ FEh, MCU no action.

1.4.5. Reset Status Flag(RSTS)

Mnemonic: RSTS **Address: A1H**

7	6	5	4	3	2	1	0	Reset
-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

PDRF: Pad reset flag.
When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.
WDTF: Watchdog timer reset flag.
When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software.
SWRF: Software reset flag.
When MCU is reset by software, SWRF flag will be set to one by hardware. This flag clear by software.
LVRF: Low voltage reset flag.
When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.
PORF: Power on reset flag.
When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

1.4.6. Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah    ; enable SWRES write attribute
MOV SWRES, #FFh    ; software reset MCU
```

1.5. Clocks

The default clock is the 22.1184MHz Internal OSC. This clock is used during the initialization stage. The major work of the initialization stage is to determine the clock source used in normal operation.

The internal clock sources are from the internal OSC with difference frequency division as given in table 1-1, the clock source can set by writer。

Table 1-1: Selection of clock source

Clock source
external crystal
External OSC into Xtal1
22.1184 MHz from internal OSC(default)
11.0592MHz from internal OSC
5.5296MHz from internal OSC
2.7648MHz from internal OSC
1.3824MHz from internal OSC

The internal OSC have ±2% variance at room temperature.

2. Instruction Set

All SM59R02G1 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables give a summary of the instruction set cycles of the SM59R02G1 Microcontroller core.

Table 2-1: Arithmetic operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	28-2F	1	1
ADD A,direct	Add direct byte to accumulator	25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A,#data	Add immediate data to accumulator	24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A,#data	Add immediate data to A with carry flag	34	2	2
SUBB A,Rn	Subtract register from A with borrow	98-9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

Table 2-2: Logic operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	58-5F	1	1
ANL A,direct	AND direct byte to accumulator	55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A,#data	AND immediate data to accumulator	54	2	2
ANL direct,A	AND accumulator to direct byte	52	2	3
ANL direct,#data	AND immediate data to direct byte	53	3	4
ORL A,Rn	OR register to accumulator	48-4F	1	1
ORL A,direct	OR direct byte to accumulator	45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A,#data	OR immediate data to accumulator	44	2	2
ORL direct,A	OR accumulator to direct byte	42	2	3
ORL direct,#data	OR immediate data to direct byte	43	3	4
XRL A,Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RLC A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

Table 2-3: Data transfer

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	E8-EF	1	1
MOV A,direct	Move direct byte to accumulator	E5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	E6-E7	1	2
MOV A,#data	Move immediate data to accumulator	74	2	2
MOV Rn,A	Move accumulator to register	F8-FF	1	2
MOV Rn,direct	Move direct byte to register	A8-AF	2	4
MOV Rn,#data	Move immediate data to register	78-7F	2	2
MOV direct,A	Move accumulator to direct byte	F5	2	3
MOV direct,Rn	Move register to direct byte	88-8F	2	3
MOV direct1,direct2	Move direct byte to direct byte	85	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct,#data	Move immediate data to direct byte	75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri,#data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A,@A+PC	Move code byte relative to PC to accumulator	83	1	3
MOVX A,@Ri	Move external RAM (8-bit addr.) to A	E2-E3	1	3
MOVX A,@DPTR	Move external RAM (16-bit addr.) to A	E0	1	3
MOVX @Ri,A	Move A to external RAM (8-bit addr.)	F2-F3	1	4
MOVX @DPTR,A	Move A to external RAM (16-bit addr.)	F0	1	4
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A,Rn	Exchange register with accumulator	C8-CF	1	2
XCH A,direct	Exchange direct byte with accumulator	C5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A,@Ri	Exchange low-order nibble indir. RAM with A	D6-D7	1	3

Table 2-4: Program branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LJMP addr16	Long iump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit,rel	Jump if direct bit is set	20	3	4
JNB bit,rel	Jump if direct bit is not set	30	3	4
JBC bit,direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A,direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A,#data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	B8-BF	3	4
CJNE @Ri,#data rel	Compare immed. to ind. and jump if not equal	B6-B7	3	4
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct,rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

Table 2-5: Boolean manipulation

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C,bit	AND direct bit to carry flag	82	2	2
ANL C,/bit	AND complement of direct bit to carry	B0	2	2
ORL C,bit	OR direct bit to carry flag	72	2	2
ORL C,/bit	OR complement of direct bit to carry	A0	2	2
MOV C,bit	Move direct bit to carry flag	A2	2	2
MOV bit,C	Move carry flag to direct bit	92	2	3

3. Memory Structure

The SM59R02G1 memory structure follows general 8052 structure. It is 8KB program memory.

3.1. Program Memory

The SM59R02G1 has 8KB on-chip flash memory which can be used as general program memory or EEPROM, on which include up to 1K byte specific ISP service program memory space. The address range for the 8K byte is $0000 to $1FFF. The address range for the ISP service program is $1C00 to $1FFF. The ISP service program size can be partitioned as N blocks of 256 byte (N=0 to 4). When N=0 means no ISP service program space available, total 8K byte memory used as program memory. When N=1 means address $1F00 to $1FFF reserved for ISP service program. When N=2 means memory address $1E00 to $1FFF reserved for ISP service program…etc. Value N can be set and programmed into SM59R02G1 information block by writer. It can be used to record any data as EEPROM. The procedure of this EEPROM application function is described in the section 13 on internal ISP.

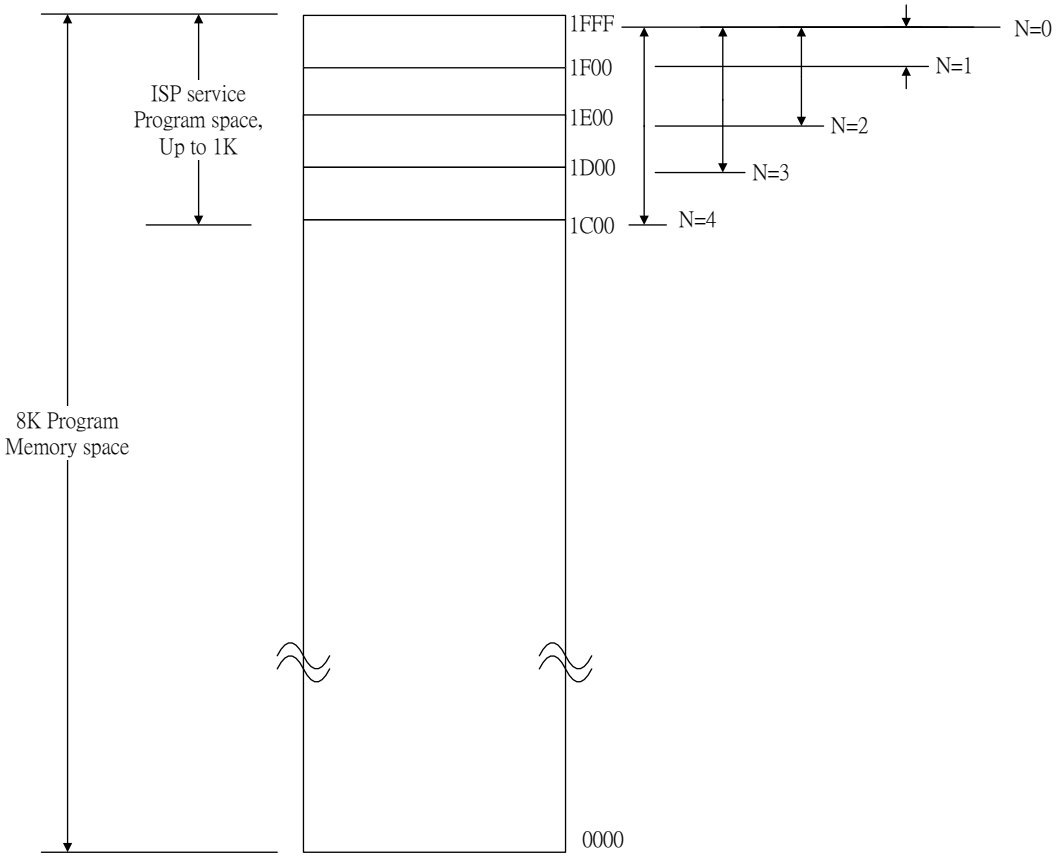


Fig. 3-1: SM59R02G1 programmable Flash

3.2. Data Memory

The SM59R02G1 has 256Bytes on-chip SRAM, 256 Bytes are the same as general 8052 internal memory structure.

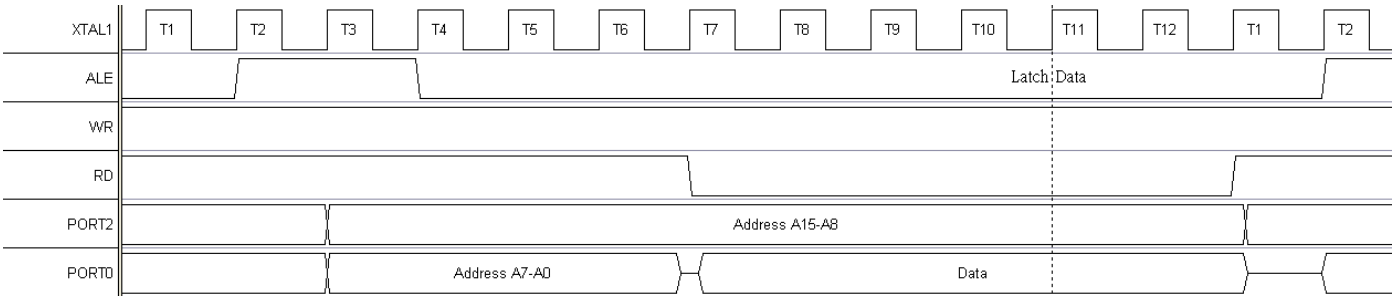


Fig 3-2 (a)：External memory access as read

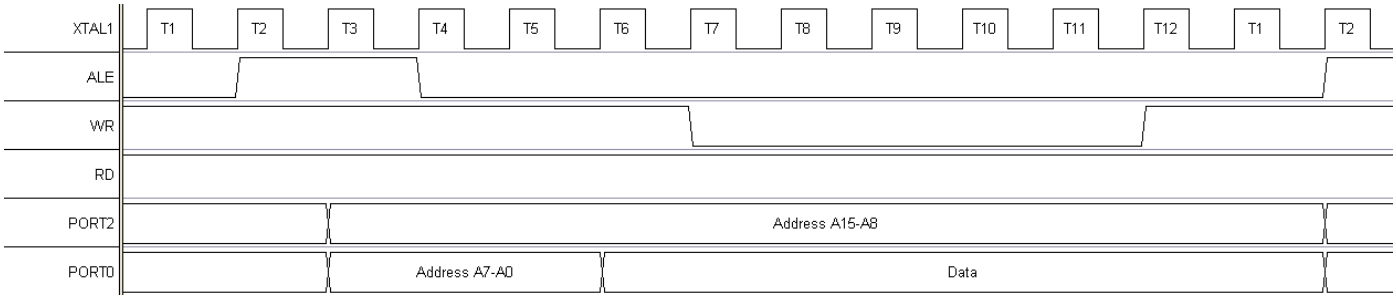


Fig 3-2 (b)：External memory access as write

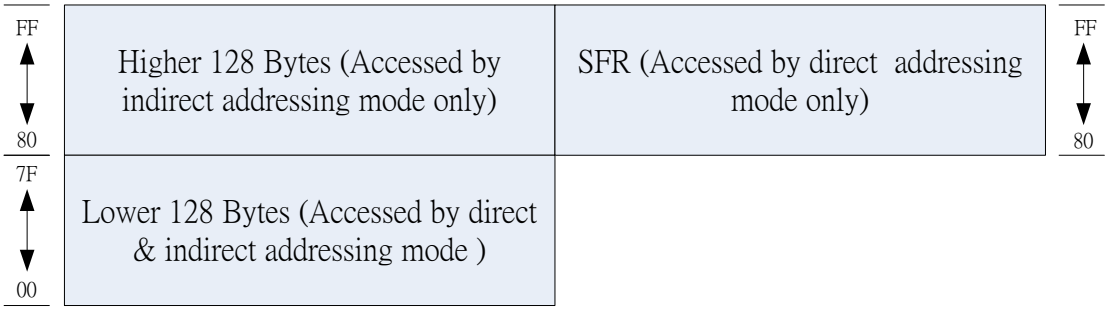


Fig. 3-3: RAM architecture

3.2.1. Data memory - lower 128 byte (00h to 7Fh)

Data memory 00h to FFh is the same as 8052.
The address 00h to 7Fh can be accessed by direct and indirect addressing modes.
Address 00h to 1Fh is register area.
Address 20h to 2Fh is memory bit area.
Address 30h to 7Fh is for general memory area.

3.2.2. Data memory - higher 128 byte (80h to FFh)

The address 80h to FFh can be accessed by indirect addressing mode.
Address 80h to FFh is data area.

4. CPU Engine

The SM59R02G1 engine is composed of four components:

a. Control unit
b. Arithmetic – logic unit
c. Memory control unit
d. RAM and SFR control unit

The SM59R02G1 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The following paragraphs describe the main engine registers.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
8051 Core											
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	PSW.1	P	00H
SP	Stack Pointer	81h	SP[7:0]								07H
DPL	Data pointer low 0	82h	DPL[7:0]								00H
DPH	Data pointer high 0	83h	DPH[7:0]								00H
DPL1	Data pointer low 1	84h	DPL1[7:0]								00H
DPH1	Data pointer high 1	85h	DPH1[7:0]								00H
AUX	Auxiliary register	91h	BRGS	-	-	P1UR	-	-	-	DPS	00H
IFCON	Interface control register	8Fh	ITS	CDPR	-	-	ALEC[1:0]		-	ISPE	00H

4.1. Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to store the operand.

Mnemonic: ACC **Address: E0h**

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC05	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator.

4.2. B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

Mnemonic: B **Address: F0h**

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

4.3. Program Status Word

Mnemonic: PSW **Address: D0h**

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS [1:0]		OV	F1	P	00h

CY: Carry flag.
AC: Auxiliary Carry flag for BCD operations.
F0: General purpose Flag 0 available for user.
RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00h – 07h
01	Bank 1	08h – 0Fh
10	Bank 2	10h – 17h
11	Bank 3	18h – 1Fh

OV: Overflow flag.
F1: General purpose Flag 1 available for user.
P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, i.e. even parity.

4.4. Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08h.

Mnemonic: SP **Address: 81h**

7	6	5	4	3	2	1	0	Reset
SP [7:0]								07h

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5. Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR, #data16) or as two separate registers (e.g. MOV DPL,#data8). It is generally used to access the external code or data space (e.g. MOVC A, @A+DPTR or MOVX A, @DPTR respectively).

Mnemonic: DPL **Address: 82h**

7	6	5	4	3	2	1	0	Reset
DPL [7:0]								00h

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH **Address: 83h**

7	6	5	4	3	2	1	0	Reset
DPH [7:0]								00h

DPH [7:0]: Data pointer High 0

4.6. Data Pointer 1

The Dual Data Pointer accelerates the moves of data block. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the SM59R02G1 core the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located in LSB of AUX register (DPS).

The user switches between pointers by toggling the LSB of AUX register. All DPTR-related instructions use the currently selected DPTR for any activity.

Mnemonic: DPL1 **Address: 84h**

7	6	5	4	3	2	1	0	Reset
DPL1 [7:0]								00h

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1 **Address: 85h**

7	6	5	4	3	2	1	0	Reset
DPH1 [7:0]								00h

DPH1[7:0]: Data pointer High 1

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	P1UR	-	-	-	DPS	00H

DPS: Data Pointer selects register.
DPS = 1 is selected DPTR1.

4.7. Interface control register

Mnemonic: IFCON **Address: 8Fh**

7	6	5	4	3	2	1	0	Reset
ITS	CDPR	-	-	ALEC[1:0]		-	ISPE	00h

ITS: Instruction timing select. (default is 2T)
ITS = 0, 2T instruction mode.
ITS = 1, 1T instruction mode.
CDPR: code protect (Read Only)
ALEC[1:0]: ALE output control register.

ALEC[1:0]	ALE Output
00	Always output
01	No ALE output
10	Only Read or Write have ALE output
11	reserved

ISPE: ISP function enable bit
ISPE = 1, enable ISP function
ISPE = 0, disable ISP function

5. GPIO

The SM59R02G1 has six I/O ports: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 3, 4 are 8-bit ports and Port 5 is a 2-bit port (Only Bit 4 and Bit 5). These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin. All I/O port pins on the SM59R02G1 may be configured by software to one of four types on a pin-by-pin basis, shown as below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P0M0	Port 0 output mode 0	D2h	P0M0 [7:0]								00H
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								00H
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								00H
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								00H
P2M0	Port 2 output mode 0	D6h	P2M0[7:0]								00H
P2M1	Port 2 output mode 1	D7h	P2M1[7:0]								00H
P3M0	Port 3 output mode 0	DAh	P3M0[7:0]								00H
P3M1	Port 3 output mode 1	DBh	P3M1[7:0]								00H
P4M0	Port 4 output mode 0	DCh	P4M0[7:0]								00H
P4M1	Port 4 output mode 1	DDh	P4M1[7:0]								00H
P5M0	Port 5 output mode 0	DEh	-	-	P5M0[5:4]		-	-	-	-	00H
P5M1	Port 5 output mode 1	DFh	-	-	P5M1[5:4]		-	-	-	-	00H

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

The XTAL2 and XTAL1 can define as P5.4 and P5.5 by writer or ISP. When user use external OSC as system clock and input into XTAL1, only XTAL2 can be defined as P5.4.

For general-purpose applications, every pin can be assigned to either high or low independently as given below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Ports											
Port 5	Port 5	D8h	-	-	P5.5	P5.4	-	-	-	-	FFh
Port 4	Port 4	E8h	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh
Port 3	Port 3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh
Port 2	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

Mnemonic: P0 **Address: 80h**

7	6	5	4	3	2	1	0	Reset
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

P0.7~ 0: Port0 [7] ~ Port0 [0]

Mnemonic: P1 **Address: 90h**

7	6	5	4	3	2	1	0	Reset
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh

P1.7~ 0: Port1 [7] ~ Port1 [0]

Mnemonic: P2 **Address: A0h**

7	6	5	4	3	2	1	0	Reset
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh

P2.7~ 0: Port2 [7] ~ Port2 [0]

Mnemonic: P3 **Address: B0h**

7	6	5	4	3	2	1	0	Reset
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh

P3.7~ 0: Port3 [7] ~ Port3 [0]

Mnemonic: P4 **Address: E8h**

7	6	5	4	3	2	1	0	Reset
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh

P4.7~ 0: Port4 [7] ~ Port4 [0]

Mnemonic: P5 **Address: D8h**

7	6	5	4	3	2	1	0	Reset
-	-	P5.5	P5.4	-	-	-	-	FFh

P5.5~ 4: Port5 [5] ~ Port5 [4]

6. Timer 0 and Timer 1

The SM59R02G1 has three 16-bit timer/counter registers: Timer 0, Timer 1 and Timer 2. All can be configured for counter or timer operations.

In timer mode, the Timer 0 register or Timer 1 register is incremented every 1/12/96 machine cycles, which means that it counts up after every 1/12/96 periods of the clk signal. It's dependent on SFR(PFCON).

In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function registers (TMOD and TCON) are used to select the appropriate mode.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Timer 0 and 1											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00h
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00h
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00h
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00h
TMOD	Timer Mode Control	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
TCON	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
PFCON	Peripheral Frequency control register	D9h			S0RELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

6.1. Timer/counter mode control register (TMOD)

Mnemonic: TMOD **Address: 89h**

7	6	5	4	3	2	1	0	Reset
GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
Timer 1				Timer 0				

GATE: If set, enables external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M[1:0]: Selects mode for Timer/Counter 0 or Timer/Counter 1.

M1	M0	Mode	Function
0	0	Mode0	13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode1	16-bit counter/timer.
1	0	Mode2	8 -bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.

1	1	Mode3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters.

6.2. Timer/counter control register (TCON)

Mnemonic: TCON **Address: 88h**

7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.
TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.
TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.
IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.
IT1: Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.
IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.
IT0: Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

6.3. Peripheral Frequency control register(PFCON)

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-	S0RELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

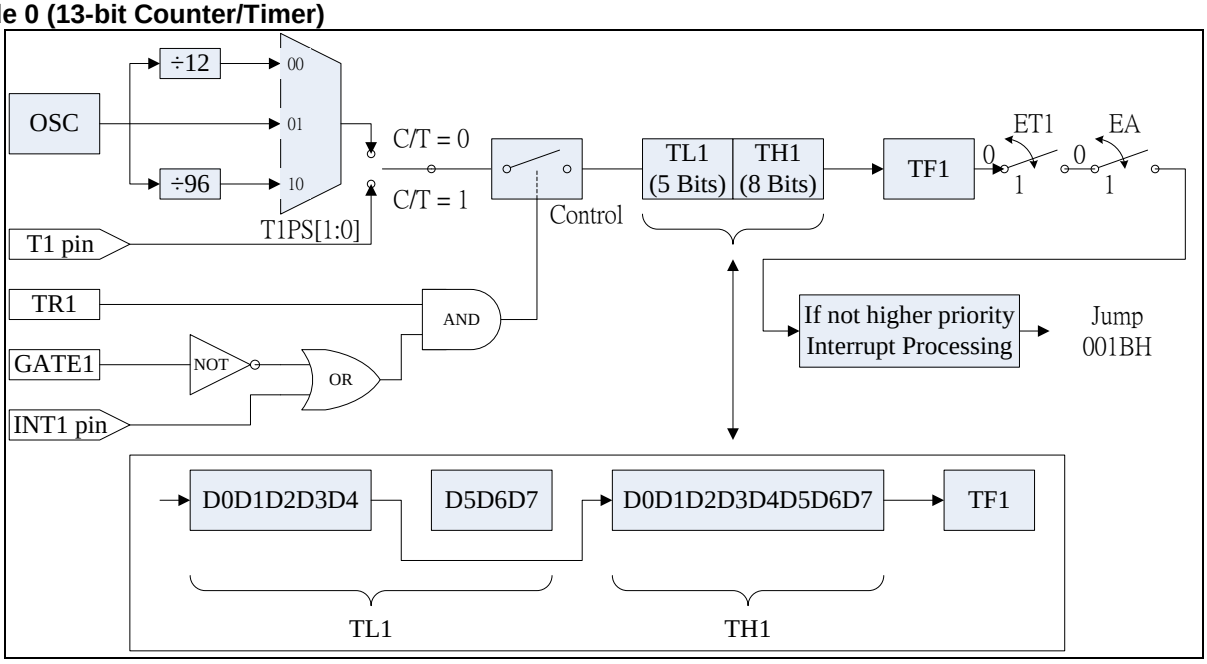
T1PS[1:0]: Timer1 Prescaler select

T1PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

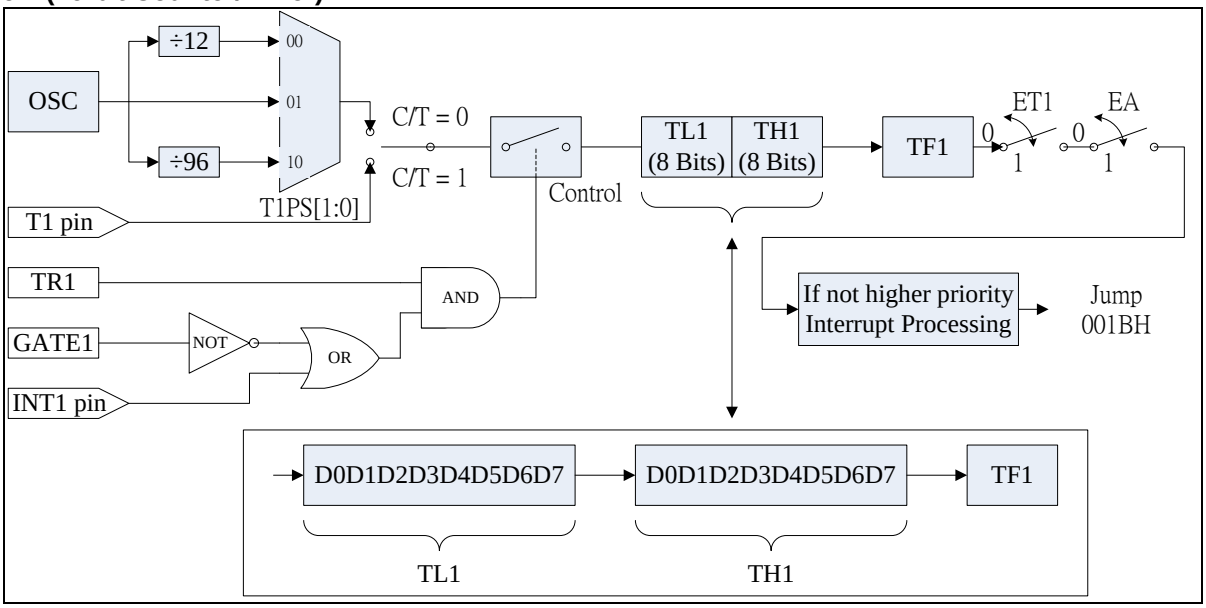
T0PS[1:0]: Timer0 Prescaler select

T0PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

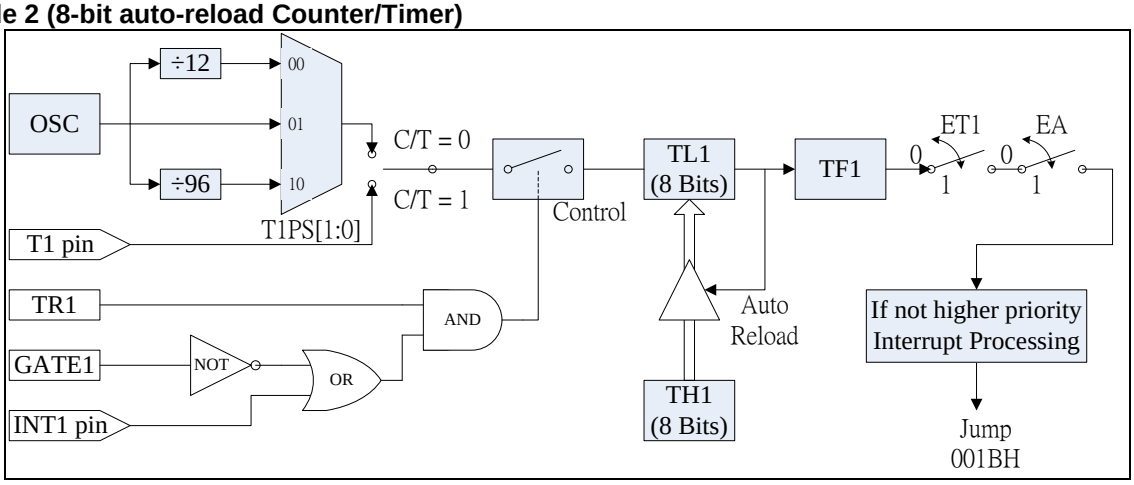
6.4. Mode 0 (13-bit Counter/Timer)



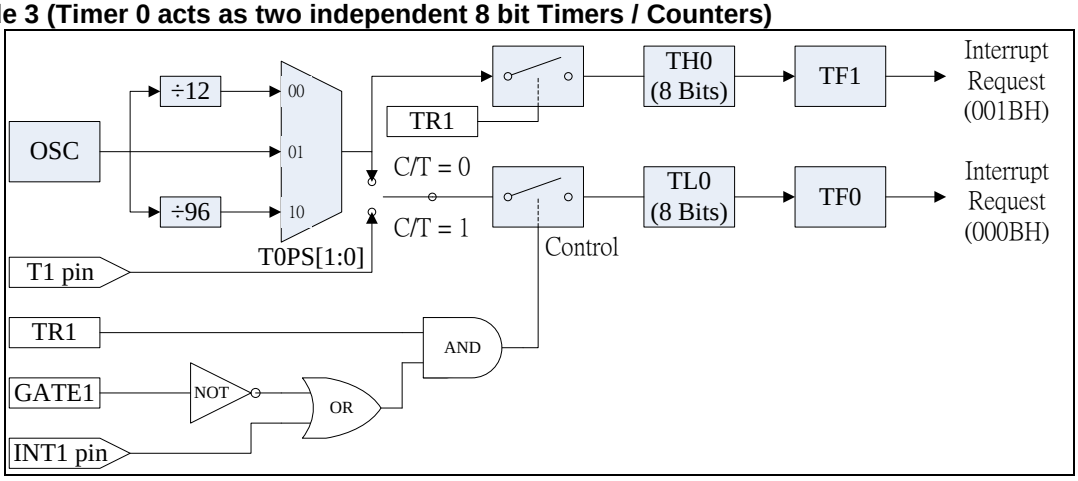
6.5. Mode 1 (16-bit Counter/Timer)



6.6. Mode 2 (8-bit auto-reload Counter/Timer)



6.7. Mode 3 (Timer 0 acts as two independent 8 bit Timers / Counters)



7. Timer 2 and Capture/Compare Unit

Timer 2 is not only a 16-bit timer, also a 4-channel unit with compare, capture and reload functions. It is very similar to the programmable counter array (PCA) in some other MCUs except pulse width modulation (PWM).

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Timer 2 and Capture Compare Unit											
AUX2	Auxiliary register2	92h	-	-	-	-	-	-	P42CC[1:0]		00h
T2CON	Timer 2 control	C8h	T2PS[2:0]			T2R[1:0]		-	T2I[1:0]		00h
CCCON	Compare/Capture Control	C9h	CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H
CCEN	Compare/Capture Enable register	C1h	-	COCAM1[2:0]			-	COCAM0[2:0]			00h
CCEN2	Compare/Capture Enable 2 register	D1h	-	COCAM3[2:0]			-	COCAM2[2:0]			00h
TL2	Timer 2, low byte	CCh	TL2[7:0]								00h
TH2	Timer 2, high byte	CDh	TH2[7:0]								00h
CRCL	Compare/Reload/ Capture register, low byte	CAh	CRCL[7:0]								00h
CRCH	Compare/Reload/ Capture register, high byte	CBh	CRCH[7:0]								00h
CCL1	Compare/Capture register 1, low byte	C2h	CCL1[7:0]								00h
CCH1	Compare/Capture register 1, high byte	C3h	CCH1[7:0]								00h
CCL2	Compare/Capture register 2, low byte	C4h	CCL2[7:0]								00h
CCH2	Compare/Capture register 2, high byte	C5h	CCH2[7:0]								00h
CCL3	Compare/Capture register 3, low byte	C6h	CCL3[7:0]								00h
CCH3	Compare/Capture register 3, high byte	C7h	CCH3[7:0]								00h

Mnemonic: AUX2 **Address: 92h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	P42CC[1: 0]		00H

P42CC[1: 0] 00: Capture/Compare function on Port1.
01: Capture/Compare function on Port2
10: Capture/Compare function on Port4
11: reserved

Mnemonic: T2CON **Address: C8h**

7	6	5	4	3	2	1	0	Reset
T2PS[2:0]			T2R[1:0]		-	T2I[1:0]		00H

T2PS[2:0]: Prescaler select bit:
T2PS = 000 – timer 2 is clocked with the oscillator frequency.
T2PS = 001 – timer 2 is clocked with 1/2 of the oscillator frequency.
T2PS = 010 – timer 2 is clocked with 1/4 of the oscillator frequency.
T2PS = 011 – timer 2 is clocked with 1/6 of the oscillator frequency.
T2PS = 100 – timer 2 is clocked with 1/8 of the oscillator frequency.
T2PS = 101 – timer 2 is clocked with 1/12 of the oscillator frequency.
T2PS = 110 – timer 2 is clocked with 1/24 of the oscillator frequency.
T2R[1:0]: Timer 2 reload mode selection
T2R[1:0] = 0X – Reload disabled
T2R[1:0] = 10 – Mode 0
T2R[1:0] = 11 – Mode 1
T2I[1:0]: Timer 2 input selection
T2I[1:0] = 00 – Timer 2 stop
T2I[1:0] = 01 – Input frequency from prescaler (T2PS[2:0])
T2I[1:0] = 10 – Timer 2 is incremented by external signal at pin T2
T2I[1:0] = 11 – internal clock input is gated to the Timer 2

Mnemonic: CCCON **Address: C9h**

7	6	5	4	3	2	1	0	Reset
CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H

CCI3: Compare/Capture 3 interrupt control bit.
"1" is enable.
CCI2: Compare/Capture 2 interrupt control bit.
"1" is enable.
CCI1: Compare/Capture 1 interrupt control bit.
"1" is enable.
CCI0: Compare/Capture 0 interrupt control bit.
"1" is enable.
CCF3: Compare/Capture 3 flag set by hardware. This flag can be cleared by software.
CCF2: Compare/Capture 2 flag set by hardware. This flag can be cleared by software.
CCF1: Compare/Capture 1 flag set by hardware. This flag can be cleared by software.
CCF0: Compare/Capture 0 flag set by hardware. This flag can be cleared by software.
Compare/Capture interrupt share T2 interrupt vector.

Mnemonic: CCEN **Address: C1h**

7	6	5	4	3	2	1	0	Reset
-	COCAM1[2:0]			-	COCAM0[2:0]			00H

COCAM1[2:0] 000: Compare/Capture disable
001: Compare enable but no output on Pin
010: Compare mode 0
011: Compare mode 1
100: Capture on rising edge at pin CC1
101: Capture on falling edge at pin CC1
110: Capture on both rising and falling edge at pin CC1
111: Capture on write operation into register CC1
COCAM0[2:0] 000: Compare/Capture disable
001: Compare enable but no output on Pin
010: Compare mode 0
011: Compare mode 1

100: Capture on rising edge at pin CC0
101: Capture on falling edge at pin CC0
110: Capture on both rising and falling edge at pin CC0
111: Capture on write operation into register CC0

Mnemonic: CCEN2 **Address: D1h**

7	6 5 4	3	2 1 0	Reset
-	COCAM3[2:0]	-	COCAM2[2:0]	00H

COCAM3[2:0] 000: Compare/Capture disable
001: Compare enable but no output on Pin
010: Compare mode 0
011: Compare mode 1
100: Capture on rising edge at pin CC3
101: Capture on falling edge at pin CC3
110: Capture on both rising and falling edge at pin CC3
111: Capture on write operation into register CC3

COCAM2[2:0] 000: Compare/Capture disable
001: Compare enable but no output on Pin
010: Compare mode 0
011: Compare mode 1
100: Capture on rising edge at pin CC2
101: Capture on falling edge at pin CC2
110: Capture on both rising and falling edge at pin CC2
111: Capture on write operation into register CC2

7.1. Timer 2 function

Timer 2 can operate as timer, event counter, or gated timer as explained later.

7.1.1. Timer mode

In this mode Timer 2 can by incremented in various frequency that depending on the prescaler. The prescaler is selected by bit T2PS[2:0] in register T2CON.

7.1.2. Event counter mode

In this mode, the timer is incremented when external signal T2 change value from 1 to 0. The T2 input is sampled in every cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected.

7.1.3. Gated timer mode

In this mode, the internal clock which incremented timer 2 is gated by external signal T2.

7.1.4. Reload of Timer 2

Reload (16-bit reload from the crc register) can be executed in the following two modes:
Mode 0: Reload signal is generate by a Timer 2 overflows - auto reload
Mode 1: Reload signal is generate by a negative transition at the corresponding input pin T2EX.

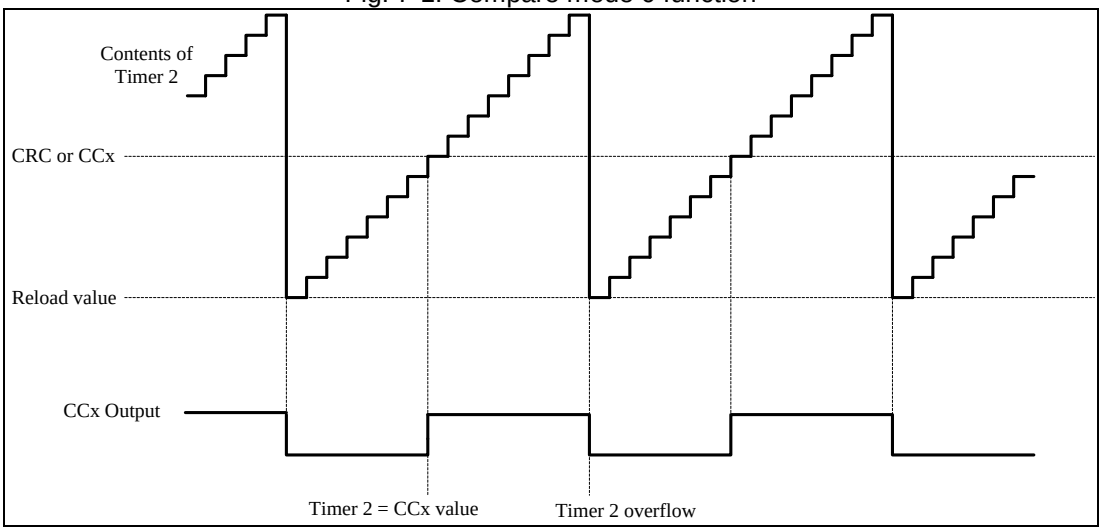
7.2. Compare function

In the four independent comparators, the value stored in any compare/capture register is compared with the contents of the timer register. The compare modes 0 and 1 are selected by bit T2CM. In both compare modes, the results of comparison arrives at Port 1 within the same machine cycle in which the internal compare signal is activated.

7.2.1. Compare Mode 0

In mode 0, when the value in Timer 2 equals the value of the compare register, the output signal changes from low to high. It goes back to a low level on timer overflow. In this mode, writing to the port will have no effect, because the input line from the internal bus and the write-to-latch line are disconnected. The following figure illustrates the function of compare mode 0.

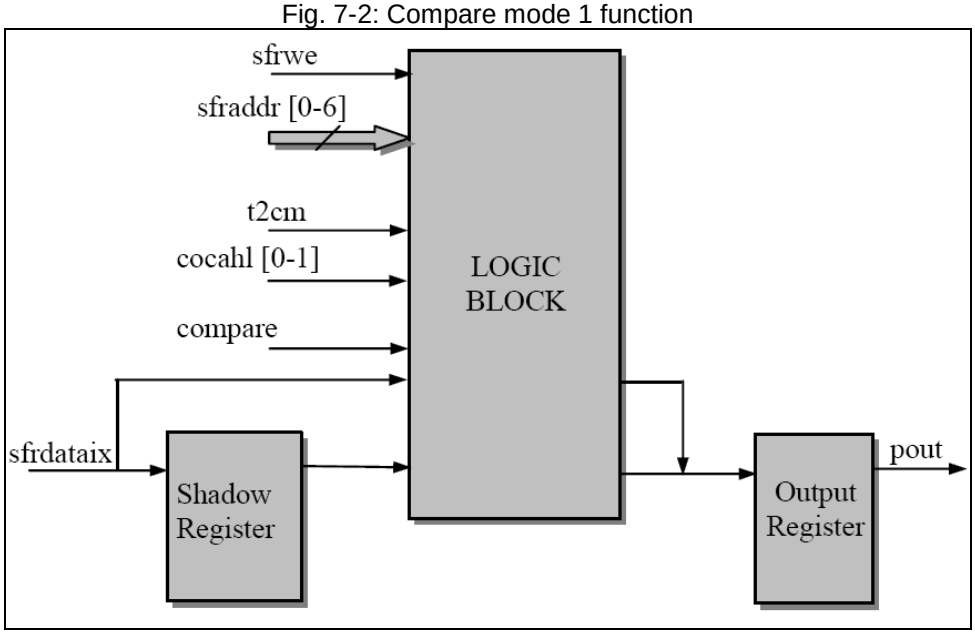
Fig. 7-1: Compare mode 0 function

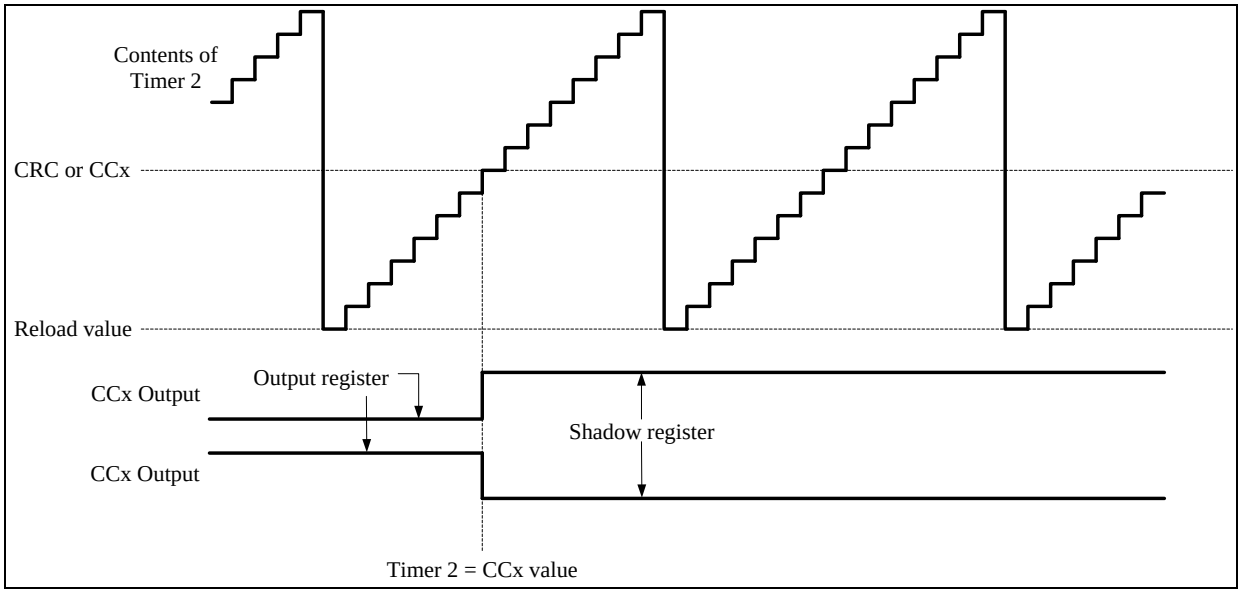


7.2.2. Compare Mode 1

In compare mode 1, the transition of the output signal can be determined by software. A timer 2 overflow causes no output change. In this mode, both transitions of a signal can be controlled. Fig. 7-2 shows a functional diagram of a register/port configuration in compare Mode 1. In compare Mode 1, the value is written first to the “Shadow Register”, when compare signal is active, this value is transferred to the output register.

Fig. 7-2: Compare mode 1 function





7.3. Capture function

Actual timer/counter contents can be saved into registers CCx or CRC upon an external event (mode 0) or a software write operation (mode 1).

7.3.1. Capture Mode 0

In mode 0, value capture of Timer 2 is executed when:
(a) Rising edge on input CC0-CC3
(b) Falling edge on input CC0-CC3
(c) Both rising and falling edge on input CC0-CC3
The contents of Timer 2 will be latched into the appropriate capture register.

7.3.2. Capture Mode 1

In mode 1, value capture of timer 2 is caused by writing any value into the low-order byte of the dedicated capture register. The value written to the capture register is irrelevant to this function. The contents of Timer 2 will be latched into the appropriate capture register.

8. Serial interface 0

As the conventional UART, the communication speed can be selected by configuring the baud rate in SFRs.

These two serial buffers consists of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR S0BUF sets this data in serial output buffer and starts the transmission. Reading from the S0BUF reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Serial interface 0											
PCON	Power control	87h	SMOD	-	-	-	-	-	STOP	IDLE	40h
AUX	Auxiliary register	91h	BRGS	-	-	P1UR	-	-	-	DPS	00H
S0CON	Serial Port 0 control register	98h	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0	00h
S0RELL	Serial Port 0 reload register low byte	AAh	S0REL .7	S0REL .6	S0REL .5	S0REL .4	S0REL .3	S0REL .2	S0REL .1	S0REL .0	00h
S0RELH	Serial Port 0 reload register high byte	BAh	-	-	-	-	-	-	S0REL .9	S0REL .8	00h
S0BUF	Serial Port 0 data buffer	99h	S0BUF[7:0]								00h
PFCON	Peripheral Frequency control register	D9H			S0RELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	-	-	P1UR	-	-	-	DPS	00H

BRGS: Baud rate generator.
BRGS = 0 - baud rate generator from Timer 1.
BRGS = 1 - baud rate generator by S0REL.
P1UR: P1UR = 0 – Serial interface function on P3.
P1UR = 1 – Serial interface function on P1.

Mnemonic: S0CON **Address: 98h**

7	6	5	4	3	2	1	0	Reset
SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0	00h

SM0,SM1: Serial Port 0 mode selection.

SM0	SM1	Mode
0	0	0
0	1	1
1	0	2
1	1	3

The 4 modes in UART0, Mode 0 ~ 3, are explained later.

SM20: Enables multiprocessor communication feature
REN0: If set, enables serial reception. Cleared by software to disable reception.
TB80: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB80: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM20 is 0, RB80 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.
TI0: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
RI0: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

Mnemonic: PFCON **Address: D9H**

7	6	5 4	3 2	1 0	Reset
-	-	S0RELPS[1:0]	T1PS[1:0]	T0PS[1:0]	00H

S0RELPS[1:0]: S0REL Prescaler select

S0RELPS[1:0]	Prescaler
00	Fosc/64
01	Fosc/32

T1PS[1:0]: Timer 1 Prescaler select

T1PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

8.1. Serial interface 0

The Serial Interface 0 can operate in the following 4 modes:

SM0	SM1	Mode	Description	Board Rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Variable

Here Fosc is the crystal or oscillator frequency.

8.1.1. Mode 0

Pin RXD0 serves as input and output. TXD0 outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In the other modes, a start bit when REN0 = 1 starts receiving serial data.

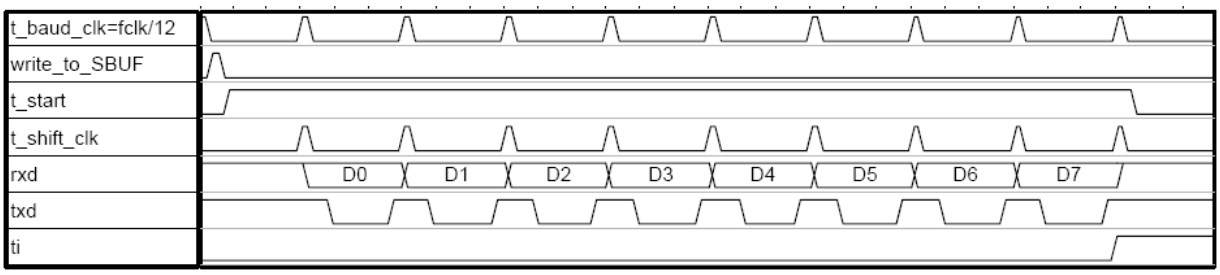


Fig. 8-1: Transmit mode 0 for Serial 0

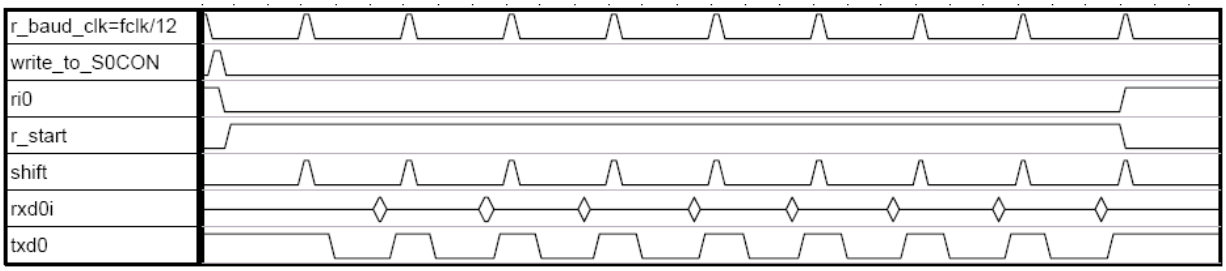


Fig. 8-2: Receive mode 0 for Serial 0

8.1.2. Mode 1

Here Pin RXD0 serves as input, and TXD0 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and a stop bit sets the flag RB80 in the SFR S0CON. In mode 1, either internal baud rate generator or timer 1 can be use to specify the desired baud rate.

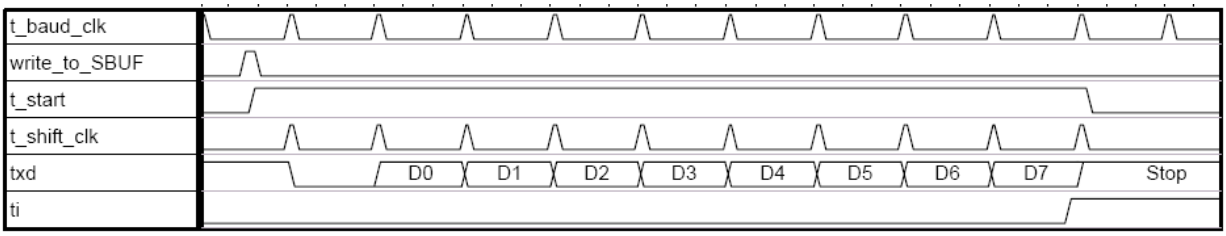


Fig. 8-3: Transmit mode 1 for Serial 0

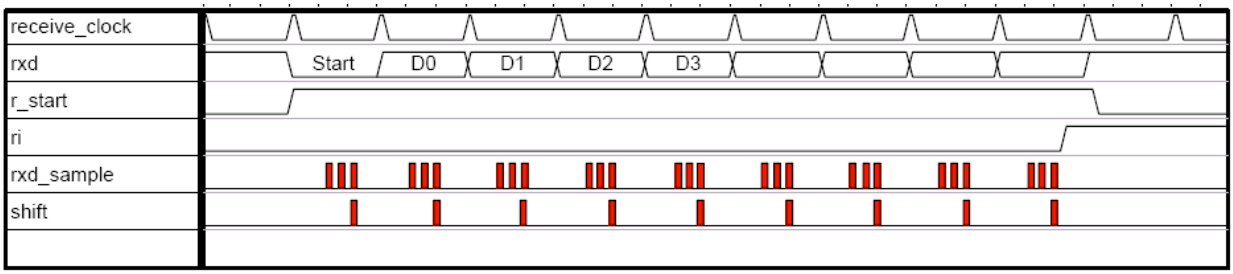


Fig. 8-4: Receive mode 1 for Serial 0

8.1.3. Mode 2

This mode is similar to Mode 1, but with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64(SMOD=0) of oscillator frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable Bit 9, and a stop bit (1). Bit 9 can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as Bit 9, and at receive, Bit 9 affects RB80 in SFR S0CON.

8.1.4. Mode 3

The only difference between Mode 2 and Mode 3 is that: in Mode 3, either internal baud rate generator or timer 1 can be use to specify baud rate.

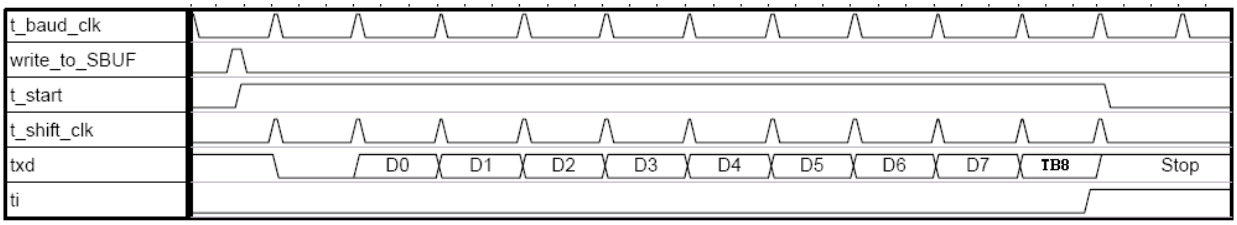


Fig. 8-5: Transmit modes 2 and 3 for Serial 0

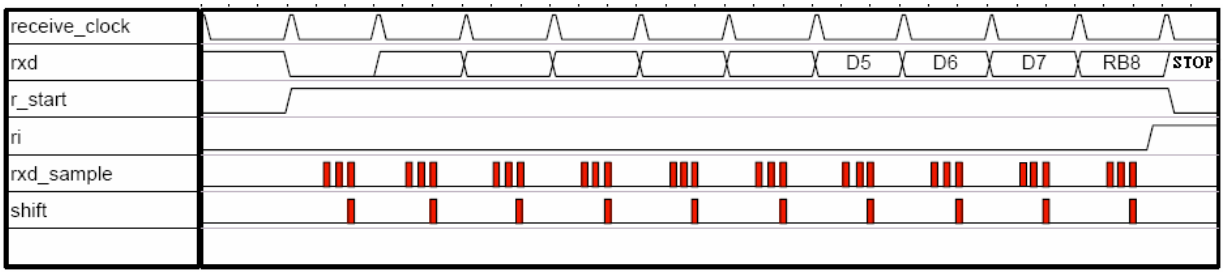


Fig. 8-6: Receive modes 2 and 3 for Serial 0

8.2. Multiprocessor communication of Serial Interface 0

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface 0 can be used for multiprocessor communication. In this case, the slave processors have bit SM20 in S0CON set to 1. When the master processor outputs slave's address, it sets the Bit 9 to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If matched, the addressed slave will clear SM20 and receive the rest of the message, while other slaves will leave SM20 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the Bit 9 set to 0, so no serial port receive interrupt will be generated in unselected slaves.

8.3. Baud rate generator

8.3.1. Serial interface 0 modes 1 and 3

(a) When BRGS = 0 (in SFR AUX):

T1PS[1:0] = 00

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{32 \times 12 \times (256 - \text{TH1})}$$

T1PS[1:0] = 01

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{32 \times (256 - \text{TH1})}$$

T1PS[1:0] = 10

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{32 \times 96 \times (256 - \text{TH1})}$$

(b) When BRGS = 1 (in SFR AUX):

S0RELPS[1:0] = 00

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{64 \times (2^{10} - \text{S0REL})}$$

S0RELPS[1:0] = 01

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{OSC}}{32 \times (2^{10} - \text{S0REL})}$$

9. Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDTF bit of WDTC register whenever un-predicted reset happened. After an external reset the watchdog timer is disabled and all registers are set to zeros.

The watchdog timer has a free running on-chip RC oscillator (250KHz). The WDT will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the MCU to reset. The WDT can be enabled or disabled any time during the normal mode. Please refer the WDTE bit of WDTC register. The default WDT time-out period is approximately 16.38ms (WDTM [3:0] = 0100b).

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit3 ~ bit0 (WDTM [3:0]) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

$$WDTCLK = \frac{250\text{KHz}}{2^{\text{WDTM}}}$$

$$\text{Watchdog reset time} = \frac{256}{\text{WDTCLK}}$$

Table 9.1 WDT time-out period

WDTM [3:0]	Divider (250 KHz RC oscillator in)	Time period @ 250KHz
0000	1	1.02ms
0001	2	2.05ms
0010	4	4.10ms
0011	8	8.19ms
0100	16	16.38ms (default)
0101	32	32.77ms
0110	64	65.54ms
0111	128	131.07ms
1000	256	262.14ms
1001	512	524.29ms
1010	1024	1.05s
1011	2048	2.10s
1100	4096	4.19s
1101	8192	8.39s
1110	16384	16.78s
1111	32768	33.55s

When MCU is reset, the MCU will be read WDTEN control bit status. When WDTEN bit is set to 1, the watchdog function will be disabled no matter what the WDTE bit status is. When WDTEN bit is clear to 0, the watchdog function will be enabled if WDTE bit is set to 1 by program. User can to set WDTEN on the writer or ISP.

The program can enable the WDT function by programming 1 to the WDTE bit premise that WDTEN control bit is clear to 0. After WDTE set to 1, the 8 bit-counter starts to count with the selected time base source clock which set by WDTM [3:0]. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when MCU been reset, either hardware reset or WDT reset.

Once the watchdog is started it cannot be stopped. User can refreshed the watchdog timer to zero by writing 0x55 to Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start to count from the beginning. The watchdog timer must be refreshed regularly to prevent reset request signal from

becoming active.

When Watchdog timer is overflow, the WDTF flag will set to one and automatically reset MCU. The WDTF flag can be clear by software or external reset or power on reset.

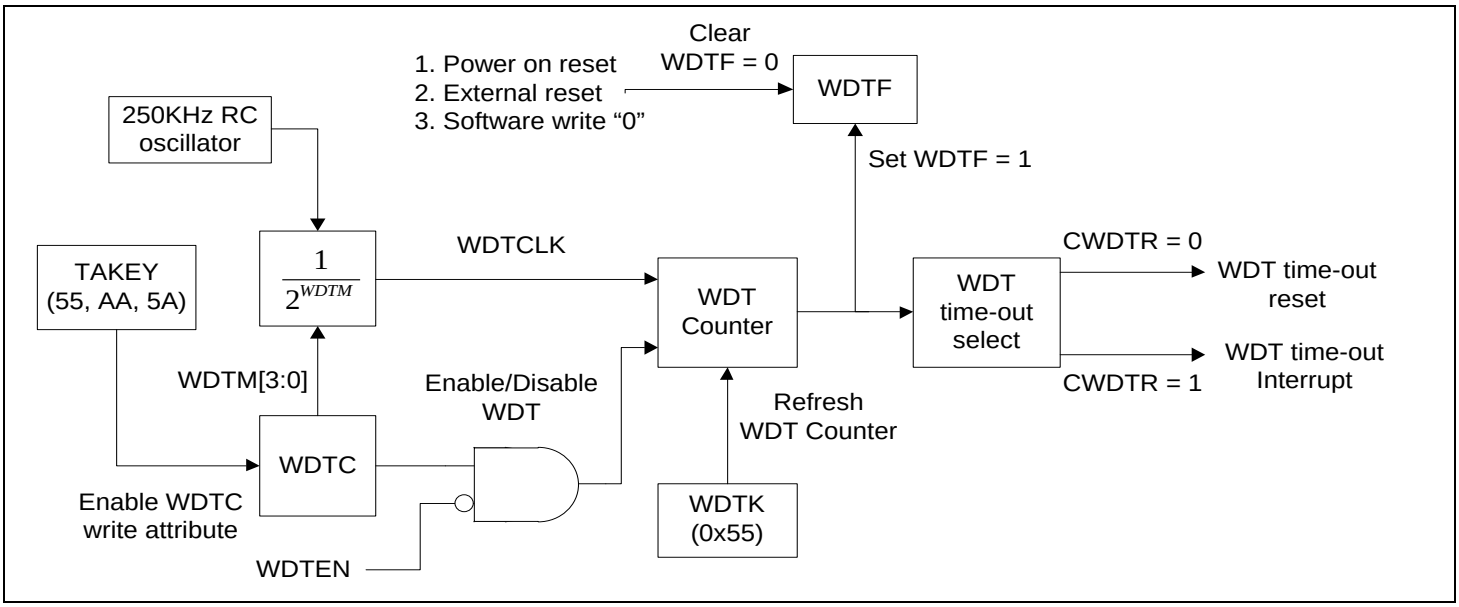


Fig. 9-1: Watchdog timer block diagram

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Watchdog Timer											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
WDTC	Watchdog timer control register	B6h	-	CWDTR	WDTE	-	WDTM [3:0]				04H
WDTK	Watchdog timer refresh key	B7h	WDTK[7:0]								00H
RSTS	Reset Status Flag register	A1h	-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

Mnemonic: TAKEY **Address: F7h**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Watchdog timer control register (WDTC) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the WDTC write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

Mnemonic: WDTC **Address: B6h**

7	6	5	4	3	2	1	0	Reset
-	CWDTR	WDTE	-	WDTM [3:0]				04H

CWDTR: 0: watchdog reset
1: watchdog interrupt
WDTE: Control bit used to enable Watchdog timer.

The WDTE bit can be used only if WDTEN is "0". If the WDTEN bit is "0", then WDT can be disabled / enabled by the WDTE bit.
0: Disable WDT.
1: Enable WDT.
The WDTE bit is not used if WDTEN is "1". That is, if the WDTEN bit is "1", WDT is always disabled no matter what the WDTE bit status is. The WDTE bit can be read and written.

WDTM [3:0]: WDT clock source divider bit. Please see table 7.8.1 to reference the WDT time-out period.

Mnemonic: WDTK **Address: B7h**

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00h

WDTK: Watchdog timer refresh key.
A programmer must write 0x55 into WDTK register, and then the watchdog timer will be cleared to zero.

For example, if enable WDT and select time-out reset period is 327.68ms.
First, programming the information block OP3 bit7 WDTEN to “0”.
Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah          ; enable WDTC write attribute.
MOV WDTC, #28h           ; Set WDTM [3:0] = 1000b. Set WDTE =1 to enable WDT
                         ; function.
.
.
MOV WDTK, #55h           ; Clear WDT timer to 0.
```

Mnemonic: RSTS **Address: B6h**

7	6	5	4	3	2	1	0	Reset
-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

WDTF: Watchdog timer reset flag.
When MCU is reset by watchdog, WDTF flag will be set to one by hardware.
This flag clear by software or external reset or power on reset.

10. Interrupt

The SM59R02G1 provides 7 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register. Each interrupt requested by the corresponding flag could individually be enabled or disabled by the enable bits in SFR's IEN0, IEN1 and IEN2.

When the interrupt occurs, the engine will vector to the predetermined address as shown in Table 10.1. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When an RETI is performed, the processor will return to the instruction that would have been next when interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then interrupt request flag is set. On the next instruction cycle the interrupt will be acknowledged by hardware forcing an LCALL to appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of microcontroller when the interrupt occurs. If microcontroller is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles for perform the LCALL.

Table 10-1: Interrupt vectors

Interrupt Request Flags	Interrupt Vector Address	Interrupt Number *(use Keil C Tool)
IE0 – External interrupt 0	0003h	0
TF0 – Timer 0 interrupt	000Bh	1
IE1 – External interrupt 1	0013h	2
TF1 – Timer 1 interrupt	001Bh	3
RI0/TI0 – Serial channel 0 interrupt	0023h	4
TF2/EXF2 – Timer 2 interrupt	002Bh	5
WDT interrupt	008Bh	17

*See Keil C about C51 User's Guide about Interrupt Function description

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Interrupt											
IEN0	Interrupt Enable 0 register	A8h	EA	-	ET2	ES0	ET1	EX1	ET0	EX0	00h
IEN1	Interrupt Enable 1 register	B8h	EXEN2	-	-	-	-	-	-	-	00h
IRCON	Interrupt request register	C0H	EXF2	TF2	-	-	-	-	-	-	00h
IEN2	Interrupt Enable 2 register	9AH	-	-	-	-	-	-	IEWDT	-	00h
IRCON2	Interrupt request register 2	97H	-	-	-	-	-	-	WDTIF	-	00h
IP0	Interrupt priority level 0	A9h	-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h
IP1	Interrupt priority level 1	B9h	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h

Interrupt Enable 0 register(IEN0)

Mnemonic: IEN0 **Address: A8h**

7	6	5	4	3	2	1	0	Reset
EA	-	ET2	ES0	ET1	EX1	ET0	EX0	00h

EA: EA=0 – Disable all interrupt.
EA=1 – Enable all interrupt.

ET2: ET2=0 – Disable Timer 2 overflow or external reload interrupt.
ET2=1 – Enable Timer 2 overflow or external reload interrupt.

ES0: ES0=0 – Disable Serial channel 0 interrupt.
ES0=1 – Enable Serial channel 0 interrupt.

ET1: ET1=0 – Disable Timer 1 overflow interrupt.
ET1=1 – Enable Timer 1 overflow interrupt.

EX1: EX1=0 – Disable external interrupt 1.
EX1=1 – Enable external interrupt 1.

ET0: ET0=0 – Disable Timer 0 overflow interrupt.
ET0=1 – Enable Timer 0 overflow interrupt.

EX0: EX0=0 – Disable external interrupt 0.
EX0=1 – Enable external interrupt 0.

Interrupt Enable 1 register(IEN1)

Mnemonic: IEN1 **Address: B8h**

7	6	5	4	3	2	1	0	Reset
EXEN2	-	-	-	-	-	-	-	00h

EXEN2: Timer 2 reload interrupt enable.
EXEN2 = 0 – Disable Timer 2 external reload interrupt.
EXEN2 = 1 – Enable Timer 2 external reload interrupt.

Interrupt Enable 2 register(IEN2)

Mnemonic: IEN2 **Address: 9Ah**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	IEWDT	-	00h

IEWDT: WDT interrupt enable..
IEWDT = 0 – Disable WDT interrupt.
IEWDT = 1 – Enable WDT interrupt.

Interrupt request register(IRCON)

Mnemonic: IRCON **Address: C0h**

7	6	5	4	3	2	1	0	Reset
EXF2	TF2	-	-	-	-	-	-	00H

EXF2: Timer 2 external reloads flag. Must be cleared by software.
TF2: Timer 2 overflows flag. Must be cleared by software.

Interrupt request register 2(IRCON2)

Mnemonic: IRCON2 **Address: 97h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	WDTIF	-	00H

WDTIF: WDT interrupt flag.

Priority level structure

All interrupt sources are combined in groups:

Table 10-2: Priority level groups

Groups	
External interrupt 0	-
Timer 0 interrupt	-
External interrupt 1	WDT interrupt
Timer 1 interrupt	-
Serial channel 0 interrupt	-
Timer 2 interrupt	-

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first.

Mnemonic: IP0 **Address: A9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h

Mnemonic: IP1 **Address: B9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h

Table 10-3: Priority levels

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 10-4: Groups of priority

Bit	Group	
IP1.0, IP0.0	External interrupt 0	-
IP1.1, IP0.1	Timer 0 interrupt	WDT interrupt
IP1.2, IP0.2	External interrupt 1	-
IP1.3, IP0.3	Timer 1 interrupt	-
IP1.4, IP0.4	Serial channel 0 interrupt	-
IP1.5, IP0.5	Timer 2 interrupt	-

Table 10-5: Polling sequence

Interrupt source	Sequence
External interrupt 0	Polling sequence ↓
Timer 0 interrupt	
WDT interrupt	
External interrupt 1	
Timer 1 interrupt	
Serial channel 0 interrupt	
Timer 2 interrupt	

11. Power Management Unit

Power management unit serves two power management modes, IDLE and STOP, for the users to do power saving function.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	-	-	-	-	-	STOP	IDLE	40h

STOP: Stop mode control bit. Setting this bit turning on the Stop Mode.
Stop bit is always read as 0
IDLE: Idle mode control bit. Setting this bit turning on the Idle Mode.
Idle bit is always read as 0

11.1. Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

11.2. Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state from a no-clocked interrupt (external INT0/1) or WDT Interrupt or a reset (WDT, LVR) condition. Internally generated interrupts (timer, serial port ...) have no effect on stop mode since they require clocking activity.

12. Low Voltage Control

Mnemonic: LVC **Address: E6h**

7	6	5	4	3	2	1	0	Reset
-	-	LVREN	-	-	-	-	-	00H

LVREN: External low voltage reset function enable bit.
LVREN = 0 : disable external low voltage reset function.
LVREN = 1 : enable external low voltage reset function.

LVR-level：

Symbol	Parameter	Min	Typ	Max	Units
V_{LVR}	Low Voltage Reset Voltage Level	1.9	2.1	2.3	V

13. In-System Programming (Internal ISP)

The SM59R02G1 can generate flash control signal by internal hardware circuit. Users utilize flash control register, flash address register and flash data register to perform the ISP function without removing the SM59R02G1 from the system. The SM59R02G1 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which SM59R02G1 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

13.1. ISP service program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM59R02G1 for the ISP purpose.

The ISP service programs were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM59R02G1 and host device which output data to the SM59R02G1. For example, if user utilize UART interface to receive/transmit data between SM59R02G1 and host device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under SM59R02G1 active or idle mode. It can not be initiated under power down mode.

13.2. Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range $1C00 to $1FFF. It can be divided as blocks of N*256 byte. (N=0 to 4). When N=0 means no ISP function, all of 8K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 256 byte while the rest of 7.75K byte flash memory can be used as program memory. The maximum ISP service program allowed is 1K byte when N=4. Under such configuration, the usable program memory space is 7K byte.

After N determined, SM59R02G1 will reserve the ISP service program space downward from the top of the program address $1FFF. The start address of the ISP service program located at $1x00 while x is depending on the lock bit N. As shown in Table 13-1.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not has been protected, the content of ISP service program still can be read. If the flash has been protected, the overall content of flash program memory space including ISP service program space can not be read.

Table 13.1 ISP code area.

N	ISP service program address
0	No ISP service program
1	256 bytes ($1F00h ~ $1FFFh)
2	512 bytes ($1E00h ~ $1FFFh)
3	768 bytes ($1D00h ~ $1FFFh)
4	1.0 K bytes ($1C00h ~ $1FFFh)

ISP service program configurable in N*256 byte (N= 0 ~ 4)

13.3. Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash

memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user needs to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when SM59R02G1 was in system.

13.4. Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are four ways to do so:

(1) Blank reset. Hardware reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program. The hardware reset includes Internal (power on reset) and external pad reset.
(2) Execute jump instruction can load the start address of the ISP service program to PC.
(3) Enters ISP service program by hardware setting. User can force SM59R02G1 enter ISP service program by setting P2.6, P2.7 “active low” or P4.3 “ active low” during hardware reset period. The hardware reset includes Internal (power on reset) and external pad reset. In application system design, user should take care of the setting of P2.6, P2.7 or P4.3 at reset period to prevent SM59R02G1 from entering ISP service program.
(4) Enter’s ISP service program by hardware setting, the port3.0 will be detected the two clock signals during hardware reset period. The hardware reset includes Internal (power on reset) and external pad reset. And detect 2 clock signals after hardware reset.

During hardware reset period, the hardware will detect the status of P2.6/P2.7/P4.3/P3.0. If they meet one of above conditions, chip will switch to ISP mode automatically. After ISP service program executed, user need to reset the SM59R02G1, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

There are 8 kinds of entry mechanisms for user different applications. This entry method will select on the writer or ISP.

(1) First Address Blank. i.e. $0000 = 0xFF. And triggered by Internal reset signal.
(2) First Address Blank. i.e. $0000 = 0xFF. And triggered by PAD reset signal.
(3) P2.6 = 0 & P2.7 = 0. And triggered by Internal reset signal.
(4) P2.6 = 0 & P2.7 = 0. And triggered by PAD reset signal.
(5) P4.3 = 0. And triggered by Internal reset signal.
(6) P4.3 = 0. And triggered by PAD reset signal.
(7) P3.0 input 2 clocks. And triggered by Internal reset signal.
(8) P3.0 input 2 clocks. And triggered by PAD reset signal.

13.5. ISP register – TAKEY, IFCON, ISPFAH, ISPFAL, ISPFD and ISPFC

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
ISP function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
IFCON	Interface Control register	8Fh	ITS	CDPR	-	-	ALEC[1:0]		-	ISPE	00H
ISPFAH	ISP Flash Address - High register	E1h	-	-	-	ISPFAH [4:0]					FFH
ISPFAL	ISP Flash Address - Low register	E2h	ISPFAL [7:0]								FFH
ISPFD	ISP Flash Data register	E3h	ISPFD [7:0]								FFH
ISPFC	ISP Flash Control register	E4h	EMF1	EMF2	EMF3	EMF4	-	ISPF.2	ISPF.1	ISPF.0	00H

Mnemonic: TAKEY **Address: F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

ISP enable bit (ISPE) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the ISPE bit write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

Mnemonic: IFCON **Address: 8FH**

7	6	5	4	3	2	1	0	Reset
ITS	CDPR	-	-	ALEC[1:0]		-	ISPE	00H

The bit 0 (ISPE) of IFCON is ISP enable bit. User can enable overall SM59R02G1 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0. The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally. ISP registers ISPFAH, ISPFAL, ISPFD and ISPFC are read-only by default. Software must be set ISPE bit to 1 to enable these 4 registers write attribute.

Mnemonic: ISPFAH **Address: E1H**

7	6	5	4	3	2	1	0	Reset
-	-	-	ISPFAH4	ISPFAH3	ISPFAH2	ISPFAH1	ISPFAH0	FFH

ISPFAH [4:0]: Flash address-high for ISP function

Mnemonic: ISPFAL **Address: E2H**

7	6	5	4	3	2	1	0	Reset
ISPFAL7	ISPFAL6	ISPFAL5	ISPFAL4	ISPFAL3	ISPFAL2	ISPFAL1	ISPFAL0	FFH

ISPFAL [7:0]: Flash address-Low for ISP function

The ISPFAH & ISPFAL provide the 13-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

Mnemonic: ISPFD **Address: E3H**

7	6	5	4	3	2	1	0	Reset
ISPFD7	ISPFD6	ISPFD5	ISPFD4	ISPFD3	ISPFD2	ISPFD1	ISPFD0	FFH

ISPFD [7:0]: Flash data for ISP function.

The ISPFD provide the 8-bit data register for ISP function.

Mnemonic: ISPFC **Address: E4H**

7	6	5	4	3	2	1	0	Reset
EMF1	EMF2	EMF3	EMF4	-	ISPF[2]	ISPF[1]	ISPF[0]	00H

EMF1: Entry mechanism (1) flag, clear by reset. (Read only)
EMF2: Entry mechanism (2) flag, clear by reset. (Read only)
EMF3: Entry mechanism (3) flag, clear by reset. (Read only)
EMF4: Entry mechanism (4) flag, clear by reset. (Read only)
ISPF [2:0]: ISP function select bit.

ISPF[2:0]	ISP function
000	Byte program
001	Chip protect
010	Page erase
011	Chip erase
100	Write option
101	Read option
110	Erase option
111	Finish Flag

One page of flash memory is 256 byte

The Option function can access the Internal reset time select(description in section 1.4.1)、clock source select(description in section 1.5)、P4[4:7] pins function select(description in section 5)、WDTEN control bit(description in section 9)、or ISP entry mechanisms select(description in section 13).
When chip protected or no ISP service, option can only read.

The choice ISP function will start to execute once the software write data to ISPFC register.

To perform byte program/page erases ISP function, user need to specify flash address at first. When performing page erase function, SM59R02G1 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $XYMN

page erase function will erase from $XY00 to $XYFF

To perform the chip erase ISP function, SM59R02G1 will erase all the flash program memory except the ISP service program space. To perform chip protect ISP function, the SM59R02G1 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah         ; enable ISPE write attribute
MOV IFCON, #01H         ; enable SM59R02G1 ISP function
MOV ISPFAH, #10H        ; set flash address-high, 10H
MOV ISPFAL, #05H        ; set flash address-low, 05H
MOV ISPFD, #22H         ; set flash data to be programmed, data = 22H
MOV ISPFC, #00H         ; start to program #22H to the flash address $1005H
```

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VDD	Supply voltage	2.7		5.5	V	

DC Characteristics

T_A = -40℃ to 85℃, V_{CC} = 5.0V

Symbol	Parameter	Valid	Min	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3,4,5	-0.5	0.8	V	Vcc=5V
VIL2	Input Low-voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High-voltage	Port 0,1,2,3,4,5	2.0	V_{CC} + 0.5	V	
VIH2	Input High-voltage	RES, XTAL1	70%Vcc	V_{CC} + 0.5	V	
VOL	Output Low-voltage	Port 0,1,2,3,4,5		0.4	V	IOL=4.9mA Vcc=5V
VOH1	Output High-voltage using Strong Pull-up(1)	Port 0,1,2,3,4,5	90% V_{CC}		V	IOH= -4.6mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0,1,2,3,4,5	2.4		V	IOH= -250uA
			75% V_{CC}		V	IOH= -162uA
			90% V_{CC}		V	IOH= -73uA
IIL	Logic 0 Input Current	Port 0,1,2,3,4,5		-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,2,3,4,5		-650	uA	Vin= 2.0V
ILI	Input Leakage Current	Port 0,1,2,3,4,5		±10	uA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50	300	kΩ	
CIO	Pin Capacitance			10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD		12	mA	Active mode, 12MHz V_{CC} =5V 25 ℃
				11	mA	Idle mode, 12MHz V_{CC} =5V 25 ℃
				5	uA	Power down mode V_{CC} =5V 25 ℃

Notes： 1. Port in Push-Pull Output Mode
2. Port in Quasi-Bidirectional Mode

T_A = -40℃ to 85℃, V_{CC} = 3.0V

Symbol	Parameter	Valid	Min	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3,4,5	-0.5	0.8	V	Vcc=3.0V
VIL2	Input Low-voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High-voltage	Port 0,1,2,3,4,5	2.0	V_{CC} + 0.5	V	
VIH2	Input High-voltage	RES, XTAL1	70%Vcc	V_{CC} + 0.5	V	
VOL	Output Low-voltage	Port 0,1,2,3,4,5		0.4	V	IOL=3.2mA Vcc=3.0V
VOH1	Output High-voltage using Strong Pull-up(1)	Port 0,1,2,3,4,5	90% V_{CC}		V	IOH= -2.3mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0,1,2,3,4,5	2.4		V	IOH= -77uA
			90% V_{CC}		V	IOH= -33uA
IIL	Logic 0 Input Current	Port 0,1,2,3,4,5		-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,2,3,4,5		-650	uA	Vin=1.5V
ILI	Input Leakage Current	Port 0,1,2,3,4,5		±10	uA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50	300	kΩ	
CIO	Pin Capacitance			10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD		11	mA	Active mode ,12MHz V_{CC} = 3.0 V 25 ℃
				10	mA	Idle mode, 12MHz V_{CC} =3.0V 25 ℃
				4	uA	Power down mode V_{CC} =3.0V 25 ℃

Notes： 1. Port in Push-Pull Output Mode

2. Port in Quasi-Bidirectional Mode