Preliminary Data Sheet

BCM5222

Dual Port 10/100BASE-TX IEEE 802.3u Fast Ethernet Transceiver

GENERAL DESCRIPTION

The BCM5222 is a dual-port, low-power, 10/100BASE-TX transceiver targeting a number of applications requiring intelligent power management and robust network tolerance. The BCM5222 operates using a 1.8V and 3.3V supply. The devices contain two full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, which perform all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4, and 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable.

The BCM5222 is a highly integrated solution combining a digital adaptive equalizer, ADC, phase lock loop, line driver, encoder, decoder and all the required support circuitry into a single monolithic CMOS chip. It complies fully with the IEEE 802.3u specification, including the Media Independent Interface (MII) and Auto-Negotiation subsections.

The effective use of digital technology in the BCM5222 design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field proven digital adaptive equalization and digital clock recovery techniques.

FEATURES

- Dual Port 10/100BASE-TX IEEE 802.3u Fast Ethernet Transceiver
- Power Consumption: <180 mW/port
- Unique Energy Detection Circuit to Enable Intelligent Power Management
- HP Auto-MDIX
- Cable Length Indication
- Cable Noise Level Indication
- Cable length greater than 140 meters
- Well Under 10 PPM defect ratio quality
- Industrial Temperature Range (-40 to 85C)
- MII/7-wire serial interface
- IEEE 1149.1 (JTAG) Scan Chain Support
- MII Management Via Serial Port
- 100-pin PQFP and 100-pin fpBGA packages

APPLICATIONS

- IP Phones
- Backplane Bus Communication
- Embedded Telecom
- Print Servers

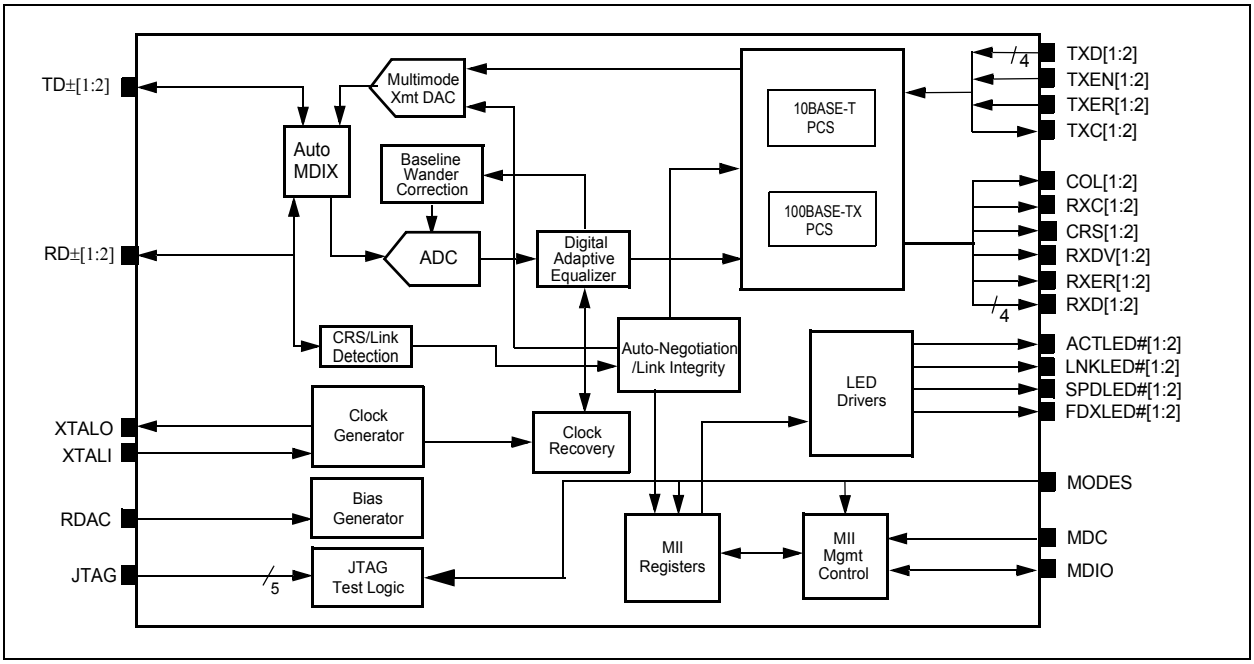

Figure 1: Functional Block Diagram

16215 Alton Parkway • P.O. Box 57013 • Irvine, CA 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

REVISION HISTORY

Revision	*Date*	*Change Description*
5222-DS02-R	7/20/04	Revised pin assignments, signal definitions, added new characterizations.
5222-DS01-R	10/12/01	Updated clock information.
5222-DS00-R	3/1/01	Initial Release

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, CA 92619-7013

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Section 1: Functional Description

OVERVIEW

The BCM5222 is a dual-port, single-chip Fast Ethernet transceiver. It performs all of the physical layer interface functions for 100BASE-TX full-or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full-or half-duplex Ethernet on CAT 3, 4, or 5 cable.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, auto-negotiation and Media Independent Interface (MII) management functions. Each of the two PHYs in the BCM5222 can be connected to a MAC switch controller through the MII on one side, and can connect directly to the network media on the other side (through isolation transformers for unshielded twisted pair (UTP)). The BCM5222 is fully compliant with the IEEE 802.3 and 802.3u standards.

ENCODER/DECODER

In 100BASE-TX mode, the BCM5222 transmits and receives a continuous data stream on twisted-pair cable. When the MII transmit enable is asserted, nibble-wide (4-bit) data from the transmit data pins is encoded into 5-bit code groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1 on page 4. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. When the MII transmit error input is asserted during a packet, the transmit error code group (H) is sent in place of the corresponding data code group. The transmitter repeatedly sends the idle code group between packets.

In 100BASE-TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multi-mode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization, and clock recovery in 100BASE-TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM5222 asserts the MII RXER signal. The chip also asserts RXER for several other error conditions that improperly terminate the data stream. While RXER is asserted, the receive data pins are driven with a 4-bit code indicating the type of error detected. The error codes are listed in Table 2 on page 5.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the link fail state, where only idle codes are transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the link pass state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD± pins for the presence of valid link pulses.

CARRIER SENSE

In 100BASE-TX mode, carrier sense is asserted asynchronously on the CRS pin as soon as activity is detected in the receive data stream. RXDV is asserted as soon as a valid Start-of-Stream Delimiter (SSD) is detected. Carrier sense and RXDV are deasserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. If carrier sense is asserted and a valid SSD is not detected immediately, then RXER is asserted in place of RXDV. A value of 1110 is driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD± input pins.

In half-duplex DTE mode, the BCM5222 asserts carrier sense while transmit enable is asserted and the link monitor is in the Pass state. In full-duplex mode, CRS is only asserted for receive activity.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted and transmission is in progress.

AUTO-NEGOTIATION

The BCM5222 contains the ability to negotiate its mode of operation over the twisted pair link using the auto-negotiation mechanism defined in the IEEE 802.3u specification. Auto-negotiation can be enabled or disabled by hardware or software control. When the auto-negotiation function is enabled, the BCM5222 automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5222 has Next Page capabilities. The Next Page and auto-negotiation must be enabled. Once auto-negotiation begins the pages are to be sent by writing to Register 7 for each page.

The BCM5222 can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full-and/or half-duplex. The transceiver negotiates with its link partner and chooses the highest level of operation available for its own link.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes Intersymbol Interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5222 achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5222 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self-adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode, the adaptive equalizer is bypassed in these two modes of operation.

ADC

The receive channel has a 6-bit, 125-MHz analog-to-digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The ADC output is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low-offset, high-power-supply noise rejection, fast-settling time, and low-bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clock is locked to the 25-MHz clock input, while the receive clock is locked to the incoming data stream. Clock recovery circuits optimized to MLT3 and Manchester encoding schemes are included for use with the different operating modes. The input data stream is sampled by the recovered clock, and fed synchronously to the digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5222 automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error.

The baseline wander correction circuit is not required, and therefore is bypassed, in 10BASE-T operating mode.

MULTIMODE TRANSMIT DAC

The multimode transmit digital-to-analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It allows programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components, thereby reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output, which is well balanced, and produces very low noise transmit signals.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted-pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit-wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724µs, it becomes unlocked, and the receive decoder is disabled. The descrambler is always forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T mode.

MII MANAGEMENT

The BCM5222 contains two complete sets of MII management registers accessible by using the management clock line (MDC) and the bidirectional serial data line (MDIO). Each PHY has one associated MII register which is accessed by commands containing the corresponding PHY address. By configuring the five external PHY address input pins, the PHY address of PHY 1 is set. PHY 2 address will be one bit higher than that of PHY 1.

Every time an MII read or write operation is executed, the BCM5222 compares the operation's PHY address with its own PHY address definition. The operation is executed only when the addresses match.

For further details, see Section 5: “Register Summary” on page 16.

Table 1: 4B5B Encoding

Name	*4B Code*	*5B Code*	*Meaning*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B

Table 1: 4B5B Encoding (Cont.)

Name	*4B Code*	*5B Code*	*Meaning*
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start-of-Stream Delimiter, Part 1
K	0101*	10001	Start-of-Stream Delimiter, Part 2
T	0000*	01101	End-of-Stream Delimiter, Part 1
R	0000*	00111	End-of-Stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signalling errors)
V	0111	00000	Invalid Code
V	0111	00001	Invalid Code
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	011000	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code
* Treated as invalid code (mapped to 0111) when received in data field.			

Table 2: Receive Error Encoding

Error Type	*RXD[3:0]*
Stream cipher error—descrambler lost lock	0010
Link failure	0011
Premature end of stream	0110
Invalid code	0111
Transmit error	1000
False carrier sense	1110

Section 2: Hardware Signal Definitions

Table 3 provides the pin descriptions for the BCM5222 BGA and MQFP packages.

Table 3: Pin Descriptions

BGA	*MQFP*	*Pin Label*	*Type*	*Description*
MEDIA CONNECTIONS				
K5, K6 K4, K7	38, 44 37, 45	RD+{2}, RD+{1} RD–{2}, RD-{1}	I/O	**Receive Pair**. Differential data from the media is received on the RD± signal pair. This pair will function as TX± in the MDIX configuration.
K2, K9 K3, K8	35, 47 36, 46	TD+{2}, TD+{1} TD–{2}, TD-{1}	I/O	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair. This pair will function as RX± in the MDIX configuration.
CLOCK				
H3, H4	33 32	XTALI XTALO	I/O	**Crystal Input, Output.** A continuous 25 MHz reference clock must be supplied to the BCM5222 by connecting a 25 MHz crystal between these two pins or by driving XTALI with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to ground. When using an oscillator, leave XTALO unconnected.
MII INTERFACE				
A2, C7	97, 84	TXC{2}, TXC{1}	O_{3S}	**Transmit Clock.** 25-MHz output in 100BASE-TX mode and 2.5 MHz in 10BASE-T MII mode. 10-MHz output in 10BASE-T serial mode. This clock is a continuously driven output, generated from the XTALI input.
D5, A8 A3, B7 D6, A7 A4, C6	96, 85 95, 86 94, 87 93, 88	TXD3{2}, TXD3{1} TXD2{2}, TXD2{1} TXD1{2}, TXD1{1} TXD0{2}, TXD0{1}	I_{PD}	**MII Transmit Data Input.** Nibble-wide transmit data stream is input on these pins synchronous with TXC. TXD3 is the most significant bit. Only TXD0 is used in 10BASE-T serial mode.
C5, A9	98, 83	TXEN{2}, TXEN{1}	I_{PD}	**MII Transmit Enable.** Active high. Indicates that the data nibble on TXD[3:0] is valid.
G8, E10	62, 65	TDI/TXER{2}, TMS/TXER{1}	I_{PD}	**MII Transmit Error.** An active high input is asserted when a transmit error condition is requested by the MAC.
C2, D9	8, 73	RXC{2}, RXC{1}	O_{3S}	**MII Receive Clock.** 25-MHz output in 100BASE-TX MII mode and 2.5-MHz output in 10BASE-T MII mode. 10-MHz output in 10BASE-T serial mode. This clock is recovered from the incoming data on the cable inputs. RXC is a continuously running output clock resynchronized at the start of each incoming packet. This synchronization may result in an elongated period during one cycle while RXDV is low.
A1, D7 B2, A10 C3, C9 B1, D8	2, 79 3, 78 4, 77 5, 76	RXD3{2}, RXD3{1} RXD2{2}, RXD2{1} RXD1{2}, RXD1{1} RXD0{2}, RXD0{1}	O_{3S}	**MII Receive Data Outputs.** Nibble-wide receive data stream is driven out on these pins synchronous with RXC. RXD3 is the most significant bit. Only RXD0 is used in 10BASE-T serial mode.
D4, B10	6, 75	RXDV{2}, RXDV{1}	O_{3S}	**MII Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD output pins is valid.

[MSB:LSB]; $\overline{\text{OVERLINE}}$ = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

Table 3: Pin Descriptions (Cont.)

BGA	*MQFP*	*Pin Label*	*Type*	*Description*
C1, E6	7, 74	RXER{2}, RXER{1}	O_{3S}	**MII Receive Error Detected.** Active high. Indicates that an error is occurring during a receive frame.
E5, C10	9, 72	CRS{2}, CRS{1}	O_{3S}	**MII Carrier Sense.** Active high. Indicates traffic on link. In 100BASE-TX mode, CRS is asserted when a non-idle condition is detected in the receive data stream and deasserted when idle or a valid end of stream delimiter is detected. In 10BASE-T mode, CRS is asserted when a valid preamble is detected and deasserted when end-of-file or an idle condition is detected. CRS is also asserted during transmission of packets except in full-duplex modes. CRS is an asynchronous output signal.
D3, E7	10, 71	COL{2}, COL{1}	O_{3S}	**Collision Detect.** In half-duplex modes, active high output indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous output signal.
A5	91	MDIO	I/O_{PU}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers of each of the PHYs. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
B5	92	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 25 MHz are supported.
MODE				
D10	68	RESET	I_{PU}	**Reset.** Active Low. Resets the BCM5222. Also used to enable Power Off and Low Power modes.
E1, E4	13, 14	PHYAD0, PHYAD1,	I_{PU}	**PHY Address Selects PHYAD[1:0].** These inputs set the two least significant bits of the MII management PHY address for PHY 1. PHY 2 address will be one greater than the PHY 1 address.These pins are sampled only during power-on reset.
E3, E2, F1	15, 16, 17	PHYAD2, PHYAD3, PHYAD4	I_{PD}	**PHY Address Selects PHYAD[4:2].** These inputs set the three most significant bits of the MII management PHY address for PHY 1. PHY 2 address will be one greater than the PHY 1 address.These pins are sampled only during power-on reset.
H8 F9	51, 64	PAUSE{2}, TDO/PAUSE{1}	O_{PD}	**PAUSE.** Status of the link partner's PAUSE bit, bit 10d of MII Link Partner Ability register 05d.
F6	63	TCK/FDX	I_{PU}	**Full-Duplex Mode.** When auto-negotiation is disabled, the FDX pin is logically ORed with register 00, bit 8 to select full-duplex (1) or half-duplex (0) operation. (This pin becomes TCK if TRST pin is high.) When auto-negotiation is enabled, this pin is ignored.
H2	27	LOW_PWR	I_{PD}	**Low Power Mode Enable.** Active high input places the BCM5222 into Low Power operation with the chip deactivated except for the crystal oscillator if bit 2 of Shadow register 1Ah is set to the non-default value of 1. When asserted with RESET pulled low, the entire chip is deactivated (Power Off mode).

[MSB:LSB]; $\overline{\text{OVERLINE}}$ = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

Table 3: Pin Descriptions (Cont.)

BGA	*MQFP*	*Pin Label*	*Type*	*Description*
J1	25	F100	I_{PU}	**Force 100BASE-TX Control.** When F100 is high and ANEN is low, the transceiver is forced to 100BASE-TX operation. When F100 is low and ANEN is low, the transceiver is forced to 10BASE-T operation. When ANEN is high, F100 has no effect on operation.
G2	24	ANEN	I_{PU}	**Auto-Negotiation Enable.** ANEN is active high. When pulled high, auto-negotiation begins immediately after reset. When low, auto-negotiation is disabled by default.
F7	67	TESTEN	I_{PD}	**Test Mode Enable.** Active high. Can float or be grounded for normal operation.
J7, H9	53, 54	ADV_PAUSE{2}, ADV_PAUSE{1}	I_{PU}	**ADV_PAUSE.** Active low. During power-on reset, this pin is sampled and causes the default value of MII auto-negotiation Advertisement register, 4, bit 10d to be set accordingly.
J10	52	MDIX_DIS	I_{PD}	**HP Auto-MDIX Disable.** Active high. During power-on reset if this pin is high the BCM5222 disables MDI cable cross-over detection on both ports.
A6	89	INTR	O_{3S}	Interrupt. When the interrupt mode is enabled, pin becomes INTR. This pin is shared by both PHY 1 and PHY 2.
K10	50	DLLTEST	I_{PU}	DLL Test. This pin must be left unconnected during normal operation.
BIAS				
G4	29	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of the transmit DAC. A resistor of 1.31 kΩ ±1% must be connected between the RDAC pin and GND.
LEDS				
F5, G9	18, 60	$\overline{\text{LNKLED}}${2}, $\overline{\text{LNKLED}}${1}	O_{3S}	**Link Integrity LED.** The Link Integrity LED indicates the link status of the PHY. $\overline{\text{LNKLED}}$ is driven low when the link to the PHY is good.
F2, G7	20, 58	$\overline{\text{SPDLED}}${2}, $\overline{\text{SPDLED}}${1}	O_{3S}	**100BASE-TX LED.** The 100 Base-TX LED is driven low when operating in 100BASE-TX modes and high when operating in 10BASE-T modes.
F3, G6	21, 57	$\overline{\text{FDXLED}}${2}, $\overline{\text{FDXLED}}${1}	O_{3S}	**Full-Duplex LED.** Driven low when the link is full-duplex and driven high in half-duplex.
F4, G10	19, 59	$\overline{\text{ACTLED}}${2}, $\overline{\text{ACTLED}}${1}	O_{3S}	**Activity LED.** Active low output. The receive activity LED is driven low for approximately 80 ms each time there is receive or transmit activity, while in the link pass state.
JTAG				
F8	66	TRST	I_{PD}	**Test Reset.** Must be set low for normal operation, holding the JTAG circuitry in reset. Transition from low to high initializes the JTAG Tap Controller to the test-logic-reset state. Hold high during JTAG.
F6	63	TCK/FDX	I_{PU}	**Test Clock.** This pin becomes TCK if $\overline{\text{TRST}}$ pin is high. Clock input used to synchronize JTAG TAP control and data transfers.
G8	62	TDI/TXER{2}	I_{PD}	**Test Data Input.** This pin becomes TDI if $\overline{\text{TRST}}$ is high. Data or instruction input for JTAG test logic. Sampled on the rising edge of TCK.

[MSB:LSB]; $\overline{\text{OVERLINE}}$ = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

Table 3: Pin Descriptions (Cont.)

BGA	*MQFP*	*Pin Label*	*Type*	*Description*
E10	65	TMS/TXER{1}	I_{PD}	**Test Mode Select.** This pin becomes TMS if $\overline{TRST}$ is high. Single control input to the JTAG TAP controller is used to traverse the test-logic state machine. Sampled on the rising edge of TCK.
F9	64	TDO/PAUSE{1}	O_{3S}	**Test Data Output.** This pin becomes TDO if $\overline{TRST}$ is high. Serial data output from the JTAG TAP controller. Updated on the falling edge of TCK.
POWER				
B8, C4	99, 82	DVDD	PWR	**Digital VDD (1.8V).** Connect these pins to decoupling capacitors as shown in Figure 17 on page 60.
J5	41	AVDD	PWR	**Analog VDD (1.8V).** Connect this pin to decoupling capacitors as shown in Figure 17 on page 60.
B3, C8, D1, E8, G1, H10	1, 11, 22, 56, 70, 80	OVDD	PWR	3.3V Digital Periphery (Output Buffer) VDD supply.
B6, B4, B9	100, 90, 81	DGND	GND	Digital Ground.
G5, J6, H5, H6	39, 40, 42, 43	AGND	GND	Analog Ground.
J2	28	BIASVDD	PWR	**BIAS VDD (3.3V).** Connect this pin to decoupling capacitors as shown in Figure 17 on page 60.
J3	30	BIASGND	GND	Bias Ground. Connect this pin to AGND.
H7, H1, D2, E9	12, 23, 55, 69	OGND	GND	**Output Buffer Ground.** Digital Periphery (Output Buffer) ground.
J4	34	PLLAGND	GND	**PLL Analog Ground.** Phase Locked Loop ground.
K1	31	PLLAVDD	PWR	**PLL Analog VDD (1.8V).** 1.8V, Phase Locked Loop VDD Core. Connect this pin to decoupling capacitors as shown in Figure 17 on page 60.
NO CONNECTS				
J8, J9 G3, F10	26, 48, 49, 61	NC	NC	**No Connection.** Leave these pins floating.

[MSB:LSB]; $\overline{OVERLINE}$ = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

Section 3: Pinout Diagram

Figure 2 provides the pinout diagram for the BCM5222KQM package, and Figure 3 on page 11 provides the pinout diagram for the BCM5222KPF package.

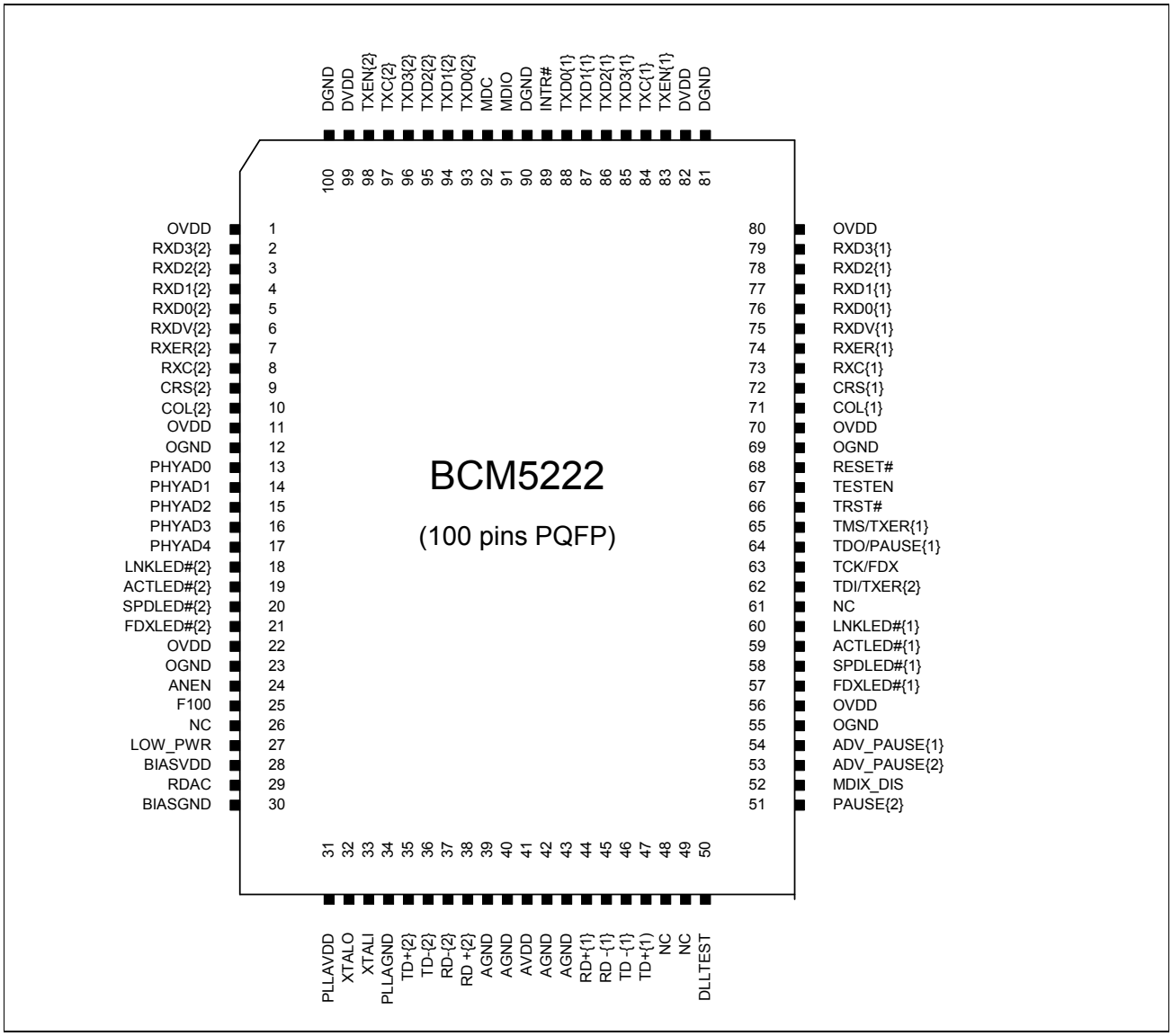
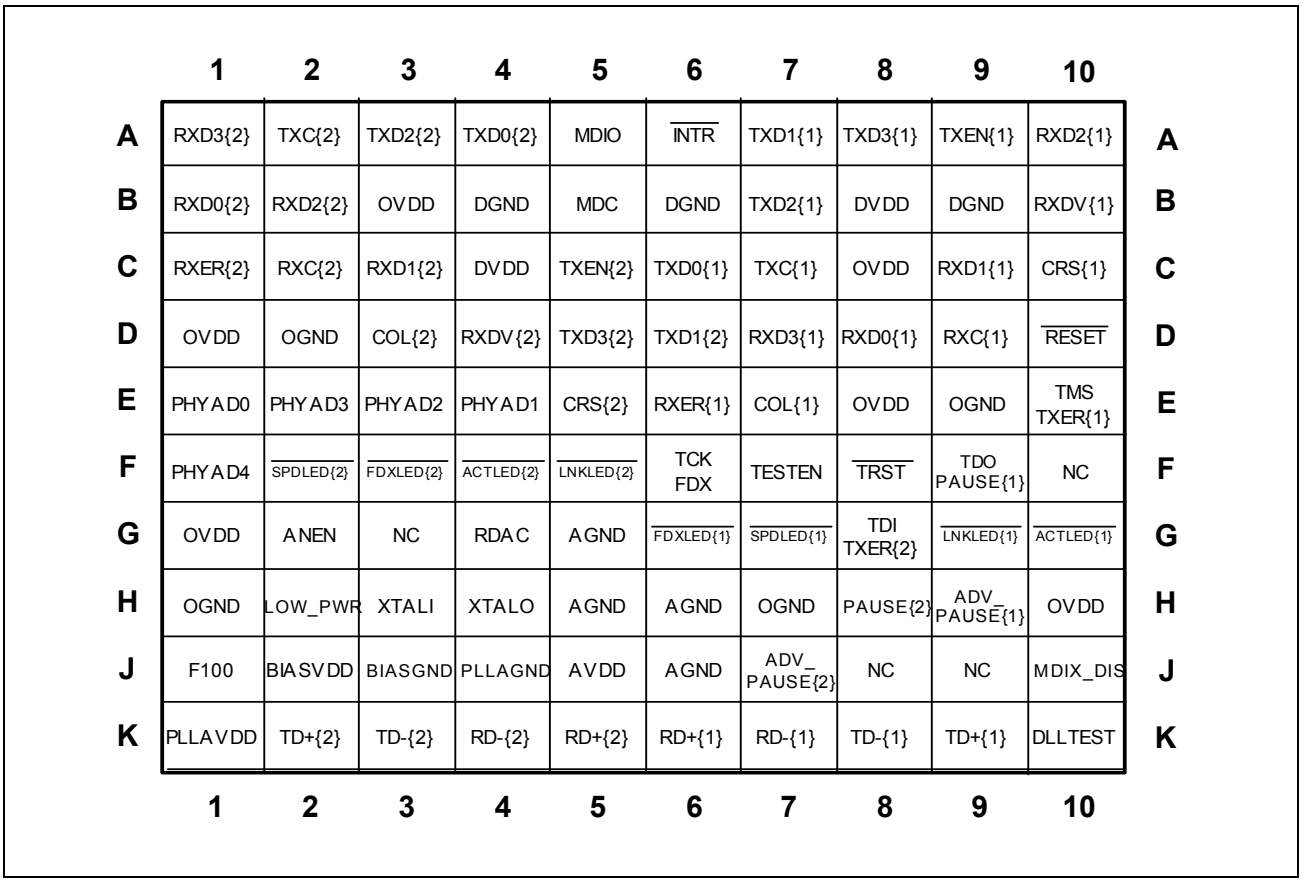


Figure 2: BCM5222KQM Pinout Diagram



	1	2	3	4	5	6	7	8	9	10	
A	RXD3{2}	TXC{2}	TXD2{2}	TXD0{2}	MDIO	$\overline{\text{INTR}}$	TXD1{1}	TXD3{1}	TXEN{1}	RXD2{1}	A
B	RXD0{2}	RXD2{2}	OVDD	DGND	MDC	DGND	TXD2{1}	DVDD	DGND	RXDV{1}	B
C	RXER{2}	RXC{2}	RXD1{2}	DVDD	TXEN{2}	TXD0{1}	TXC{1}	OVDD	RXD1{1}	CRS{1}	C
D	OVDD	OGND	COL{2}	RXDV{2}	TXD3{2}	TXD1{2}	RXD3{1}	RXD0{1}	RXC{1}	$\overline{\text{RESET}}$	D
E	PHYAD0	PHYAD3	PHYAD2	PHYAD1	CRS{2}	RXER{1}	COL{1}	OVDD	OGND	TMS TXER{1}	E
F	PHYAD4	$\overline{\text{SPDLED{2}}}$	$\overline{\text{FDXLED{2}}}$	$\overline{\text{ACTLED{2}}}$	$\overline{\text{LNKLED{2}}}$	TCK FDX	TESTEN	$\overline{\text{TRST}}$	TDO PAUSE{1}	NC	F
G	OVDD	ANEN	NC	RDAC	AGND	$\overline{\text{FDXLED{1}}}$	$\overline{\text{SPDLED{1}}}$	TDI TXER{2}	$\overline{\text{LNKLED{1}}}$	$\overline{\text{ACTLED{1}}}$	G
H	OGND	LOW_PWR	XTALI	XTALO	AGND	AGND	OGND	PAUSE{2}	ADV_ PAUSE{1}	OVDD	H
J	F100	BIASVDD	BIASGND	PLLAGND	AVDD	AGND	ADV_ PAUSE{2}	NC	NC	MDIX_DIS	J
K	PLLAVDD	TD+{2}	TD-{2}	RD-{2}	RD+{2}	RD+{1}	RD-{1}	TD-{1}	TD+{1}	DLLTEST	K
	1	2	3	4	5	6	7	8	9	10	

Figure 3: BCM5222KPF Pinout Diagram

Section 4: Operational Description

RESET

There are two ways to reset the BCM5222. A hardware reset pin is provided that resets all internal nodes in the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to the BCM5222 after power-up.

The BCM5222 also has a software reset capability. To perform software reset, a 1 must be written to bit 15 of the MII Control register. This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a 0 is written to the MII Control register reset bit.

CLOCK

The BCM5222 requires a 25 MHz clock reference which can be driven by attaching a 25-MHz crystal between the XTALI and XTALO pins or by connecting an external oscillator to pin XTALI. Connect 22 pF capacitors from each pin to ground when using a crystal. When using an oscillator, leave XTALO unconnected. The reference clock requires accuracy of at least ± 50 ppm.

ISOLATE MODE

When the BCM5222 is put into isolate mode, all MII inputs (TXD[3:0], TXEN, and TXER) are ignored, and all MII outputs (TXC, COL, CRS, RXC, RXDV, RXER, and RXD[3:0]) are set to high impedance. Only the MII management pins (MDC, MDIO) operate normally. Upon resetting the chip, the isolate mode is off. Writing a 1 to bit 10 of the MII Control register puts the transceiver into isolate mode. Writing a 0 to the same bit removes it from isolate mode.

LOOPBACK MODE

Loopback mode allows in-circuit testing of the BCM5222 chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. The loopback mode is enabled by writing a 1 to bit 14 of the MII Control register. To resume normal operation, bit 14 of the MII Control register must be 0.

Incoming packets on the cable are ignored in loopback mode. Because of this, the COL pin is normally not activated during loopback mode. To test that the COL pin is actually working, the BCM5222 can be placed into collision test mode. This mode is enabled by writing a 1 to bit 7 of the MII Control register. Asserting TXEN causes the COL output to go high, and deasserting TXEN causes the COL output to go low.

While in loopback mode, several function bypass modes are also available that can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include bypass scrambler, bypass MLT3 encoder and bypass 4B5B encoder. All bypass modes can be accessed by writing bits of the Auxiliary Control register (10h).

Due to the nature of the Block RXDV mode (bit 9 of MII register 1Bh), which is enabled by default, 10BASE-T loopback does not function properly. It is necessary to first disable the Block RXDV mode by writing FD00h to the Aux Mode 2 register (1Bh).

FULL-DUPLEX MODE

The BCM5222 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. The COL signal is never activated when in full-duplex mode. The CRS output is asserted only during receive packets, not transmit packets.

By default, the BCM5222 powers up in half-duplex mode. When auto-negotiation is disabled, full-duplex operation can be enabled either by FDX pin control or by an MII register bit (register 0h, bit 8).

When auto-negotiation is enabled in DTE mode, full-duplex capability is advertised by default, but can be overridden by a write to the Auto-Negotiation Advertisement register (04h).

AUTO-MDIX

The BCM5222 offers Auto-MDIX functioning on both PHYs. This enables the device to automatically adapt the configuration of the device transmit and receive pins in order to successfully link and transmit with a link partner. During auto-negotiation and 10/100BASE-TX operation, the BCM5222 normally transmits on TD± pins and receives on RD± pins. The BCM5222 automatically switches its transmitter to the RD± pins and its receiver to the TD± pins, if required, in order to communicate with the remote device. If two devices are connected that both have Auto-MDI/MDIX crossover capability, then a random algorithm determines which end performs the crossover function.

The Auto-MDI/MDIX crossover feature is a function of auto-negotiation. If the BCM5222 is configured not to perform auto-negotiation, the feature does not work, and a specific cable, either crossed or straight, is required to ensure the transmit function at one end of the cable is connected with the receive function at the other end of the cable. This feature is enabled by default, but can be disabled by setting the MDIX_DIS pin high during power-on reset. This will disable the function on both PHYs. By setting bit 11 in register 1Ch to a 1, the Auto-MDIX can be disabled for an individual PHY. During operation, the MDI state can be determined by reading bit 13 of register 1Ch, as indicated in the BCM5222 data sheet. Additionally, a manual MDI swap can be forced by setting or clearing bit 12 of register 1Ch.

10BASE-T MODE

The same magnetics module used in 100BASE-TX mode can be used to interface to the twisted-pair cable when operating in 10BASE-T mode. The data is two-level Manchester encoded instead of three-level MLT3, and no scrambling/descrambling or 4B5B coding is performed. Data and clock rates are decreased by a factor of 10, with the MII interface signals operating at 2.5 MHz.

10BASE-T SERIAL MODE

The BCM5222 supports 10BASE-T serial mode, also known as the 7-wire interface. In this mode, 10BASE-T transmit and receive packets appear at the MII in serial fashion, at a rate of 10 MHz. Receive packet data is output on RXD0 synchronously with RXC. Transmit packet data must be input on TXD0 synchronously with TXC. Both clocks toggle at 10 MHz.

The 10BASE-T serial mode is enabled by writing a 1 to bit 1 of the Auxiliary Multiple-PHY register (1Eh). This mode is not available in 100BASE-TX mode. Table 4 on page 14 shows the MII pins used in this mode and their direction of operation.

Table 4: 10BASE-T Serial Mode (7-Wire) Signals

pin LABEL	*Type*	*DESCRIPTION*
TXD0	I	Serial Transmit Data
TXC	O	Transmit Data Clock (10 MHz)
TXEN	I	Transmit Enable
RXD0	O	Serial Receive Data
RXC	O	Receive Data Clock (10 MHz)
CRS	O	Carrier Sense
COL/RXEN	O	Collision Detect

SPECIAL LED MODES

FORCE LEDS ON

The $\overline{\text{SPDLED}}$, $\overline{\text{LNKLED}}$, $\overline{\text{ACTLED}}$, and $\overline{\text{FDXLED}}$ outputs can be forced on (0 value) by writing a 01 to bit 5 and 4 of Shadow register 1Ah.

DISABLE LEDS

The $\overline{\text{SPDLED}}$, $\overline{\text{LNKLED}}$, $\overline{\text{ACTLED}}$, and $\overline{\text{FDXLED}}$ outputs can be forced off (1 value) by writing a 10 to bit 5 and 4 of Shadow register 1Ah.

INTERRUPT MODE

The BCM5222 can be programmed to provide an interrupt output that is shared between the two PHYs. Three conditions can cause an interrupt to be generated: changes in the duplex mode, changes in the speed of operation or changes in the link status. The interrupt feature is disabled by default and is enabled by setting MII register 1Ah, bit 14. The $\overline{\text{INTR}}$ pin is open-drain and can be wire-ORed with $\overline{\text{INTR}}$ pins of other chips on a board. The status of each interrupt source is reflected in register 1Ah, bits 1, 2 and 3. If any type of interrupt occurs, the Interrupt Status bit, register 1Ah, bit 0, is set.

The Interrupt register (1Ah) also contains several bits to control different facets of the interrupt function. If the interrupt enable bit is set to 0, no status bits are set and no interrupts are generated. If the interrupt enable bit is set to 1, the following conditions apply:

- If mask status bits (bits 9,10,11) are set to 0 and the interrupt mask (bit 8) is set to 0, status bits and interrupts are available.
- If mask status bits (bits 9,10,11) are set to 0 and the interrupt mask (bit 8) is set to 1, status bits are set but no interrupts generated.
- If any mask status bit is set to 1 and the interrupt mask is set to 0, that status bit is not set and no hardware interrupt of that type is generated.
- If any mask status bit is set to 1 and the interrupt mask is set to 1, that status bit is not set and no interrupt of any kind is generated.

POWER SAVING MODES

Several power saving modes are implemented in the BCM5222. Table 5 shows low power modes available in the BCM5222. Low power modes can be achieved either by hardware pin or MII register programming. The table shows both hardware pin and software bits that determine the low power modes and whether the BCM5222 keeps the clocks active. The BCM5222 requires a hard reset to return to normal mode from a low power mode if the clocks are not running. Allow at least 2 ms before resuming normal operation with the BCM5222 after the device is set to run in normal mode from a low power mode.

Table 5: Low Power Modes

Hardware Settings		*Software Setting*					*Chip Operation*
LOW_PWR	*RESET*	*FORCE IDDQ*	*LOW_PWR MODE*	*ENABLE CLOCK*	*CLOCKS*	*AUTO MDIX*	*COMMENT*
1	0	X	1	X	OFF	NO	Reset State.
0	1	0	0	X	ON	Avail	Normal operation without any power saving modes active.
X	X	1	X	X	OFF	NO	Force Iddq register serves as a software induced power-down mode.
1	1	0	0	0	OFF	NO	Low Power Mode without CLK functioning, induced through hardware.
1	1	0	0	1	ON	Avail	Low Power Mode with CLK functioning, induced through hardware.
0	1	0	1	0	OFF	NO	Low Power Mode without CLK functioning, induced through software.
0	1	0	1	1	ON	Avail	Low Power Mode with CLK functioning, induced through software.

LOW_PWR: Pin 27 (Active high)
RESET: Pin 68 (Active Low)
Force Iddq: Bit 0 of Shadow register 1Ah (0–Normal Op. 1–Power down)
Low Power Mode: Bit 1 of Shadow register 1Ah(0–Normal Op. 1–Low Power Mode)
Enable Clock: Bit 2 of Shadow register 1Ah(0–Disabled in LP mode 1–Enabled)
Clock Operation: If clock is off, additional power is saved.
Auto-MDIX Operation: Only available if device has clock running.
X=1/0 or Don't Care

Section 5: Register Summary

MEDIA INDEPENDENT INTERFACE (MII) MANAGEMENT INTERFACE: REGISTER PROGRAMMING

The BCM5222 fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers are serially written to and read from using the MDIO and MDC pins. A single clock waveform must be provided to the BCM5222 at a rate of 0–25MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock.

See Table 6 for the fields in every MII instruction's read or write packet frame.

Table 6: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*Regad*	*TA*	*Data*	*idle*	*Direction*
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5222 Driven by BCM5222
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5222

PREAMBLE (PRE)

32 consecutive 1 bits must be sent through the MDIO pin to the BCM5222 to signal the beginning of an MII instruction. Fewer than 32 1 bits causes the remainder of the instruction to be ignored, unless the Preamble Suppression mode is enabled (register 01, bit 6).

START OF FRAME (ST)

A 01 pattern indicates that the start of the instruction follows.

OPERATION CODE (OP)

A read instruction is indicated by 10, while a write instruction is indicated by 01.

PHY ADDRESS (PHYAD)

A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple transceivers. The BCM5222 supports the full 32-PHY address space.

REGISTER ADDRESS (REGAD)

A 5-bit register address follows, with the MSB transmitted first. The register map of the BCM5222, containing register addresses and bit definitions, are provided on the following pages.

TURNAROUND (TA)

The next two bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a write operation, 10 must be sent to the chip during these two bit times. For a read operation, the MDIO pin must be placed into high-impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

DATA

The last 16 bits of the frame are the actual data bits. For a write operation, these bits are sent to the BCM5222. For a read operation, these bits are driven by the BCM5222. In either case, the MSB is transmitted first.

When writing to the BCM5222, the data field bits must be stable 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5222, the data field bits are valid after the rising edge of MDC until the next rising edge of MDC.

IDLE

A high-impedance state of the MDIO line. All drivers are disabled and the PHY's pull-up resistor pulls the line high. At least one or more clocked idle states are required between frames. Following are two examples of MII write and read instructions.

To put a chip with PHY address 00001 into loopback mode, the following MII write instruction must be issued:

```
1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000 1...
```

To determine whether a PHY is in the link pass state, the following MII read instruction must be issued:

```
1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...
```

For the MII read operation, the BCM5222 drives the MDIO line during the TA and Data fields (the last 17 bit times). A final 65th clock pulse must be sent to close the transaction and cause a write operation.

MII CONTROL REGISTER

The MII Control register bit descriptions are shown in Table 7.

Table 7: MII Control Register (Address 00000b, 0d, 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Reset	R/W (SC)	1 = PHY reset 0 = Normal operation	0
14	Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = Auto-negotiation enable 0 = Auto-negotiation disable	1
11	Power Down	RO	0 = Normal operation	0

Table 7: MII Control Register (Address 00000b, 0d, 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
10	Isolate	R/W	1 = Electrically isolate PHY from MII 0 = Normal operation	0
9	Restart Auto-Negotiation	R/W (SC)	1 = Restart Auto-negotiation process 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	0
7	Collision Test Enable	R/W	1 = Enable the collision test mode 0 = Disable the collision test mode	0
6:0	Reserved	RO	Ignore when read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

RESET

To reset the BCM5222 by software control, a 1 must be written to bit 15 of the Control register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control register bits has no effect until the reset process is completed, which requires approximately 1 μs. Writing a 0 to this bit has no effect. Since this bit is self-clearing, within a few cycles after a write operation, it returns a 0 when read.

LOOPBACK

The BCM5222 may be placed into loopback mode by writing a 1 to bit 14 of the Control register. Clear the loopback mode by writing a 0 to bit 14 of the Control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in loopback mode, otherwise it returns a 0.

FORCED SPEED SELECTION

If auto-negotiation is enabled (both auto-negotiation pin and bit are enabled) or disabled by hardware control (auto-negotiation pin is pulled-low), this bit has no effect on the speed selection. However, if auto-negotiation is enabled by hardware, but is disabled by software control, the operating speed of the BCM5222 can be forced by writing the appropriate value to bit 13 of the Control register. In this state, the speed is not affected by the F100 hardware pin. Writing a 1 to this bit forces 100BASE-TX operation, while writing a 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 2 of the Auxiliary Control register (18h).

AUTO-NEGOTIATION ENABLE

Auto-negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic 0, auto-negotiation is disabled by hardware control. If bit 12 of the Control register is written with a value of 0, auto-negotiation is disabled by software control. When auto-negotiation is disabled in this manner, writing a 1 to the same bit of the Control register or resetting the chip re-enables auto-negotiation. Writing to this bit has no effect when auto-negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

POWER DOWN

The power modes of the BCM5222 are not accessible by this MII register bit. Use Shadow register control instead.

ISOLATE

The PHY can be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control register. All MII outputs are tri-stated and all MII inputs are ignored. Because the MII management interface is still active, the isolate mode can be cleared by writing a 0 to bit 10 of the Control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode; otherwise it returns a 0.

RESTART AUTO-NEGOTIATION

Bit 9 of the Control register is a self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the auto-negotiation state machine. For this bit to have an effect, auto-negotiation must be enabled. Writing a 1 to this bit restarts the auto-negotiation, while writing a 0 to this bit has no effect. Because the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 8 of the Auxiliary Multiple PHY register (1Eh).

Duplex Mode

This bit is logically or'd with the hardware pin, FDX, whenever Auto-negotiation is disabled.

COLLISION TEST

Test the COL pin by activating the collision test mode. While in this mode, asserting TXEN causes the COL output to go high within 512 bit times. Deasserting TXEN causes the COL output to go low within 4 bit times. Writing a 1 to bit 7 of the Control register enables the collision test mode. Writing a 0 to this bit or resetting the chip disables the collision test mode. When this bit is read, it returns a 1 when the collision test mode has been enabled; otherwise it returns a 0. This bit should only be set while in loopback test mode.

RESERVED BITS

All reserved MII register bits must be written as 0 at all times. Ignore the BCM5222 output when these bits are read.

MII STATUS REGISTER

The MII status register bit descriptions are shown in Table 8.

Table 8: MII Status Register (Address 00001B, 01d, 01h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when read Ignore when read	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	0
4	Remote Fault	RO	1 = Far-end fault condition detected 0 = No far-end fault condition detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-negotiation capable	1
2	Link Status	RO LL	1 = Link is up (link pass state) 0 = Link is down (link fail state)	0
1	Jabber Detect	RO LL	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

100BASE-T4 CAPABILITY

The BCM5222 is not capable of 100BASE-T4 operation, and returns a 0 when bit 15 of the status register is read.

100BASE-TX FULL-DUPLEX CAPABILITY

The BCM5222 is capable of 100BASE-TX full-duplex operation, and returns a 1 when bit 14 of the Status register is read.

100BASE-TX HALF-DUPLEX CAPABILITY

The BCM5222 is capable of 100BASE-TX half-duplex operation, and returns a 1 when bit 13 of the Status register is read.

10BASE-T FULL-DUPLEX CAPABILITY

The BCM5222 is capable of 10BASE-T full-duplex operation, and returns a 1 when bit 12 of the Status register is read.

10BASE-T Half-Duplex Capability

The BCM5222 is capable of 10BASE-T half-duplex operation, and returns a 1 when bit 11 of the Status register is read.

Reserved Bits

Ignore the BCM5222 output when these bits are read.

Preamble Suppression

This bit is the only writable bit in the Status register. Setting this bit to a 1 allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When preamble suppression is enabled, only 2 preamble bits are required between successive management commands, instead of the normal 32.

Auto-Negotiation Complete

Returns a 1 if auto-negotiation process has been completed and the contents of registers 4, 5, and 6 are valid.

Remote Fault

The PHY returns a 1 on bit 4 of the status register when its link partner has signalled a far-end fault condition. When a far-end fault occurs, the bit is latched at 1 and remains so until the register is read and the remote fault condition has been cleared.

Auto-Negotiation Capability

The BCM5222 is capable of performing IEEE auto-negotiation, and returns a 1 when bit 4 of the Status register is read, regardless of whether the auto-negotiation function has been disabled.

Link Status

The BCM5222 returns a 1 on bit 2 of the Status register when the link state machine is in link pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the link pass state has been entered, the link status bit is etched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 when the link pass state is entered again.

Jabber Detect

10BASE-T operation only. The BCM5222 returns a 1 on bit 1 of the Status register if a jabber condition has been detected. After the bit is read once, or if the chip is reset, it reverts to 0.

Extended Capability

The BCM5222 supports extended capability registers, and returns a 1 when bit 0 of the Status register is read. Several extended registers have been implemented in the BCM5222, and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

The physical indentifier registers bit descriptions are shown in Table 9.

Table 9: PHY Indentifier Registers (Addresses 00010 and 00011b, 02 and 03b, 02 and 03h)

Bit	*Name*	*R/W*	*Description*	*Value*
15:0	MII Address 02h	RO	PHYID HIGH	0040h
15:0	MII Address 03h	RO	PHYID LOW	632n (Hex)

Note: The revision number (n) changes with each silicon revision.

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24-bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5222 part, 32h, and Broadcom Revision number (n), is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier register occurs as follows:

- PHYID HIGH [15:0] = OUI[21:6]
- PHY LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

The 2 most significant bits of the OUI are not represented (OUI[23:22]).

Table 9 shows the result of concatenating these values to form MII Identifier Registers PHYID HIGH and PHYID LOW.

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 10: Auto-Negotiation Advertisement Register (Address 04d, 04h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Next page ability is enabled 0 = Next page ability is disabled	0
14	Reserved	RO	Ignore when read	
13	Remote Fault	R/W	1 = Transmit remote fault	0
12:11	Reserved	RO	Ignore when read	00
10	Pause	R/W	1 = Pause operation for full-duplex	0
9	Advertise 100BASE-T4	RO	0 = Do not advertise T4 capability	0
8	Advertise 100BASE-TX FDX	R/W	1 = Advertise 100BASE-TX full-duplex 0 = Do not advertise 100BASE-TX full-duplex	1
7	Advertise 100BASE-TX	R/W	1 = Advertise 100BASE-TX	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex 0 = Do not advertise 10BASE-T full-duplex	1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

Table 10: Auto-Negotiation Advertisement Register (Address 04d, 04h) (Cont.)

Bit	*Name*	*R/W*	*Description*	*Default*
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	R/W	Indicates 802.3	00001

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

NEXT PAGE

Writing a 1 to bit 15 of the Advertisement register enables the next page functioning. Writing a 0 to this bit or resetting the chip clears the next page enable bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

RESERVED BITS

Ignore output when read.

REMOTE FAULT

Writing a 1 to bit 13 of the Advertisement register causes a remote fault indicator to be sent to the link partner during auto-negotiation. Writing a 0 to this bit or resetting the chip clears the remote fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

RESERVED BITS

Ignore output when read.

PAUSE

Pause operation for full-duplex links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate pause capability to its link partner and has no effect on PHY operation.

ADVERTISEMENT BITS

Use bits 9:5 of the Advertisement register to customize the ability information transmitted to the link partner. The default value for each bit reflects the abilities of the BCM5222. By writing a 1 to any of the bits, the corresponding ability can be transmitted to the link partner. Writing a 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

SELECTOR FIELD

Bits 4:0 of the Advertisement register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 11: Auto-Negotiation Link Partner Ability Register (Address 05d, 05h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	LP Next Page	RO	Link partner next page bit	0
14	LP Acknowledge	RO	Link partner acknowledge bit	0
13	LP Remote Fault	RO	Link partner remote fault indicator	0
12:11	Reserved	RO	Ignore when read	00
10	LP Advertise Pause	RO	Link partner has pause capability	0
9	LP Advertise 100BASE-T4	RO	Link partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-TX FDX	RO	Link partner has 100BASE-TX FDX capability	0
7	LP Advertise 100BASE-TX	RO	Link partner has 100BASE-TX capability	0
6	LP Advertise 10BASE-T FDX	RO	Link partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link partner selector field	00000

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

The values contained in the Auto-Negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed, as indicated by bit 5 of the MII Status register.

LP NEXT PAGE

Bit 15 of the Link Partner Ability register returns a value of 1 when the link partner implements the next page function and has next page information that it wants to transmit.

LP ACKNOWLEDGE

Bit 14 of the Link Partner Ability register is used by auto-negotiation to indicate that a device has successfully received its link partner's link code word.

LP REMOTE FAULT

Bit 13 of the Link Partner Ability register returns a value of 1 when the link partner signals that a remote fault has occurred. The BCM5222 simply copies the value to this register and does not act upon it.

Reserved Bits

Ignore when read.

LP Advertise Pause

Indicates that the Link Partner Pause bit is set.

LP Advertise Bits

Bits 9:5 of the Link Partner Ability register reflect the abilities of the link partner. A 1 on any of these bits indicates that the link partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time auto-negotiation is restarted or the BCM5222 is reset.

LP Selector Field

Bits 4:0 of the Link Partner Ability register reflect the value of the link partner's selector field. These bits are cleared any time auto-negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 14 shows the Auto-Negotiation Expansion register bit descriptions.

Table 12: Auto-Negotiation Expansion Register (Address 00110b, 6d, 06h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	RO	Ignore when read	
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault 0 = No parallel detection fault	0
3	Link Partner Next Page Able	RO	1 = Link partner has next page capability 0 = Link partner does not have next page	0
2	Next Page Able	RO	1 = BCM5222 does have next page capability	1
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

RESERVED BITS

Ignore when read.

PARALLEL DETECTION FAULT

Bit 4 of the Auto-Negotiation Expansion register is a read-only bit that gets latched high when a parallel detection fault occurs in the auto-negotiation state machine. For further details, refer to the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

LINK PARTNER NEXT PAGE ABLE

Bit 3 of the Auto-Negotiation Expansion register returns a 1 when the link partner has next page capabilities. It has the same value as bit 15 of the Link Partner Ability register.

NEXT PAGE ABLE

The BCM5222 returns 1 when bit 2 of the Auto-Negotiation Expansion register is read, indicating that it has next page capabilities.

PAGE RECEIVED

Bit 1 of the Auto-Negotiation Expansion register is latched high when a new link code word is received from the link partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

LINK PARTNER AUTO-NEGOTIATION ABLE

Bit 0 of the Auto-Negotiation Expansion register returns a 1 when the link partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged, or if the link partner does not comply with IEEE auto-negotiation, the bit returns a value of 0.

AUTO-NEGOTIATION NEXT PAGE REGISTER

Table 13: Next Page Transmit Register (Address 07d, 07h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Additional next page(s) will follow 0 = Last page	0
14	Reserved	R/W	Ignore when read	0
13	Message Page	R/W	1= Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted link code word equalled logic zero 0 = Previous value of the transmitted link code word equalled logic one	0
10:0	Message/Unformatted Code Field	R/W		1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

NEXT PAGE

Indicates whether this is the last next page to be transmitted.

MESSAGE PAGE

Differentiates a Message Page from an Unformatted Page.

ACKNOWLEDGE 2

Indicates that a device has the ability to comply with the message.

TOGGLE

Used by the Arbitration function to ensure synchronization with the link partner during next page exchange.

MESSAGE CODE FIELD

An 11-bit-wide field, encoding 2048 possible messages.

UNFORMATTED CODE FIELD

An 11-bit-wide field, which may contain an arbitrary value.

AUTO-NEGOTIATION LINK PARTNER (LP) NEXT PAGE TRANSMIT REGISTER

Table 14: Next Page Transmit Register (Address 08d, 08h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	RO	1 = Additional next page(s) will follow 0 = Last page	0
14	Reserved	RO	Ignore when read	0
13	Message Page	RO	1= Message page 0 = Unformatted page	0
12	Acknowledge 2	RO	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted link code word equalled logic zero 0 = Previous value of the transmitted link code word equalled logic one	0
10:0	Message/Unformatted Code Field	RO		0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

NEXT PAGE

Indicates whether this is the last next page.

MESSAGE PAGE

Differentiates a Message Page from an Unformatted Page.

ACKNOWLEDGE 2

Indicates that link partner has the ability to comply with the message.

TOGGLE

Used by the Arbitration function to ensure synchronization with the link partner during next page exchange.

MESSAGE CODE FIELD

An 11-bit-wide field, encoding 2048 possible messages.

UNFORMATTED CODE FIELD

An 11-bit-wide field, which may contain an arbitrary value.

100BASE-TX AUXILIARY CONTROL REGISTER

Table 15: 100BASE-TX Auxiliary Control Register (Address 16d, 10h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:14	Reserved		Write as 0, Ignore when read	0
13	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Normal operation	0
12:11	Reserved	R/W	Write as 0, Ignore when read	00
10	Bypass 4B5B Encoder/ Decoder	R/W	1 = Transmit and receive 5B codes over MII pins 0 = Normal MII interface	0
9	Bypass Scrambler/ Descrambler	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/ Decoder	R/W	1 = NRZI encoder and decoder is disabled 0 = NRZI encoder and decoder is enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline wander correction disabled 0 = Baseline wander correction enabled	0
5:0	Reserved	R/W	Write as 0, Ignore when read	00000

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

TRANSMIT DISABLE

The transmitter can be disabled by writing a 1 to bit 13 of MII register 10h. The transmitter output (TD±) is forced into a high impedance state.

BYPASS 4B5B ENCODER/DECODER

The 4B5B encoder and decoder can be bypassed by writing a 1 to bit 10 of MII register 10h. The transmitter sends 5B codes from the TXER and TXD[3:0] pins directly to the scrambler. TXEN must be active and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RXER and RXD[3:0] pins. CRS can be asserted when a valid frame is received.

BYPASS SCRAMBLER/DESCRAMBLER

The stream cipher function can be disabled by writing a 1 to bit 9 of MII register 10h. The stream cipher function is re-enabled by writing a 0 to this bit.

BYPASS NRZI ENCODER/DECODER

The NRZI encoder and decoder can be bypassed by writing a 1 to bit 8 of MII register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) can be re-enabled by writing a 0 to this bit.

BYPASS RECEIVE SYMBOL ALIGNMENT

Receive symbol alignment can be bypassed by writing a 1 to bit 7 of MII register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD[3:0] pins.

BASELINE WANDER CORRECTION DISABLE

The baseline wander correction circuit can be disabled by writing a 1 to bit 6 of MII register 10h. The BCM5222 corrects for baseline wander on the receive data signal when this bit is cleared.

RESERVED BITS

The reserved bits of the 100BASE-TX Auxiliary Control register must be written as 0 at all times. Ignore the BCM5222 outputs when these bits are read.

100BASE-TX AUXILIARY STATUS REGISTER

Table 16: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:10	Reserved	RO	Ignore when read	00h
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7	Remote Fault	RO	1 = Remote fault detected 0 = No remote fault detected	0
6	Reserved	RO	Ignore when read	0
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

LOCKED

The PHY returns a 1 in bit 9 when the descrambler is locked to the incoming data stream. Otherwise it returns a 0.

CURRENT 100BASE-TX LINK STATUS

The PHY returns a 1 in bit 8 when the 100BASE-TX link status is good. Otherwise it returns a 0.

REMOTE FAULT

The PHY returns a 1 while its link partner is signalling a far-end fault condition. Otherwise it returns a 0.

FALSE CARRIER DETECTED

The PHY returns a 1 in bit 5 of the Extended Status register if a false carrier has been detected since the last time this register was read. Otherwise it returns a 0.

BAD ESD DETECTED

The PHY returns a 1 in bit 4 if an end of stream delimiter error has been detected since the last time this register was read. Otherwise it returns a 0.

RECEIVE ERROR DETECTED

The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise it returns a 0.

TRANSMIT ERROR DETECTED

The PHY returns a 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise it returns a 0.

LOCK ERROR DETECTED

The PHY returns a 1 in bit 1 if the descrambler has lost lock since the last time this register was read. Otherwise it returns a 0.

MLT3 CODE ERROR DETECTED

The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it returns a 0.

100BASE-TX RECEIVE ERROR COUNTER

Table 17: 100BASE-TX Receive Error Counter (Address 18d, 12h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:0	Receive Error Counter [15:0]	R/W	Number of non-collision packets with receive errors since last read	0000h

RECEIVE ERROR COUNTER [15:0]

This counter increments each time the BCM5222 receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting receive errors until cleared.

100BASE-TX False Carrier Sense Counter

Table 18: 100BASE-TX False Carrier Sense Counter (Address 19d, 13h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore these bits	00h
7:0	False Carrier Sense Counter [7:0]	R/W	Number of false carrier sense events since last read	00h

False Carrier Sense Counter [7:0]

This counter increments each time the BCM5222 detects a false carrier on the receive input. This counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting False Carrier Sense Errors until cleared.

Auxiliary Control/Status Register

The Auxiliary Control/Status register bit descriptions are shown in Table 19.

Table 19: Auxiliary Control/Status Register (Address 11000b, 24d, 18h)

Bit	Name	R/W	Description	Default
15	Jabber Disable	R/W	1 = Jabber function disabled 0 = Jabber function enabled	0
14	Force Link	R/W	1 = Force link pass 0 = Normal link operation	0
13:9	Reserved	RO	Ignore when read	000000
8	10M Transmit Power Mode	R/W	1 = 10BASE-T Full Power Mode 0 = 10BASE-T Low Power Mode	0
7:6	HSQ : LSQ	R/W	These two bits define the squelch mode of the 10BASE-T Carrier Sense mechanism 00 = Normal Squelch 01 = Low Squelch 10 = High Squelch 11 = Not Allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indication	RO	1 = Auto-negotiation activated 0 = Speed forced manually	ANEN Pin
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-TX 0 = Speed forced to 10BASE-T	
1	Speed Indication	RO	1 = 100BASE-TX 0 = 10BASE-T	
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	

JABBER DISABLE

10BASE-T operation only. Bit 15 of the Auxiliary Control register allows the user to disable the jabber detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a 1 to bit 15 of the Auxiliary Control register, the jabber detect function is disabled. Writing a 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of jabber detect disable.

FORCE LINK

Writing a 1 to bit 14 of the Auxiliary Control register allows the user to disable the link integrity state machines, and place the BCM5222 into forced link pass status. Writing a 0 to this bit or resetting the chip restores the link integrity functions. Reading this bit returns the value of the force link bit.

10M TRANSMIT POWER MODE

Writing a 1 to bit 8 of the Auxiliary Control register allows the user to enable the 10BASE-T Full Power Mode. Writing a 0 to this bit or resetting the chip restores the setting to the 10BASE-T Low Power Mode.

HSQ AND LSQ

Extend or decrease the squelch levels for detection of incoming 10BASET data packets. The default squelch levels implemented are those defined in the IEEE standard. The high-and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5222 to operate properly over longer cable lengths. Decreasing the squelch levels can be useful in situations where there is a high level of noise present on the cables. Reading these 2 bits returns the value of the squelch levels.

EDGE RATE

Control bits used to program the transmit DAC output edge rate in both 10BASE-T and 100BASE-TX mode. A larger value on these bits produces slower transitions on the transmit waveform.

AUTO-NEGOTIATION INDICATION

This read-only bit indicates whether auto-negotiation has been enabled or disabled on the BCM5222. A combination of a 1 in bit 12 of the Control register and a logic 1 on the ANEN input pin is required to enable auto-negotiation. When auto-negotiation is disabled, bit 3 of the Auxiliary Control register (18h) returns a 0. At all other times, it returns a 1.

FORCE100/10 INDICATION

This read-only bit returns a value of 0 when one of following cases is true:

- The ANEN pin is low AND the F100 pin is low.
- The ANEN pin is high AND bit 12 of the Control register has been written 0 and bit 13 of the Control register has been written 0.

When bit 2 of the Auxiliary Control register (18h) is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto-negotiation is enabled), or the speed is forced to 100BASE-TX.

SPEED INDICATION

This read-only bit shows the true current operation speed of the BCM5222. A 1 indicates 100BASE-TX operation, and a 0 indicates 10BASE-T. While the auto-negotiation exchange is performed, the BCM5222 is always operating at 10BASE-T speed.

FULL-DUPLEX INDICATION

This read-only bit returns a 1 when the BCM5222 is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY STATUS SUMMARY REGISTER

The Auxiliary Status Summary register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bits can be found associated with their primary register descriptions. Table 20 indicates the bits found in this register.

Table 20: Auxiliary Status Summary Register (Address 11001b, 25d, 19h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed	0
14	Auto-Negotiation Complete Acknowledge	RO LH	1 = Auto-negotiation completed acknowledge state	0
13	Auto-Negotiation Acknowledge Detected	RO LH	1 = Auto-negotiation acknowledge detected	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-negotiation for link partner ability	0
11	Auto-Negotiation Pause	RO	BCM5222 and link partner pause operation bit	0
10:8	Auto-Negotiation HCD	RO	000 = No highest common denominator 001 = 10BASE-T 010 = 10BASE-T Full-Duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX Full-Duplex 11x = Undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel detection fault	0
6	Link Partner Remote Fault	RO	1 = Link partner remote fault	0
5	Link Partner Page Received	RO LH	1 = New page has been received	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link partner is auto-negotiation capable	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	

Table 20: Auxiliary Status Summary Register (Address 11001b, 25d, 19h) (Cont.)

Bit	Name	R/W	Description	Default
2	Link Status	RO LL	1 = Link is up (link pass state)	0
1	Auto-Negotiation Enabled	RO	1 = Auto-negotiation enabled	ANEN pin
0	Jabber Detect	RO LH	1 = Jabber condition detected	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

INTERRUPT REGISTER

Table 21: Interrupt Register (Address 26d, 1Ah)

Blt	Name	R/W	Description	Default
15	Reserved	R/W	Ignore when read	0
14	INTR Enable	R/W	Interrupt enable	0
13:12	Reserved	RO	Ignore when read	00
11	FDX Mask	R/W	Full-Duplex interrupt mask	1
10	SPD Mask	R/W	SPEED interrupt mask	1
9	LINK Mask	R/W	LINK interrupt mask	1
8	INTR Mask	R/W	Master interrupt mask	1
7:4	Reserved	RO	Ignore when read	0000
3	FDX Change	RO LH	Duplex change interrupt	0
2	SPD Change	RO LH	Speed change interrupt	0
1	LINK Change	RO LH	Link change interrupt	0
0	INTR Status	RO LH	Interrupt status	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

INTERRUPT ENABLE

Writing a 1 to bit 14 of the Interrupt register will enable the Interrupt function. By writing to bits [11:8] of the Interrupt register, the $\overline{\text{INTR}}$ pin will signal when the corresponding interrupt events occur. Writing a 0 to bit 14, or resetting the device will disable the Interrupt function.

FDX MASK

When this bit is set, changes in Duplex mode will not generate a hardware or software interrupt.

SPD MASK

When this bit is set, changes in operating speed will not generate a a hardware or software interrupt.

LINK MASK

When this bit is set, changes in Link status will not generate a a hardware or software interrupt.

INTERRUPT MASK

Master Interrupt Mask. When this bit is set, no interrupts will be hardware generated, regardless of the state of the other MASK bits.

FDX CHANGE

A “1” indicates a change of Duplex status since last register read. register read clears the bit.

SPD CHANGE

A “1” indicates a change of Speed status since last register read. register read clears the bit.

LINK CHANGE

A “1” indicates a change of Link status since last register read. register read clears the bit.

INTERRUPT STATUS

Represents status of the $\overline{\text{INTR}}$ pin. A “1” indicates that the Interrupt Mask is off and that one or more of the change bits are set. A register read clears the bit.

AUXILIARY MODE 2 REGISTER

Table 22: Auxiliary Mode 2 Register (Address 27d, 1Bh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:12	Reserved	RO	Ignore when read	0
11	10BT Dribble Bit Correct	R/W	1 = Enable, 0 = Disable	0
10	Jumbo Packet Enable	R/W	1 = Enable, 0 = Disable	0
9	Reserved	R/W	Write as 0, Ignore when read	00
8	TXC Invert	R/W	1= invert clock	0
7	Block 10BT Echo Mode	R/W	1 = Enable, 0 = Disable	1
6:4	Reserved	R/W	Write as 0, Ignore when read	000

Table 22: Auxiliary Mode 2 Register (Address 27d, 1Bh)

Bit	*Name*	*R/W*	*Description*	*Default*
3	Reserved	R/W	Write as 1, Ignore when read	1
2	Reserved	R/W	Write as 0, Ignore when read	0
1	Qual Parallel Detect Mode	R/W	1 = Enable, 0 = Disable	1
0	Reserved	RO	Ignore when read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

10BT Dribble Bit Correct

When enabled, the PHY rounds down to the nearest nibble when dribble bits are present on the 10Base-T input stream.

Jumbo Packet Enable

Writing a 1 to this bit enables jumbo sized packets to be received and transmitted.

TXC Invert

Writing a 1 to bit 8 of the Auxiliary Mode 2 register will invert the TXC clock.

Block 10BT Echo Mode

When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal does not echo onto the RXDV pin. The TXEN echoes onto the CRS pin and the CRS deassertion directly follows the TXEN deassertion.

Qualified Parallel Detect Mode

This bit allows the auto-negotiation/parallel detection process to be qualified with information in the Advertisement register.

If this bit is not set, the local BCM5222 device is enabled to Auto-Negotiate. If the far-end device is a 10BASE-T or 100BASE-TX non-Auto-Negotiating legacy type, the local device Auto-Negotiate/Parallel detects the far-end device, regardless of the Advertisement register (04h) contents.

If this bit is set, the local device compares the link speed detected to the contents of its Advertisement register. If the particular link speed is enabled in the Advertisement register, the local device asserts link. If the link speed is disabled in this register, then the local device does not assert link and continues monitoring for a matching capability link speed.

10BASE-T AUXILIARY ERROR AND GENERAL STATUS REGISTER

Table 23: 10BASE-T Auxiliary Error & General Status Register (Address 28d, 1Ch)

Bit	*Name*	*R/W*	*Description*	*Default*
15:14	Reserved	RO	Ignore when read	0
13	MDIX Status	RO	0 = MDI is in use 1 = MDIX is in use	0
12	MDIX Manual Swap	RW	0 = MDI or MDIX if MDIX is not disabled 1 = Force MDIX	0
11	HP Auto-MDIX disable	R/W	0 = Enable HP Auto-MDIX 1 = Disable HP Auto-MDIX	0
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	End Of Frame Error	RO	1 = EOF detection error (10BASE-T)	0
8:4	Reserved	RO	Ignore when read	00000
3	Auto-Negotiation Indication	RO	1 = Auto-negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-TX 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-TX 0 = 10BASE-T	0
0	Full-duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

Note: All Error bits in the Auxiliary Error and General Status Register are read-only and are latched high. When certain types of errors occur in the BCM5222, one or more corresponding error bits become “1”. They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER output pin at the time the error occurs.

R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

MDIX STATUS

When read as a 1, this bit indicates that the BCM5222 has its MDI TD+ and RD+ signals swapped either due to manually setting MDIX Swap bit to a 1 or through HP Auto-MDIX function if it is enabled and the BCM5222 has detected a MDI cross-over cable.

MDIX MANUAL SWAP

When this bit is set to a 1, the BCM5222 forces its MDI TD+ and RD+ signals to be swapped.

HP AUTO-MDIX DISABLE

When this bit is set to a 1, then the BCM5222 disables the HP Auto-MDIX function.

MANCHESTER CODE ERROR

Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

END OF FRAME ERROR

Indicates that the End Of Frame (EOF) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

AUTO-NEGOTIATION INDICATION

This read-only bit indicates whether auto-negotiation has been enabled or disabled on the BCM5222. A combination of a 1 in bit 12 of the Control register and a logic 1 on the ANEN input pin is required to enable auto-negotiation. When auto-negotiation is disabled, bit 15 of the Auxiliary Mode register returns a 0. At all other times, it returns a 1.

FORCE 100/10 INDICATION

This read-only bit returns a value of 0 when one of following two cases is true:

- The ANEN pin is low AND the F100 pin is low. (or)
- Bit 12 of the Control register has been written 0 AND bit 13 of the Control register has been written 0.

When bit 2 of the Auxiliary Control register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto-negotiation is enabled), or the speed is forced to 100BASE-TX.

SPEED INDICATION

This read-only bit shows the true current operation speed of the BCM5222. A 1 bit indicates 100BASE-TX operation, while a 0 indicates 10BASE-T. While the auto-negotiation exchange is performed, the BCM5222 is always operating at 10BASE-T speed.

FULL-DUPLEX INDICATION

This read-only bit returns a 1 when the BCM5222 is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY MODE REGISTER

Table 24 shows the bit descriptions for the Auxiliary Mode register.

Table 24: Auxiliary Mode Register (Address 11101b, 29d, 1Dh)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore when read	
4	Reserved	R/W	Write as 0, Ignore when Read	0
3	Link LED Disable	R/W	1 = Disable link LED output 0 = Enable link LED output	0
2	Reserved	RO	Ignore when read	0
1	Block TXEN Mode	R/W	1 = Enable block TXEN mode 0 = Disable block TXEN mode	0
0	Reserved	RO	Ignore when read	0

LINK LED DISABLE

When set to 1, disables the Link LED output pin. When 0, Link LED output is enabled.

BLOCK TXEN MODE

When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles results in the insertion of two IDLEs before the beginning of the next packet's JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

Table 25: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

Bit	Name	R/W	Description	Default
15	HCD_TX_FDX	RO	1 = Auto-negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	1 = Auto-negotiation result is 100BASE-T4	0
13	HCD_TX	RO	1 = Auto-negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto-negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when read	00
8	Restart Auto-Negotiation	R/W (SC)	1 = Restart auto-negotiation process 0 = (No effect)	0
7	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	0
6	Acknowledge Complete	RO	1 = Auto-negotiation acknowledge completed	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

Table 25: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

Bit	*Name*	*R/W*	*Description*	*Default*
5	Acknowledge Detected	RO	1 = Auto-negotiation acknowledge detected	0
4	Ability Detect	RO	1 = Auto-negotiation waiting for LP ability	0
3	Super Isolate	R/W	1 = Super isolate mode 0 = Normal operation	0
2	Reserved	RO	Ignore when read	0
1	10BASE-T Serial Mode	R/W	1 = Enable 10BASE-T serial mode 0 = Disable 10BASE-T serial mode	0
0	Reserved	R/W	Write as 0, Ignore when read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

HCD BITS

Bits 15:11 of the Auxiliary Multiple PHY register are 5 read-only bits that report the Highest Common Denominator (HCD) result of the auto-negotiation process. Immediately upon entering the link pass state after each reset or restart auto-negotiation, only 1 of these 5 bits is 1. The link pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time auto-negotiation is restarted or the BCM5222 is reset. For their intended application, these bits uniquely identify the HCD only after the first link pass after reset or restart of auto-negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the link partner is different, more than 1 of the above bits can be active.

RESTART AUTO-NEGOTIATION

This self-clearing bit allows the auto-negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, auto-negotiation must be enabled. Writing a 1 to this bit restarts auto-negotiation. Since the bit is self-clearing, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Control register.

Auto-Negotiation Complete

This read-only bit returns a 1 after the auto-negotiation process has been completed. It remains 1 until the auto-negotiation process is restarted, a Link Fault occurs, or the chip is reset. If auto-negotiation is disabled or the process is still in progress, the bit returns a 0.

ACKNOWLEDGE COMPLETE

This read-only bit returns a 1 after the acknowledgment exchange portion of the auto-negotiation process has been completed and the Arbitrator state machine has exited the Complete Acknowledge state. It remains this value until the auto-negotiation process is restarted, a Link Fault occurs, auto-negotiation is disabled, or the BCM5222 is reset.

ACKNOWLEDGE DETECTED

This read-only bit is set to 1 when the arbitrator state machine exits the acknowledged detect state. It remains high until the auto-negotiation process is restarted, or the BCM5222 is reset.

Ability Detect

This read-only bit returns a 1 when the auto-negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the auto-negotiation process begins, and exits after the first FLP burst or link pulses are detected from the link partner. This bit returns a 0 any time the auto-negotiation state machine is not in the Ability Detect state.

Super Isolate

Writing a 1 to this bit places the BCM5222 into the Super Isolate mode. Similar to the Isolate mode, all MII inputs are ignored, and all MII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5222 to coexist with another PHY on the same adapter card, with only one being activated at any time.

10BASE-T Serial Mode

Writing a 1 to bit 1 of the Auxiliary Mode register enables the 10BASE-T Serial mode. In the normal 10BASE-T mode of operation, as defined by the MII standard, transmit and receive data packets traverse the TXD[3:0] and RXD[3:0] busses at a rate of 2.5 MHz. In the special 10BASE-T Serial mode, data packets traverse to the MAC layer across only TXD0 and RXD0 at a rate of 10 MHz. Serial operation is not available in 100BASE-TX mode.

Broadcom Test Register

Table 26: Broadcom Test (Address 31d, 1Fh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:8	Reserved	RO	Ignore when read	00h
7	Shadow Register Enable	R/W	1 = Enable Shadow registers 0 = Disable Shadow registers	0
6	Reserved	RO	Ignore when read	0
5	Reserved	R/W	Write as 0, Ignore when read	0
4:0	Reserved	R/W	Write as 0Bh, Ignore when read	0Bh

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).

Shadow Register Enable

Writing a 1 to bit 7 of register 1Fh allows R/W access to the Shadow registers.

AUXILIARY MODE 4 REGISTER (SHADOW REGISTER)

Table 27: Auxiliary Mode 4 Register (Shadow Register 26d, 1Ah)

Blt	*Name*	*R/W*	*Description*	*Default*
15:6	Reserved	R/W	Write as 30h, Ignore when read	30h
5:4	Force LED [1:0]	R/W	01 = Force all LED status to on 0 state 10 = Force all LED status to off 1 state	00
3	Reserved	R/W	Write as 0, Ignore when read	0
2	Enable Clock During Low Power	R/W	0 = Disables clock during low power modes 1 = Enables clock during low power modes	0
1	Force Low Power Mode	R/W	0 = Normal operation 1 = Forces the 5222 to enter the low power mode	0
0	Force IDDQ Mode	R/W	0 = Normal operation 1 = Causes the BCM5222 to go to IDDQ mode	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.

FORCE LED [1:0]

The $\overline{\text{SPDLED}}$, $\overline{\text{LNKLED}}$, $\overline{\text{ACTLED}}$ and $\overline{\text{FDXLED}}$ outputs can be forced to on state (0) by writing a value of 01 to Force LED [1:0]. These LEDs can be forced to off state (1) by writing a value of 10 to Force LED {1:0].

ENABLE CLOCK DURING LOW POWER

If this bit is set to a 1 then the clocks are running in low mode.

FORCE IDDQ MODE

If this bit is set to a 1, then the BCM5222 enters IDDQ mode. When the device is in IDDQ mode, everything is disabled. The BCM5222 requires a hard reset to return to normal mode.

AUXILIARY STATUS 2 REGISTER (SHADOW REGISTER)

Table 28: Auxiliary Status 2 Register (Shadow Register 27d, 1Bh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	MLT3 Detected	R/O	1 = MLT3 Detected	0h
14:12	Cable Length 100X [2:0]	R/O	The BCM5222 shows the cable length in 20 meters increment as shown in the table below	000
11:6	ADC Peak Amplitude [5:0]	R/O	A to D peak amplitude seen	00h
5:0	Reserved	R/W	Write as 0, Ignore when read	01h

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.

MLT3 DETECTED

The BCM5222 returns a 1 in this bit whenever MLT3 signaling is detected.

CABLE LENGTH 100X [2:0]

The BCM5222 provides the cable length for each port when a 100TX link is established.

Table 29: Cable Length

Cable Length 100x [2:0]	*Cable Length in Meters*
000	< 20
001	20 to <40
010	40 to <60
011	60 to < 80
100	80 to < 100
101	100 to < 120
110	120 to < 140
111	> 140

ADC PEAK AMPLITUDE [5:0]

The BCM5222 returns the AD converter's 6-bit peak amplitude seen during this link.

AUXILIARY STATUS 3 REGISTER (SHADOW REGISTER)

Table 30: Auxiliary Status 3 Register (Shadow Register 28d, 1Ch)

Bit	Name	R/W	Description	Default
15:8	Noise [7:0]	R/O	Current mean square error value, valid only if link is established	00h
7:4	Reserved	R/W	Write as 0, ignore when read	0h
3:0	FIFO Consumption [3:0]	R/O	Currently utilized number of nibbles in the receive FIFO	0000
Note: MII Shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1				

NOISE [7:0]

The BCM5222 provides the current mean squared error value for noise when a valid link is established.

FIFO CONSUMPTION [3:0]

The BCM5222 indicates the number of nibbles of FIFO currently used.

AUXILIARY MODE 3 REGISTER (SHADOW REGISTER)

Table 31: Auxiliary Mode 3 Register (Shadow Register 29d, 1Dh)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Write as 00h, ignore when read	000h
3:0	FIFO Size Select [3:0]	R/W	Currently selected receive FIFO Size	4h
Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII register 1Fh bit 7 to a 1.				

FIFO SIZE SELECT [3:0]

The BCM5222 indicates the current selection of receive FIFO size using bit 3 through 0 as shown in Table 32.

Table 32: Current Receive FIFO Size

FIFO Size Select [3:0]	Receive FIFO Size in Use (# of Bits)
0001	16
0010	20
0011	24
0100	28

Table 32: Current Receive FIFO Size (Cont.)

FIFO Size Select [3:0]	*Receive FIFO Size in Use (# of Bits)*
0101	32
0110	36
0111	40
1000	44
1001	48
1010	52
1011	56
1100	60
1101	64

AUXILIARY STATUS 4 REGISTER (SHADOW REGISTER)

Table 33: Auxiliary Status 4 Register (Shadow Register 30d, 1Eh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:0	Packet Length Counter[15:0]	R/O	Number of bytes in the last received packet	0000h

PACKET LENGTH COUNTER [15:0]

The BCM5222 shows the number bytes in the last packet received. This is valid only when a valid link is established.

Section 6: Timing and AC Characteristics

The timing information contained in this section applies to the BCM5222.

All MII Interface pins comply with IEEE 802.3u timing specifications (see Reconciliation Sublayer and Media Independent Interface in IEEE 802.3u timing specifications). All digital output timing specified at C_L = 30 pF.

Output rise/fall times measured between 10% and 90% of the output signal swing. Input rise/fall times measured between V_{IL} max. and V_{IH} min. Output signal transitions referenced to the midpoint of the output signal swing. Input signal transitions referenced to the midpoint between V_{IL} max. and V_{IH} min. See Table 34and Table 35 for the timing parameters. See Figure 4 for an illustration of clock and reset timing.

Table 34: Clock Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
XTALI Cycle Time	CK_CYCLE	39.998	40	40.002	ns
XTALI High/Low Time	CK_HI CK_LO	14	20	26	ns
XTALI Rise/Fall Time	CK_EDGE			4	ns

Table 35: Reset Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
Reset Pulse Length with stable XTALI Input	RESET_LEN	400			ns
Activity after end of Hardware Reset	RESET_WAIT	100			µs
$\overline{\text{RESET}}$ Rise/Fall Time	RESET_EDGE			10	ns

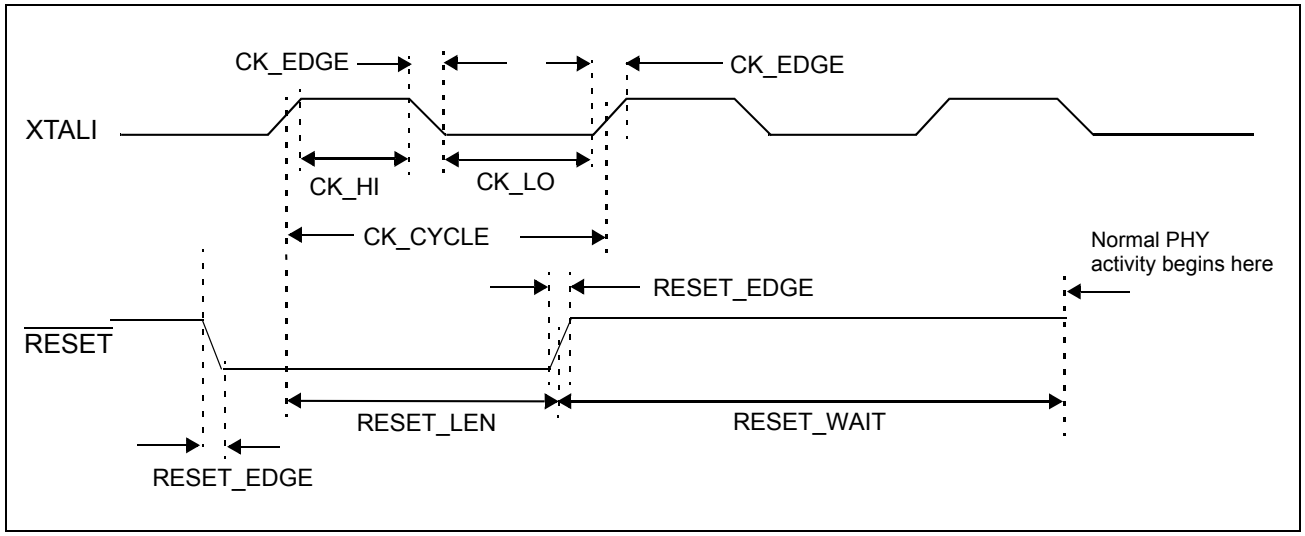


Figure 4: Clock and Reset Timing

Table 36 provides the parameters for 100BASE-TX transmit timing. Figure 5 illustrates the 100BASE-TX transmit start of packet timing and Figure 6 shows the100BASE-TX transmit end of packet timing.

Table 36: MII 100BASE-TX Transmit Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
TXC Cycle Time			40		ns
TXC High/Low Time		16	20	24	ns
TXC Rise/Fall Time		2		5	ns
TXEN, TXD[3:0] Setup Time to TXC rising*	TXEN_SETUP	10			ns
TXEN, TXD[3:0] Hold Time from TXC rising*	TXEN_HOLD	0			ns
TD± after TXEN Assert	TXEN_TDATA	60		140	ns
TXD to TD± Steady State Delay	TXD_TDATA	60		100	ns
CRS Assert after TXEN Assert	TXEN_CRS	0		40	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	0		160	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL				ns
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP				ns
TXEN, TXD[3:0] Setup Time to XTALI rising*		2			ns
TXEN, TXD[3:0] Hold Time from XTALI rising*		10			ns

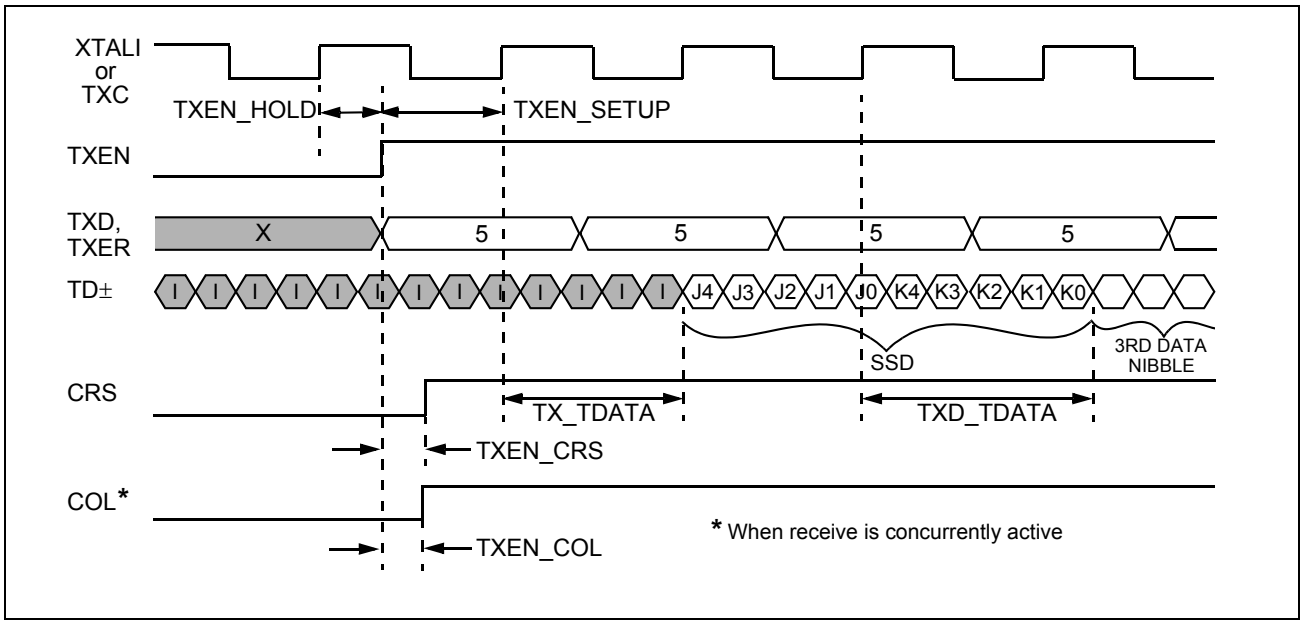


Figure 5: MII Transmit Start of Packet Timing (100BASE-TX)

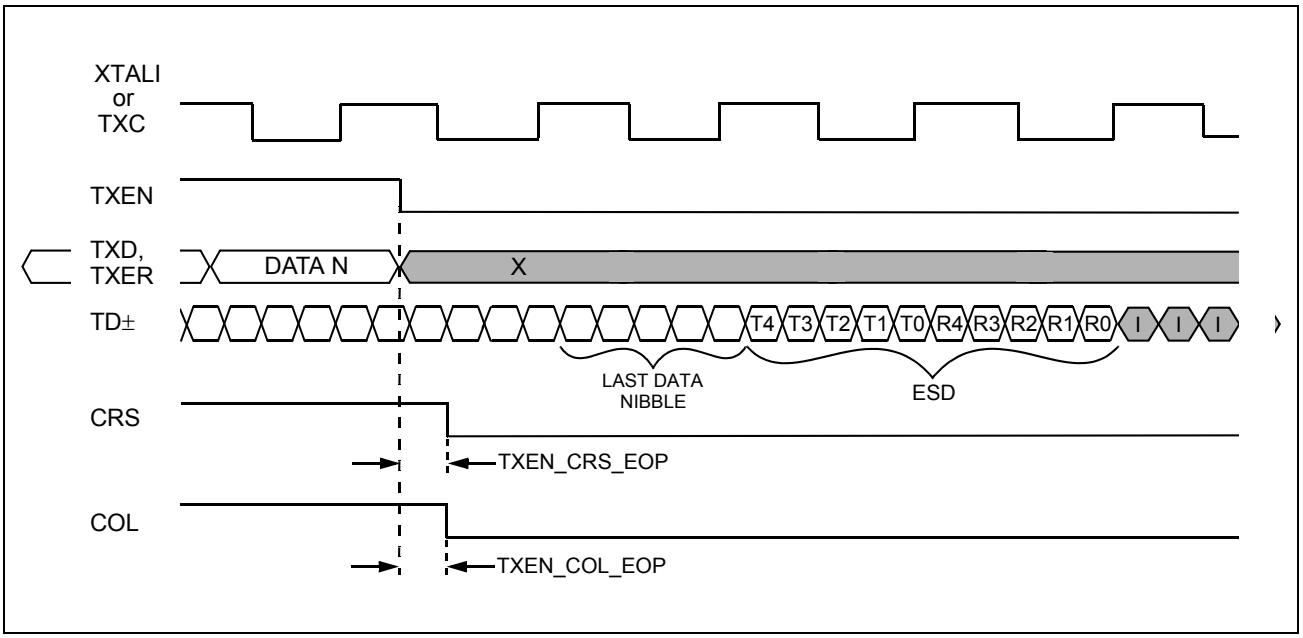


Figure 6: MII Transmit End of Packet Timing (100BASE-TX)

Table 37 below provides 100BASE-X receive timing parameters. See Figure 7 on page 50 and Figure 8 on page 51 for illustrations of 100BASE-TX receive start of packet timing parameters and 100BASE-TX receive end of packet timing. Figure 9 on page 51 shows 100BASE-TX receive packet premature end. See Figure 10 on page 52 for an illustration of link failure or stream cipher error during receive packet. 100BASE-TX False carrier sense timing is shown in Figure 11 on page 52.

Table 37: MII 100BASE-TX Receive Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
RXC Cycle Time			40		ns
RXC High/Low Time (RXDV asserted)		16	20	24	ns
RXC High Time (RXDV deasserted)			20		ns
RXC Low Time (RXDV deasserted)			20		ns
RXC Rise/Fall Time			TBD		ns
RXDV, RXER, RXD[3:0] Delay from RXC falling		-4		4	ns
CRS Deassert from RXC falling (valid EOP only)			TBD		ns
CRS Assert after RD±	RX_CRS			200	ns
CRS Deassert after RD± (valid EOP)	RX_CRS_EOP	60		240	ns
CRS Deassert after RD± (premature end)	RX_CRS_IDLE		150		ns
RXDV Assert after RD±	RX_RXDV		160		ns
RXDV Deassert after RD± (valid EOP)	RX_RXDV_EOP		200		ns
RXDV Assert after CRS			60		ns
RD± to RXD Steady State Delay	RX_RXD			180	ns
COL Assert after RD± (while TX)	RX_COL			200	ns
COL Deassert after RD± (valid EOP)	RX_COL_EOP	130		240	ns

Table 37: MII 100BASE-TX Receive Timing (Cont.)

Parameter	Symbol	Min	Typical	Max	Unit
COL Deassert after RD± (premature end)	RX_COL_IDLE	130		240	ns

Note: RXC minimum high and low times are guaranteed when RXEN is asserted or deasserted. The MII port will always tristate while RXEN is low.

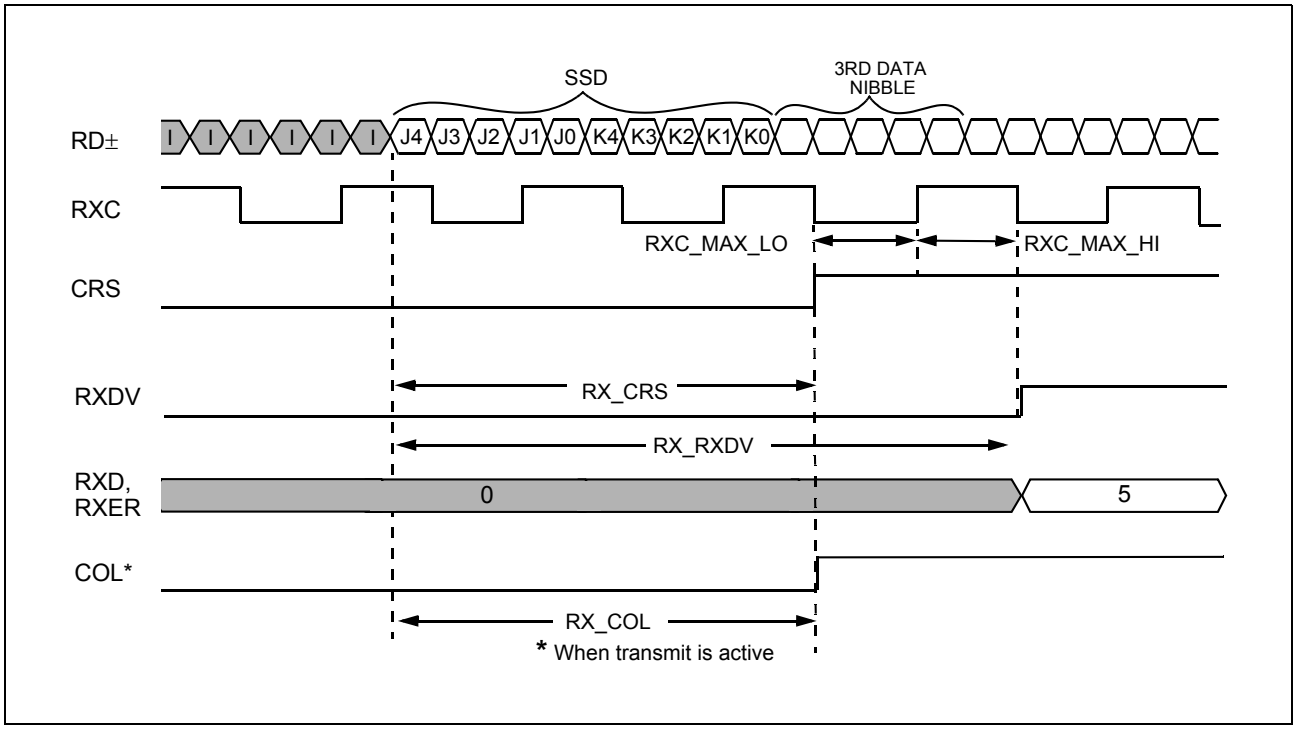


Figure 7: MII Receive Start of Packet Timing (100BASE-TX)

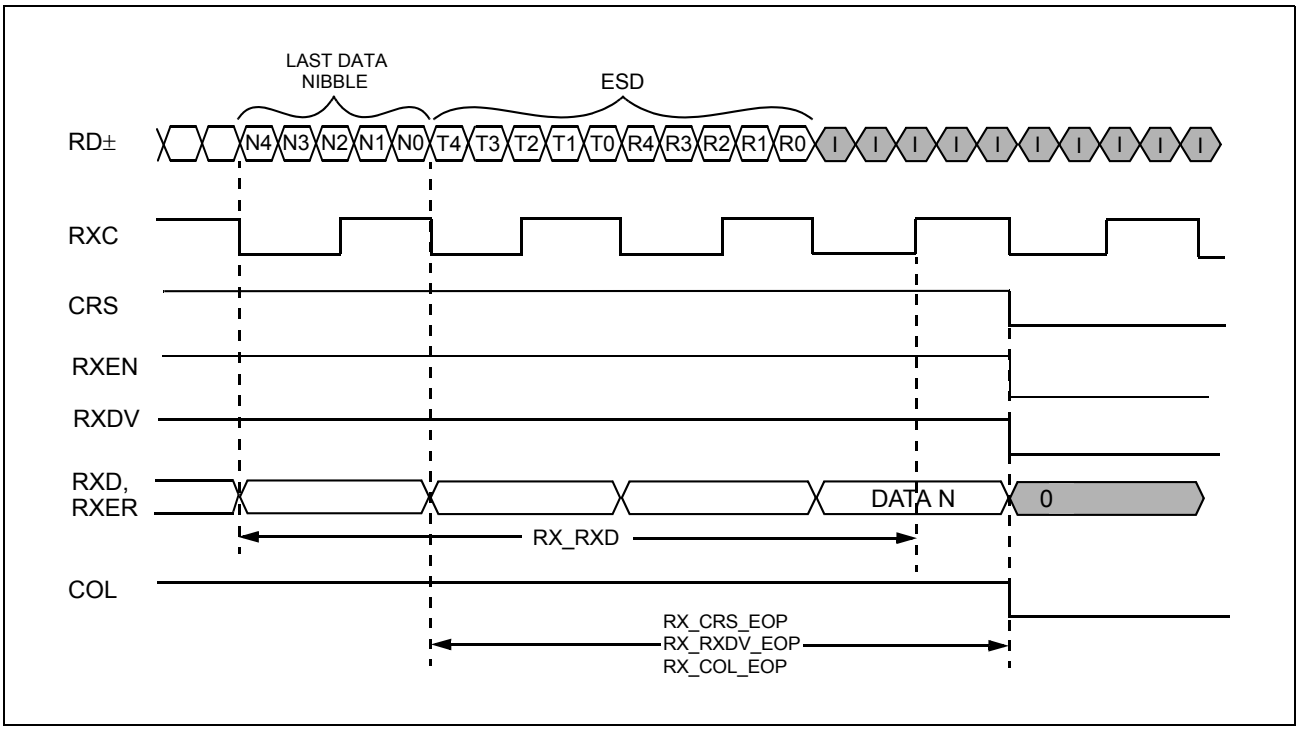


Figure 8: MII Receive End of Packet Timing (100BASE-TX

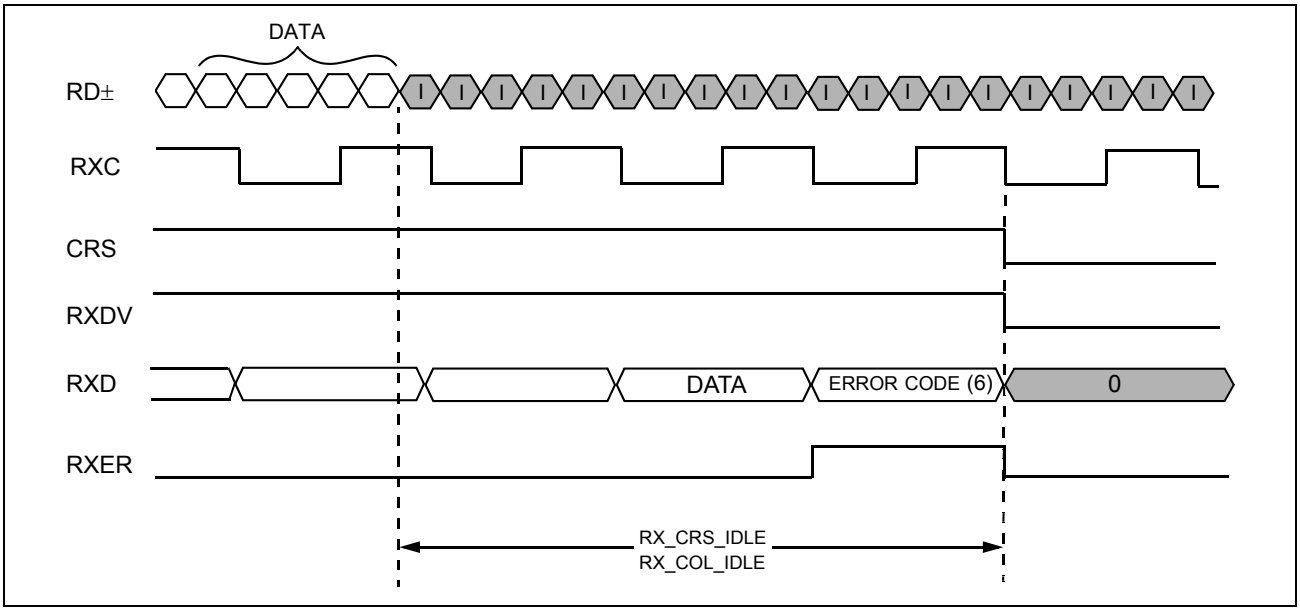


Figure 9: MII Receive Packet Premature End (100BASE-TX)

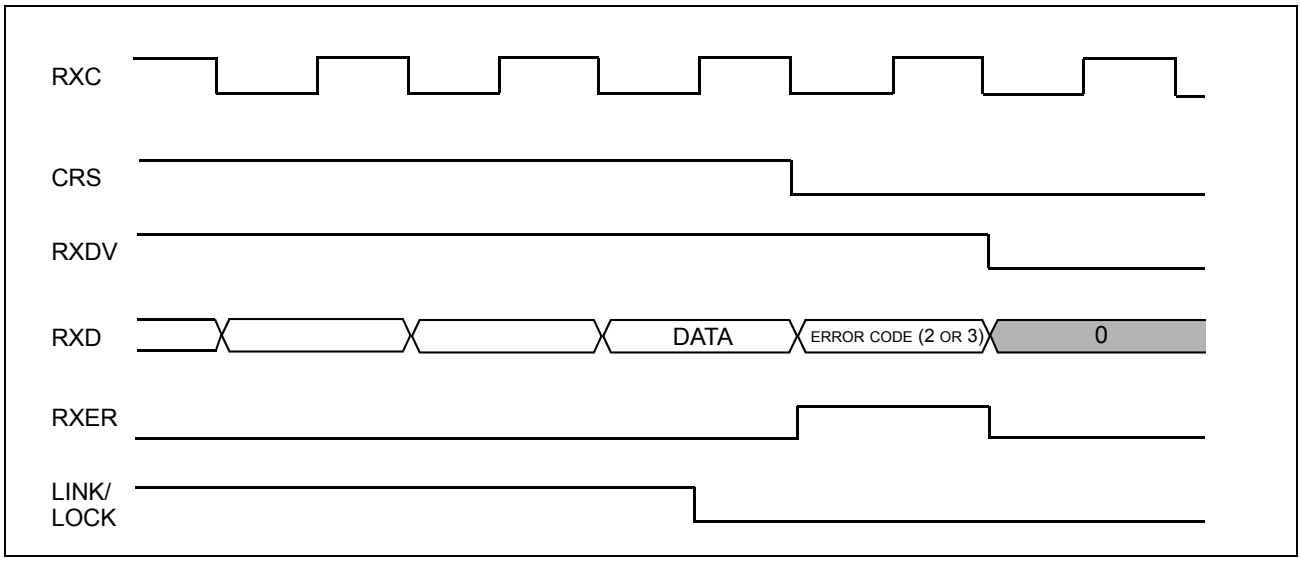


Figure 10: MII Link Failure or Stream Cipher Error During Receive Packet

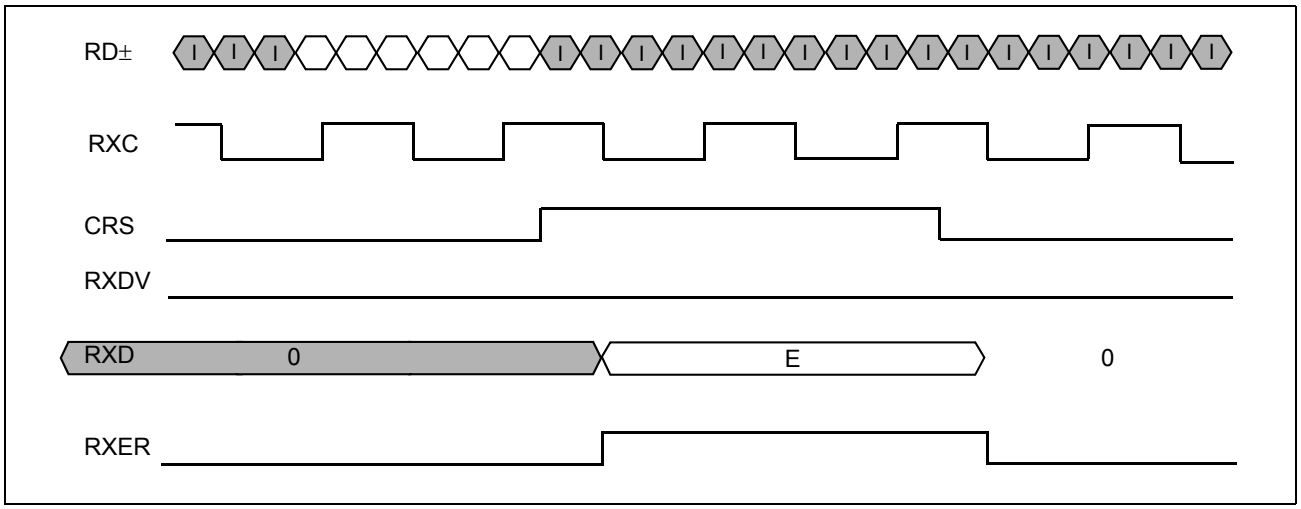


Figure 11: MII False Carrier Sense Timing (100BASE-TX)

Table 38 provides the parameters for 10BASE-T transmit timing. Figure 12 illustrates 10BASE-T transmit start of timing packet.

Table 38: MII 10BASE-T Transmit Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
TXC Cycle Time (10BASE-T)	TXC_CYCLE		400		ns
TXC High/Low Time (10BASE-T)			200		ns
TXC Rise/Fall Time		2		5	ns
TXC Rising edge to TXEN valid	TXC_TXEN_VALID			25	ns
TXC Rising edge to TXEN hold	TXC_TXEN_HOLD	75			ns
TXC Rising edge to TXD valid	TXC_TXD_VALID			25	ns
TXC Rising edge to TXD hold	TXC_TXD_HOLD	75			ns
TD± after TXEN Assert	TXEN_TDATA	60		360	ns
CRS Assert after TXEN Assert	TXEN_CRS		TBD	TBD	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP		TBD	TBD	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL				
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP				
Idle on Twisted Pair after TXEN De-Assert	TX_QUIET		450	800	ns

Note: TXD, TXEN delivered to the BCM5222 should be generated of the rising edge of TXC.

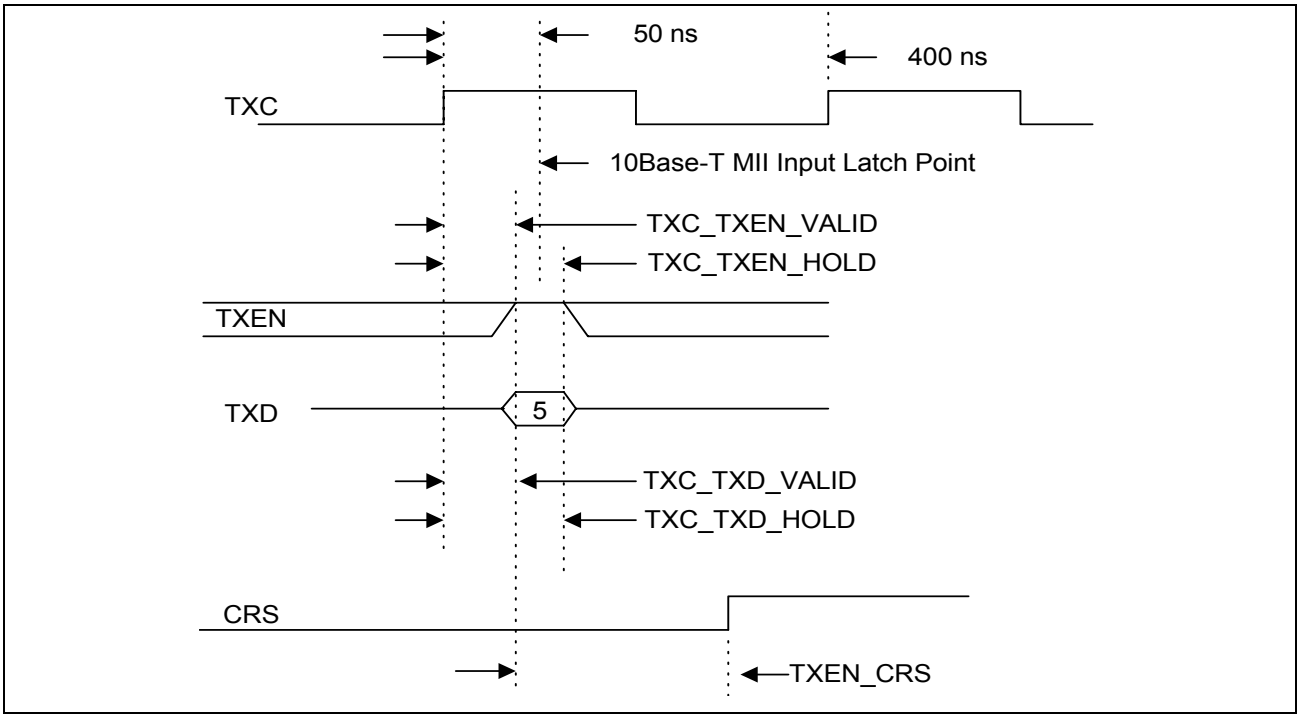


Figure 12: MII 10BASE-T Transmit Start of Packet Timing

Table 39 provides the parameters for MII 10BASE-T receive timing. MII 10BASE-T collision timing is shown in Table 40.

Table 39: MII 10BASE-T Receive Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
RXC Cycle Time	RXC_CYCLE		400		ns
RXC High/Low Time			200		ns
CRS Assert after Receive Analog Data	RX_CRS_BT			300	ns
RXC Valid after CRS Assert	RXC_VALID			2000	ns
RXDV Assert after Receive Analog Data	RX_RXDV			2300	ns
RXDV Deassert after Receive Analog EOP ends	RX_NOT_RXDV			560	ns
CRS Deassert after Receive Analog EOP ends	RX_NOT_CRS			560	ns

Table 40: MII 10BASE-T Collision Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
COL Assert after Receive Analog (while transmitting)	RX_COL		TBD		ns
COL Deassert after TXEN Deassert (while receiving)	TXEN_NOT_COL		TBD		ns
COL Assert after TXEN Assert (while receiving)	TXEN_COL		TBD		ns
COL Deassert after Receive Analog ends (while transmitting)	RX_NOT_COL		TBD		ns

Table 41: 10BASE_T Serial Transmit Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
TXC Cycle Time	TXC	95	100	105	ns
TXC Low Time TXC High Time	TXC_LO TXC_HIGH	35	50	65	ns
TXC Rise Time TXC Fall Time	TXC_RISE TXC_FALL	2		10	ns
TXEN, TXD0 to TXC Rising	TXEN_SETUP	10			
TXEN, TXD0 Hold after TXC Rising	TXEN_HOLD	4			
TXEN to TD± Start	TXEN_TDATA			500	ns
TXEN to TD± End	TXEN_QUIET			500	ns

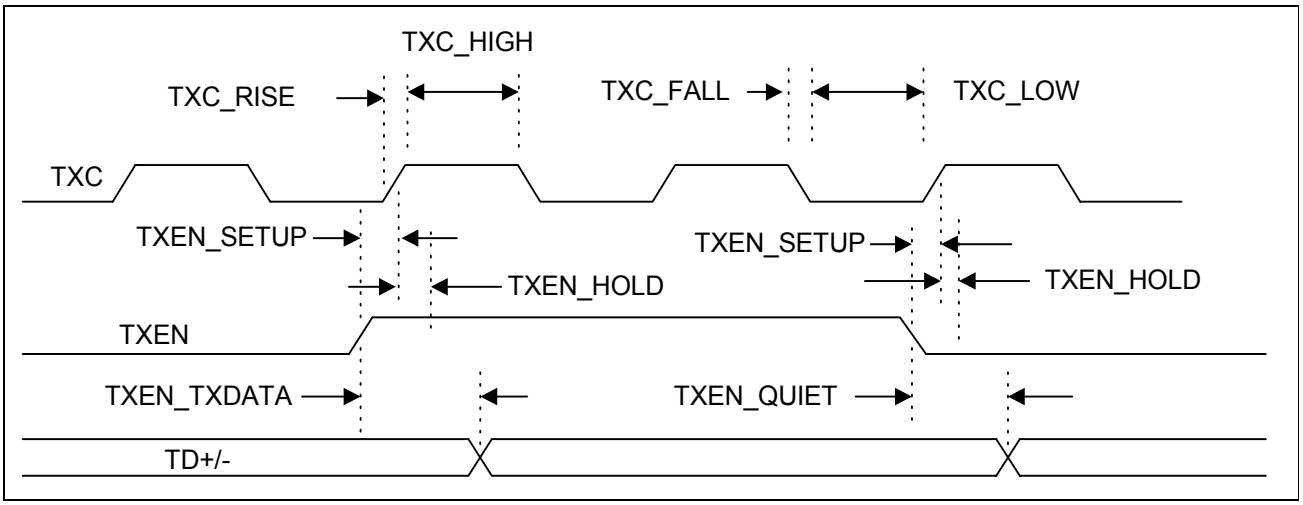


Figure 13: 10BASE-T Serial Transmit Timing

Table 42: 10BASE_T Serial Receive Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
RXC Cycle Time	RXC	95	100	105	ns
RXC Low Time RXC High Time	RXC_LO RXC_HIGH	35	50	65	ns
RXC Rise Time RXC Fall Time	RXC_RISE RXC_FALL	2	-	10	ns
RXC to RXD0 Output Delay	RXD_DELAY			5	ns
CRS Assert after RD±	RX_CRS_DV			300	ns
CRS Deassert after RD±, valid EOP	RX_NOT_CRS			560	ns

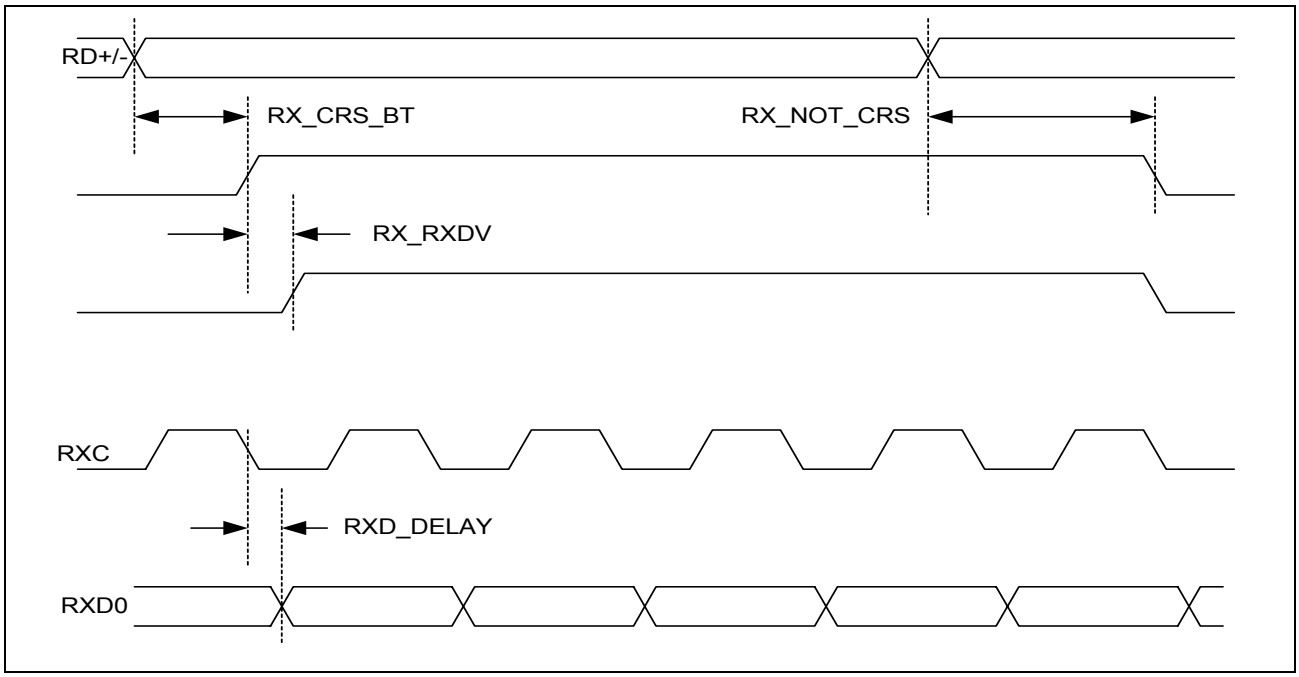


Figure 14: 10BASE-T Serial Receive Timing

Table 43, Table 44, and Table 45 provide the parameters for loopback timing, auto-negotiation timing, and LED timing.

Table 43: Loopback Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
TXD to RXD Steady State Propagation Delay			250		ns

Table 44: Auto-Negotiation Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
Link Test Pulse Width			100		ns
FLP Burst Interval			16		ms
Clock Pulse to Clock Pulse			123		µs
Clock Pulse to Data Pulse (Data = 1)			62.5		µs

Table 45: LED Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
LED On Time ($\overline{\text{ACTLED}}$)			80		ms
LED Off Time ($\overline{\text{ACTLED}}$)			80		ms

Management data interface timing parameters are described in Table 46. Figure 15 and Figure 16 illustrate two types of management interface timing.

Table 46: Management Data Interface Timing

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
MDC Cycle Time		40			ns
MDC High/Low		20			ns
MDC Rise/Fall Time				10	ns
MDIO Input Setup Time to MDC rising		10			ns
MDIO Input Hold Time from MDC rising		4			ns
MDIO Output Delay from MDC rising		0		30	ns

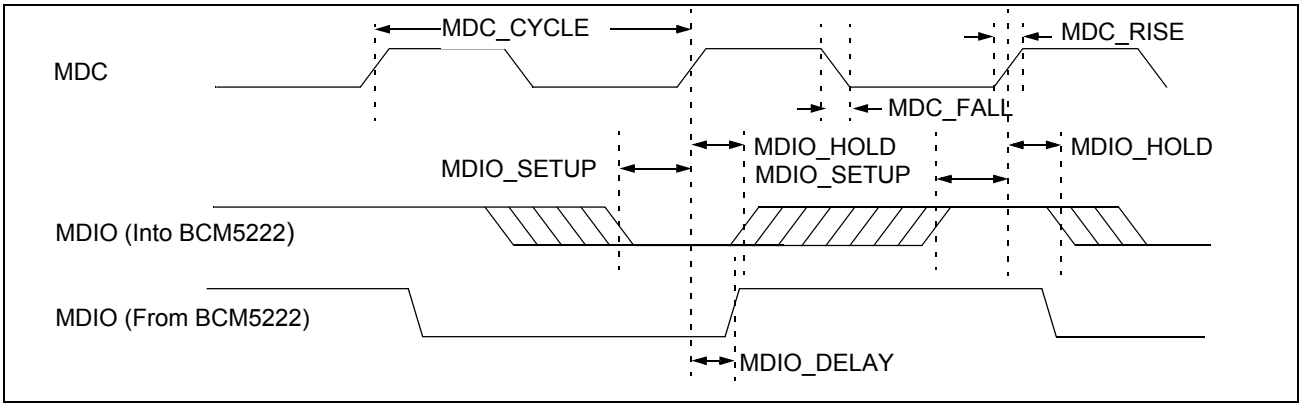


Figure 15: Management Interface Timing

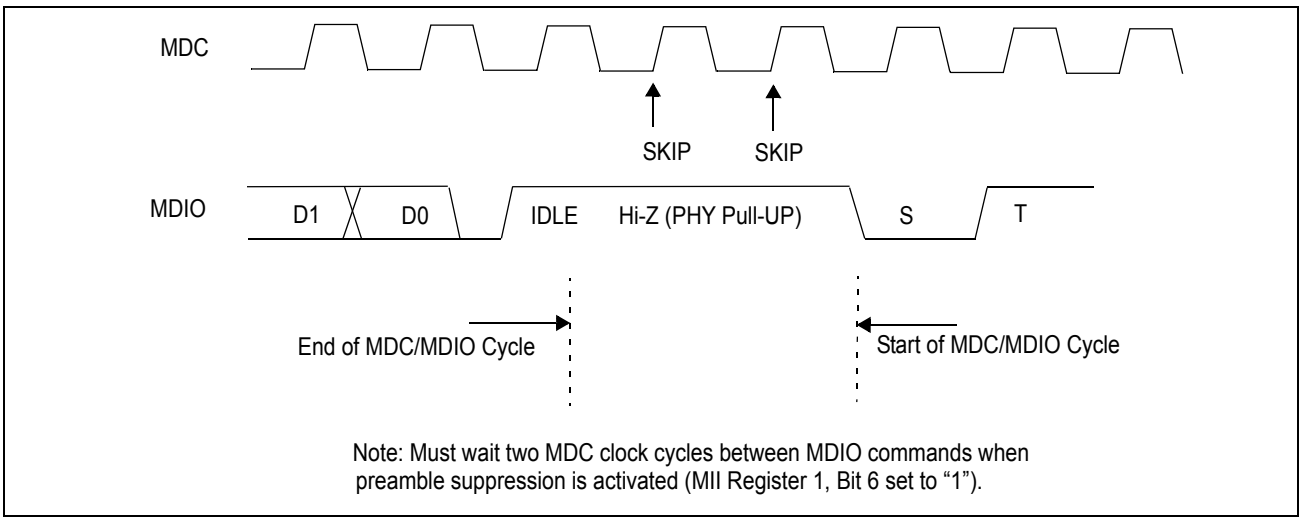


Figure 16: Management Interface Timing (with Preamble Suppression On)

Section 7: Electrical Characteristics

Table 47 provides the absolute maximum ratings for the BCM5222. The recommended operating conditions for the BCM5222 are shown in Table 48. Table 49 provides the package thermal characteristics. Table 51 on page 59 gives the electrical characteristics of the BCM5222.

Table 47: Absolute Maximum Ratings

Symbols	*Parameter*	*Pin*	*Min*	*Max*	*Unit*
V_{DD}	Supply Voltage	OVDD, BIASVDD	GND - 0.3	3.465	V
		DVDD, AVDD, PLLAVDD	GND - 0.3	1.89	V
V_I	Input Voltage		GND - 0.3	OVDD + 0.3	V
I_I	Input Current			±10	mA

Note: *These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.*

Table 48: Recommended Operating Conditions for BCM5222

Symbol	*Parameter*	*Pin*	*Operating Mode*	*Min*	*Max*	*Unit*
V_{DD}	Supply Voltage BCM5222	OVDD, BIASVDD		3.135	3.465	V
		DVDD, AVDD, PLLAVDD		1.71	1.89	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0	OVDD	V
		XTALI		1.2	2.0	V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
		XTALI		0	0.4	V
V_{IDIFF}	Differential Input Voltage	RD±	100BASE-TX	150		mV
V_{ICM}	Common Mode Input Voltage	RD±	3.3V Center Tap	1.85	2.05	V
		RD±	2.5V Center Tap	1.15	1.35	V
T_A	Ambient Operating Temperature - 5222			-40	85	°C

Table 49: Package Thermal Characteristics (BCM5222KQM)

Ambient Air Temperature	θ_{JA} *in Still Air (°C)*	θ_{JB} *(°C/W)*	θ_{JC} *(°C/W)*
70	56.96	61.73	40.28

Table 50: Package Thermal Characteristics (BCM5222KPF)

Ambient Air Temperature	θ_{JA} *in Still Air (°C)*	θ_{JB} *(°C/W)*	θ_{JC} *(°C/W)*
70	41.00	15.68	25.56

Table 51: Electrical Characteristics

Symbol	*Parameter*	*Pins*	*Condition*	*Min*	*Typical*	*Max*	*Unit*
I_{DD}	Supply Current	AVDD, PLVDD, DVDD	100BASE-TX		109		mA
		BIASVDD, OVDD	Hardware/ Software		44		mA
V_{OH}	High-Level Output Voltage	All Digital Outputs	I_{OH} = –12 mA	OVDD -0.5			V
		TD±	driving loaded magnetics module			AVDD +1.5	V
V_{OL}	Low-Level Output Voltage	All Digital Outputs	I_{OL} = 8 mA			0.4	V
		TD±	driving loaded magnetics module	AVDD -1.5			V
V_{ODIFF}	Differential Output Voltage	TD±		400			mV
I_I	Input Current	Digital Inputs w/ Pull-Up Resistors	V_I = OVDD			+100	µA
			V_I = DGND			-200	µA
		Digital Inputs w/ Pull-Down Resistors	V_I = OVDD			+200	µA
			V_I = DGND			-100	µA
		All Other Digital Inputs	DGND ≤ V_I ≤ OVDD			+100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	DGND ≤ V_O ≤ OVDD				µA
		All Open-Drain Outputs	V_O = OVDD				µA
V_{BIAS}	Bias Voltage	RDAC		1.18		1.30	V

Note: Current supplied through the center tap of the magnetics can be supplied at either 2.5V or 3.3V. Current sunk through the BCM5222 is 90mA.

Section 8: Application Example

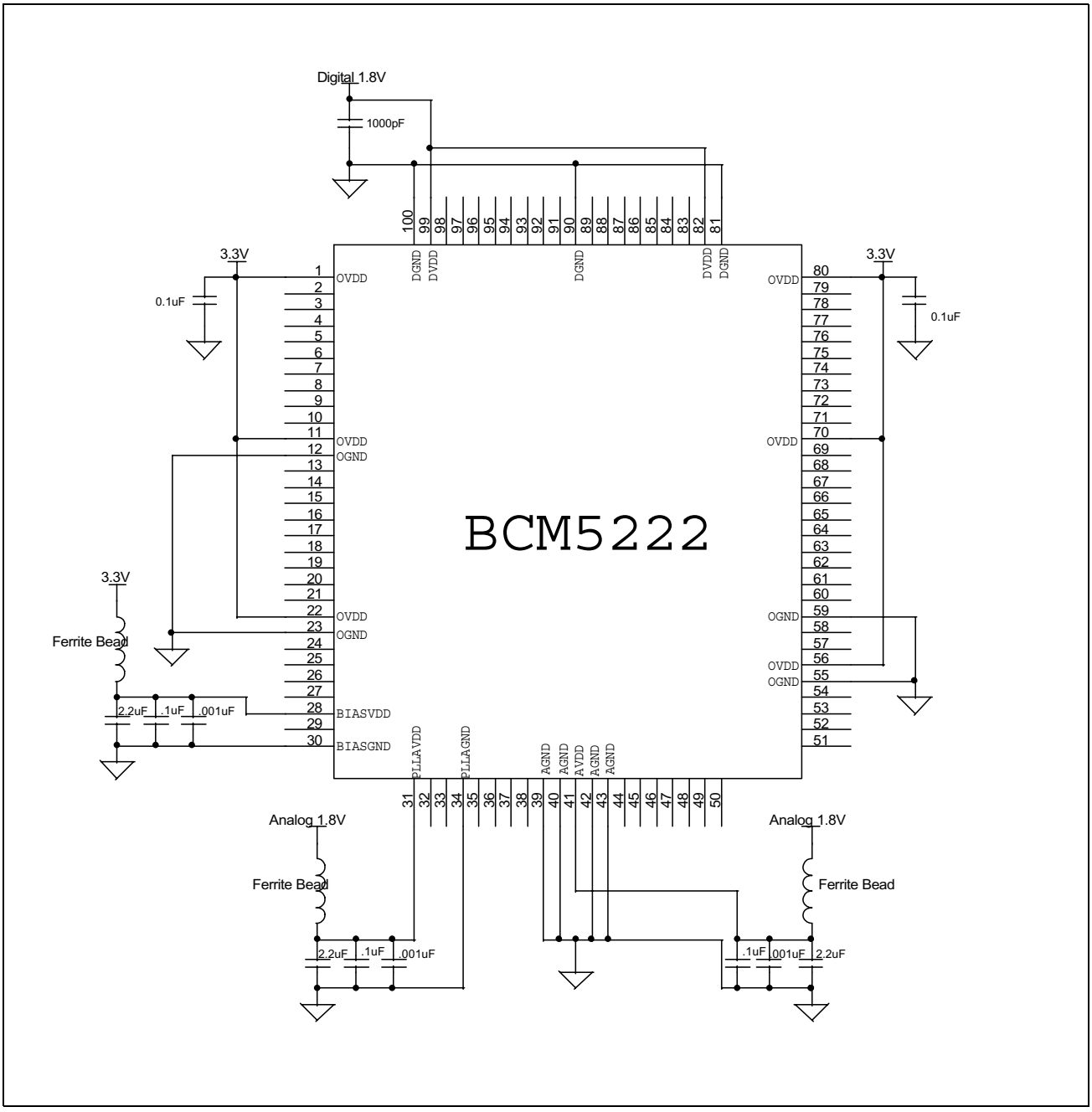


Figure 17: BCM5222 1.8V and 3.3V Power Connections in 100 MQFP Package

Section 9: Mechanical Information

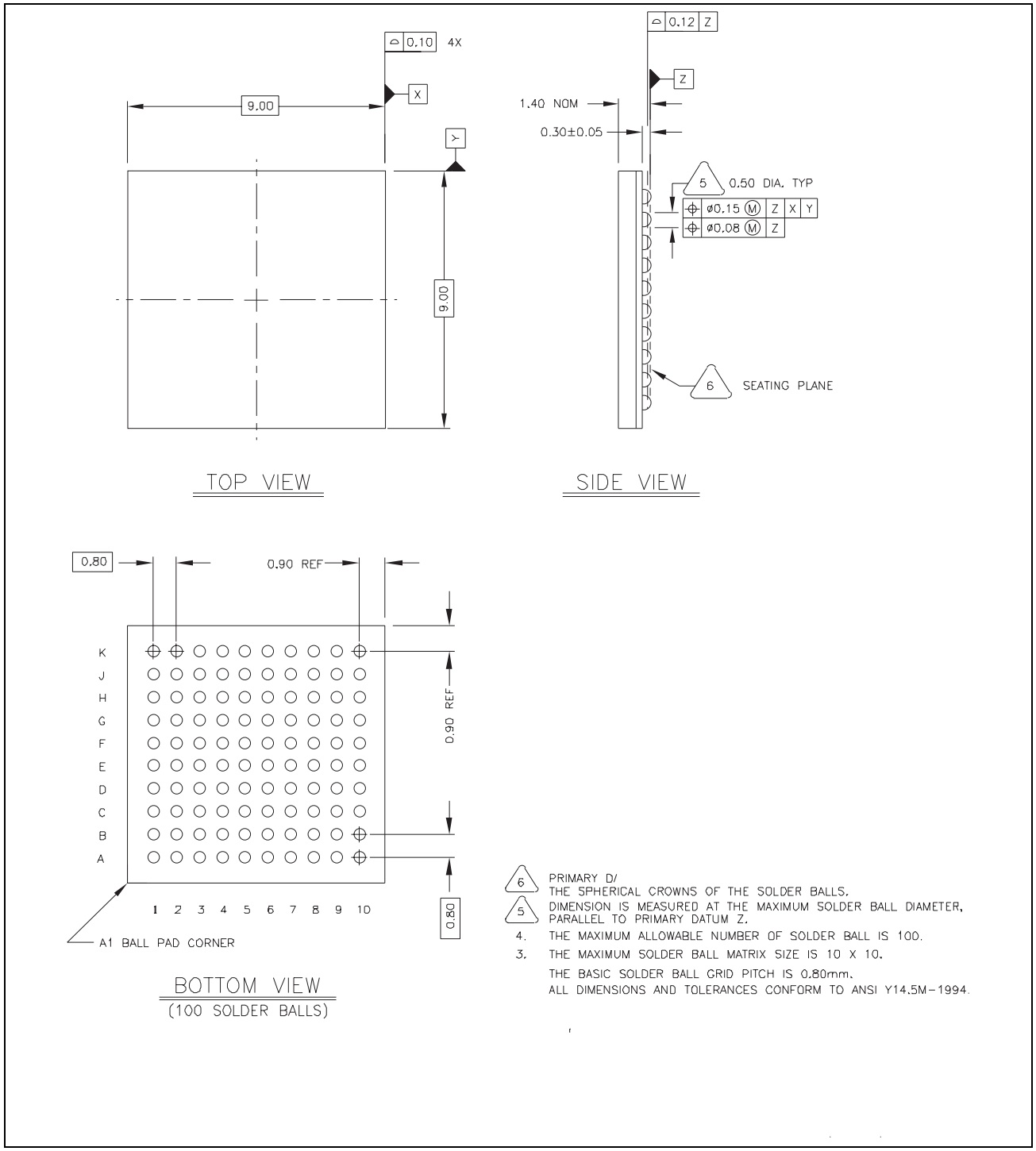


Figure 18: 100-Pin MQFP Package

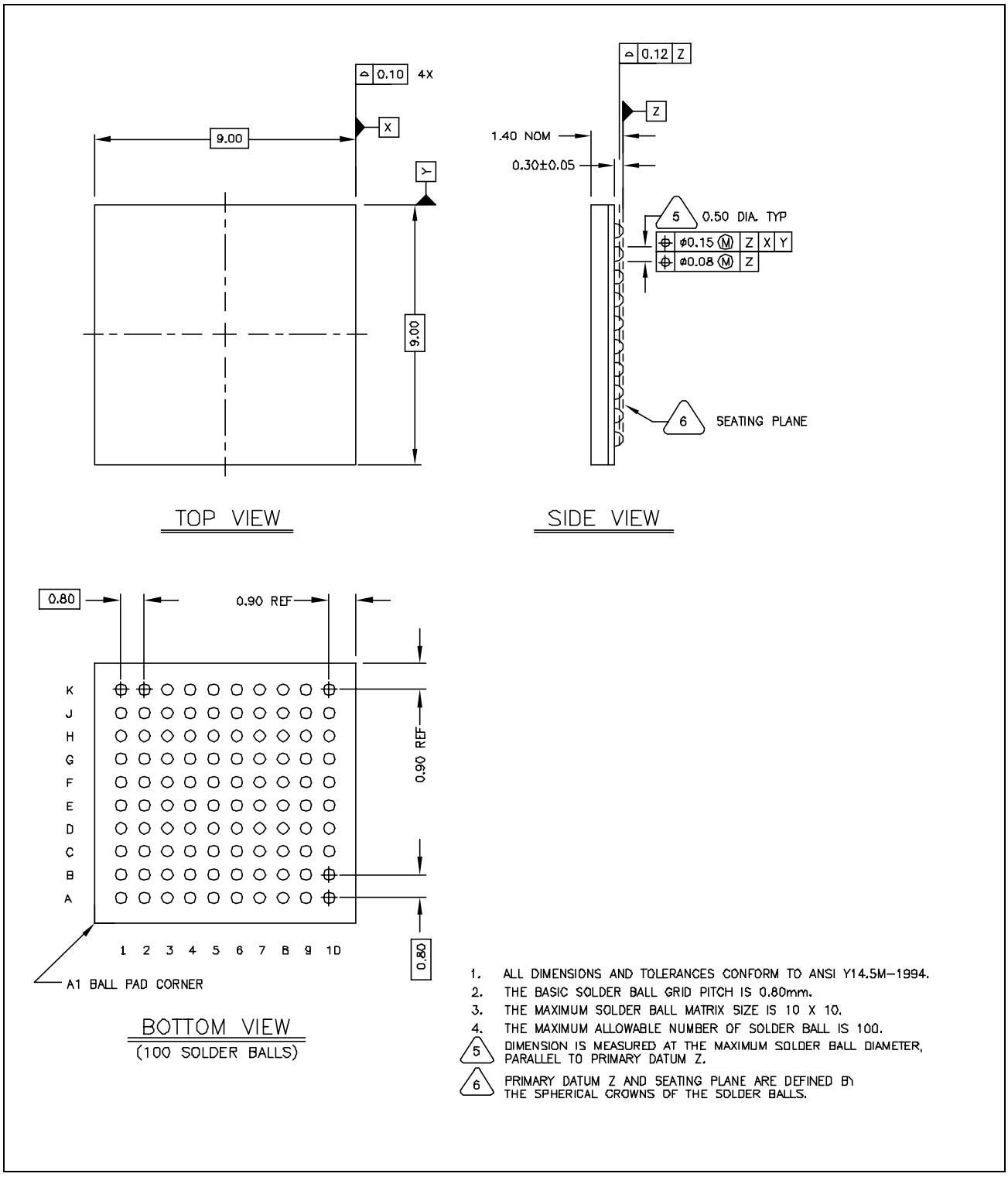


Figure 19: 100-Pin FBGA Package

Section 10: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM5222KQM	100-MQFP, 14 mm x 20 mm	-40° to 85° C -40° to 185° F
BCM5222KPF[a]	100-FBGA, 9 mm x 9 mm	-40° to 85° 5222-DS02-405-RC -40° to 185° F

a. Contact Broadcom sales department for availability.

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, CA 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710