RICOH

R5112S Series

42 V Input Ultra Low Supply Current VR with RESET

NO.EA-406-160420

OUTLINE

R5112S is an ultra-low supply current voltage regulator with a voltage detector featuring 200 mA output current and 42 V input voltage. This device consists of an Output Short-circuit Protection Circuit, an Overcurrent Protection Circuit, and a Thermal Shutdown Circuit in addition to the basic regulator circuits. The operating temperature range is between −40°C to 105°C, and the maximum input voltage is 42 V. The output voltages are internally fixed at either of the following: 1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 3.4 V, or 5.0 V. The output voltage accuracy is ±0.6%. The detector threshold accuracy of the voltage detector is ±0.6%. This device is offered in an 8-pin HSOP-8E package with high power dissipation.

FEATURES

● Input Voltage Range (Maximum Rating)	3.5 V to 42 V (50 V)
● Operating Temperature Range	−40°C to 105°C (Usable in high-temperature environment)
● Supply Current	Typ. 3.8 µA
● Standby Current	Typ. 0.1 µA
● Dropout Voltage	Typ. 0.6 V (I_{OUT} = 200 mA, V_{SET} = 5.0 V)
● Output Voltage Range	1.8 V / 2.5 V / 2.8 V / 3.0 V / 3.3 V / 3.4 V / 5.0 V *Contact Ricoh sales representatives for other voltages.
● Output Voltage Accuracy	±0.6% (Ta = 25°C)
● Output Voltage Temperature-Drift Coefficient	Typ. ±60 ppm/°C
● Detector Threshold Range	R5112Sxx1B: 1.6 V to 4.8 V R5112Sxx1D: 2.9 V to 4.8 V
● Detector Threshold Accuracy	±0.6% (Ta = 25°C)
● Detector Threshold Temperature Coefficient	Typ. ±60 ppm/°C
● Line Regulation	Typ. 0.01%/V (2.5 V ≤ V_{SET}: V_{SET} + 1 V ≤ V_{IN} ≤ 42 V)
● Built-in Output Short-circuit Protection Circuit	Typ. 80 mA
● Built-in Overcurrent Protection Circuit	Typ. 350 mA
● Built-in Thermal Shutdown Circuit	Thermal Shutdown Temperature: Typ. 170°C
● Ceramic capacitors are recommended to be used with this device	C_{OUT} = 0.1 µF or more
● Package	HSOP-8E

APPLICATIONS

- Power source for home appliances such as refrigerators, rice cookers, and electric hot-water pot.
- Power source for notebook PCs, digital TVs, cordless phones, and private LAN system.
- Power source for office equipment machines such as copiers, printers, facsimiles, scanners, and projectors.

SELECTION GUIDE

The set output voltage is user-selectable.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5112Sxx1∗-E2-FE	HSOP-8E	1,000 pcs	Yes	Yes

xx: Specify the set output voltage (V_{SET}) and the set detector threshold ($-V_{SET}$) by using serial numbers starting from 01.[1]

∗: Select the voltage detection type from the following
B: SENSE pin detection
D: VOUT pin detection

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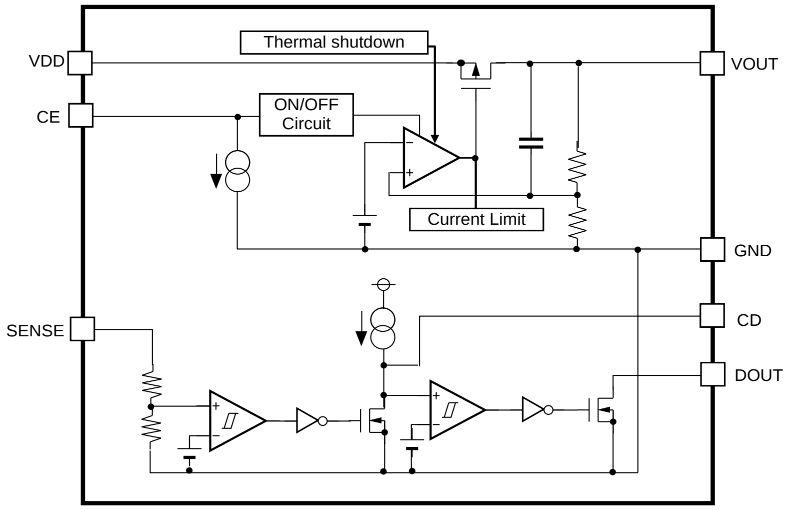
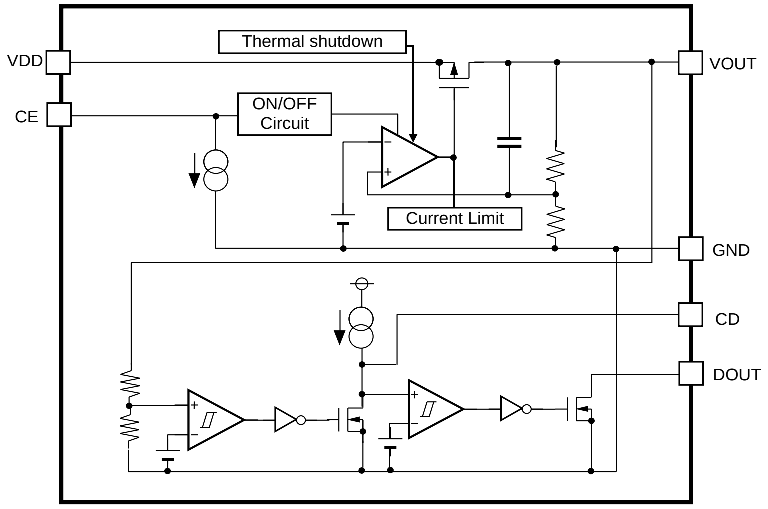
[1] The combinations of V_{SET} and $-V_{SET}$ are the following three conditions.
SENSE pin detection: V_{SET} = 3.3 V to 5.0 V, $-V_{SET}$ = 2.5 V to 5.0 V
SENSE pin detection: V_{SET} = 1.8 V to 3.2 V, $-V_{SET}$ = 1.6 V to 2.9 V
VOUT pin detection: V_{SET} = 3.3 V to 5.0 V, $-V_{SET}$ = 2.9 V to 5.0 V

BLOCK DIAGRAMS

R5112SxxxB
(SENSE Pin Detection)

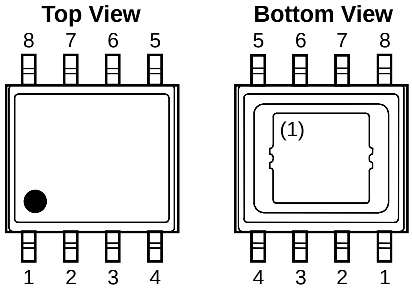


R5112SxxxD
(VOUT Pin Detection)



PIN DESCRIPTIONS

HSOP-8E



HSOP-8E (R5112SxxxB/D)

Pin No.	Symbol	Description
1	VDD	Input Pin
2	CE	Chip Enable Pin (Active-high)
3	NC	No Connection
4	DOUT(2)	VD Output Pin (Nch Open Drain)
5	CD	Pin for setting VD Release Output Delay Time (power-on reset time)
6	SENSE	VD Voltage SENSE Pin (R5112SxxxB)
	NC	No Connection (R5112SxxxD)
7	GND	Ground Pin
8	VOUT	Output Pin

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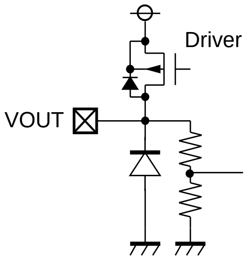
(1) The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). The tab is recommended to connect to the ground plane on the board. Otherwise it may be left floating.

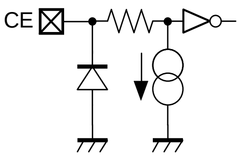
(2) DOUT pin should be pulled-up to an external voltage level.

PIN EQUIVALENT CIRCUIT DIAGRAMS

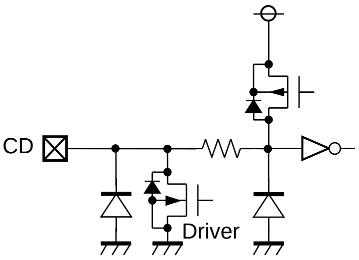
VOUT Pin



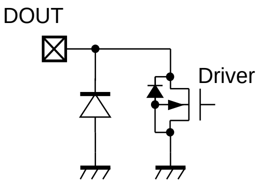
CE Pin



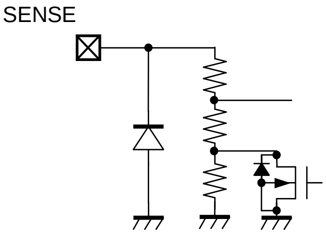
CD Pin



DOUT Pin



SENSE Pin



ABSOLUTE MAXIMUM RATINGS

Symbol	Item		Rating	Unit
V_{IN}	Input Voltage		−0.3 to 50	V
	Peak Input Voltage(1)		60	V
V_{CE}	Input Voltage (CE Pin)		−0.3 to 50	V
V_{OUT}	Output Voltage		-0.3 to $V_{IN} + 0.3 \leq 50$	V
V_{CD}	CD Pin Output Voltage		−0.3 to 7.0	V
V_{DOUT}	DOUT Pin Output Voltage		−0.3 to 7.0	V
V_{SENSE}	SENSE Pin Input Voltage		−0.3 to 7.0	V
P_D	Power Dissipation(2) (HSOP-8E)	Ultra High Wattage Land Pattern	2900	mW
Tj	Junction Temperature		−40 to 125	°C
Tstg	Storage Temperature		−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3.5 to 42	V
V_{CE}	Input Voltage (CE Pin)	0 to 42	V
V_{DOUT}	DOUT Pin Output Voltage	0 to 5.5	V
V_{SENSE}	SENSE Pin Input Voltage	0 to 5.5	V
Ta	Operating Temperature	−40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

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(1) Duration time: 200 ms

(2) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

$C_{IN} = C_{OUT} = 0.1\ \mu F$, $V_{IN} = 14\ V$, unless otherwise noted.
The specifications surrounded by $\boxed{}$ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

R5112Sxxxx-FE

For All (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	$I_{OUT} = 0$ mA		3.8	$\boxed{9.8}$	μA
Istandby	Standby Current	$V_{IN} = 42$ V, $V_{CE} = 0$ V		0.1	1.0	μA
I_{PD}	CE Pull-down Current			0.2	$\boxed{0.6}$	μA
V_{CEH}	CE Input Voltage "H"		$\boxed{2.2}$		$\boxed{42}$	V
V_{CEL}	CE Input Voltage "L"		0		$\boxed{1.0}$	V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

VR (Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	$V_{SET} + 1\ V \leq V_{IN} \leq 42\ V$ ($V_{SET} < 2.5\ V$: $V_{SET} + 1\ V = 3.5\ V$), $I_{OUT} = 1$ mA	Ta = 25°C	×0.994		×1.006	V
			−40°C ≤ Ta ≤ 105°C	$\boxed{\times 0.984}$		$\boxed{\times 1.016}$	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$V_{IN} = V_{SET} + 3.0$ V 1 mA ≤ I_{OUT} ≤ 200 mA		$\boxed{-10}$	0	$\boxed{40}$	mV
V_{DIF}	Dropout Voltage	$I_{OUT} = 200$ mA	$V_{SET} < 2.5$ V		1.6	$\boxed{2.5}$	V
			2.5 V ≤ V_{SET} < 3.3 V		1.2	$\boxed{2.2}$	
			3.3 V ≤ V_{SET} < 5.0 V		0.8	$\boxed{2.0}$	
			$V_{SET} = 5.0$ V		0.6	$\boxed{1.2}$	
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$V_{SET} + 1\ V \leq V_{IN} \leq 42\ V$ ($V_{SET} < 2.5\ V$: $V_{SET} + 1\ V = 3.5\ V$), $I_{OUT} = 1$ mA		$\boxed{-0.02}$	0.01	$\boxed{0.02}$	%/V
I_{LIM}	Output Current Limit	$V_{IN} = V_{SET} + 3.0$ V		$\boxed{220}$	350	$\boxed{420}$	mA
I_{SC}	Short current Limit	$V_{OUT} = 0$ V		$\boxed{60}$	80	$\boxed{110}$	mA
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature			170		°C
T_{TSR}	Thermal Shutdown Release Temperature	Junction Temperature			135		°C

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

C_{IN} = C_{OUT} = 0.1 µF, V_{IN} = 14 V, unless otherwise noted.

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 105°C.

VD

(Ta = 25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	V_{DD} = V_{OUT} (VOUT detection)	Ta = 25°C	×0.994		×1.006	V
			−40°C ≤ Ta ≤ 105°C	$\boxed{\times 0.984}$		$\boxed{\times 1.016}$	
V_{HYS}	Detector Threshold Hysteresis			$-V_{DET}$ $\boxed{\times 0.011}$	$-V_{DET}$ ×0.018	$-V_{DET}$ $\boxed{\times 0.025}$	V
tdelay	Release Output Delay Time (Power-on Reset)	C_D = 10 nF		$\boxed{3}$	6	$\boxed{15}$	ms
V_{DOUT}	D_{OUT} Pull-up Voltage					$\boxed{5.5}$	V
$I_{OUTDOUT}$	Nch. Output Current (D_{OUT} Output Pin)	V_{IN} = 3.5 V, V_{DOUT} = 0.1 V		$\boxed{1.0}$	2.6		mA
$I_{LEAKDOUT}$	Nch. Leakage Current (D_{OUT} Output Pin)	V_{DOUT} = 5.5 V				$\boxed{0.3}$	µA
R_{LCD}	C_D Pin Discharge Nch Tr.ON Resistance	V_{CE} = 0 V, V_{CD} = 0.1 V			12	$\boxed{30}$	kΩ
R_{SENSE}	SENSE Resistance			$\boxed{2}$		$\boxed{50}$	MΩ

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

Product-specific Electrical Characteristics

R5112SxxxB-FE

(Ta = 25°C)

Product Name	V_{OUT} [V]					V_{DET} [V]					V_{HYS} [V]	
	Ta = 25°C			−40°C ≤ Ta ≤ 105°C		Ta = 25°C			−40°C ≤ Ta ≤ 105°C			
	Min.	Typ.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Min.	Max.
R5112x011B	4.970	5.000	5.030	4.920	5.080	4.573	4.600	4.627	4.527	4.674	0.050	0.117
R5112x021B	1.790	1.800	1.810	1.772	1.829	1.590	1.600	1.610	1.574	1.626	0.017	0.041
R5112x031B	4.970	5.000	5.030	4.920	5.080	4.473	4.500	4.527	4.428	4.572	0.049	0.115
R5112x041B	4.970	5.000	5.030	4.920	5.080	4.374	4.400	4.426	4.330	4.470	0.048	0.112
R5112x051B	4.970	5.000	5.030	4.920	5.080	4.274	4.300	4.326	4.231	4.369	0.047	0.110
R5112x061B	4.970	5.000	5.030	4.920	5.080	4.175	4.200	4.225	4.133	4.267	0.045	0.107
R5112x071B	4.970	5.000	5.030	4.920	5.080	3.678	3.700	3.722	3.641	3.759	0.040	0.094
R5112x081B	3.281	3.300	3.319	3.248	3.353	2.982	3.000	3.018	2.952	3.048	0.032	0.077
R5112x091B	3.281	3.300	3.319	3.248	3.353	2.883	2.900	2.917	2.854	2.946	0.031	0.074
R5112x101B	3.281	3.300	3.319	3.248	3.353	2.783	2.800	2.817	2.755	2.845	0.030	0.071
R5112x111B	3.281	3.300	3.319	3.248	3.353	2.684	2.700	2.716	2.657	2.743	0.029	0.069
R5112x121B	4.970	5.000	5.030	4.920	5.080	4.075	4.100	4.125	4.034	4.166	0.044	0.105
R5112x131B	3.380	3.400	3.420	3.346	3.454	3.081	3.100	3.119	3.050	3.150	0.034	0.079
R5112x141B	3.281	3.300	3.319	3.248	3.353	3.081	3.100	3.119	3.050	3.150	0.034	0.079

R5112SxxxD-FE

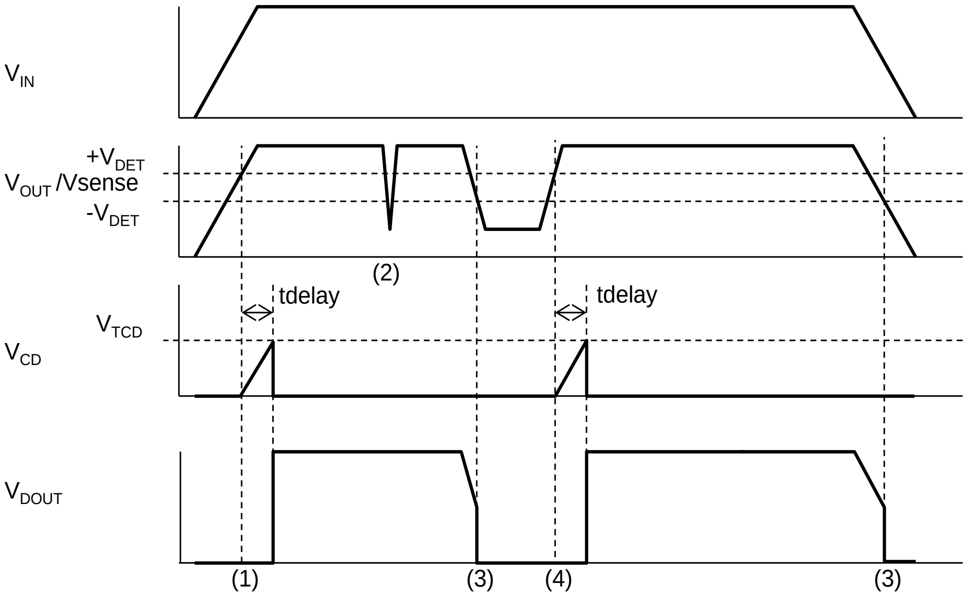
(Ta = 25°C)

Product Name	V_{OUT} [V]					V_{DET} [V]					V_{HYS} [V]	
	Ta = 25°C			−40°C ≤ Ta ≤ 105°C		Ta = 25°C			−40°C ≤ Ta ≤ 105°C			
	Min.	Typ.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Min.	Max.
R5112x011D	4.970	5.000	5.030	4.920	5.080	4.573	4.600	4.627	4.527	4.674	0.068	0.117
R5112x031D	4.970	5.000	5.030	4.920	5.080	4.473	4.500	4.527	4.428	4.572	0.066	0.115
R5112x041D	4.970	5.000	5.030	4.920	5.080	4.374	4.400	4.426	4.330	4.470	0.065	0.112
R5112x051D	4.970	5.000	5.030	4.920	5.080	4.274	4.300	4.326	4.231	4.369	0.063	0.110
R5112x061D	4.970	5.000	5.030	4.920	5.080	4.175	4.200	4.225	4.133	4.267	0.062	0.107
R5112x071D	4.970	5.000	5.030	4.920	5.080	3.678	3.700	3.722	3.641	3.759	0.054	0.094
R5112x081D	3.281	3.300	3.319	3.248	3.353	2.982	3.000	3.018	2.952	3.048	0.044	0.077
R5112x091D	3.281	3.300	3.319	3.248	3.353	2.883	2.900	2.917	2.854	2.946	0.043	0.074
R5112x121D	4.970	5.000	5.030	4.920	5.080	4.075	4.100	4.125	4.034	4.166	0.060	0.105
R5112x131D	3.380	3.400	3.420	3.346	3.454	3.081	3.100	3.119	3.050	3.150	0.046	0.079
R5112x141D	3.281	3.300	3.319	3.248	3.353	3.081	3.100	3.119	3.050	3.150	0.046	0.079

THEORY OF OPERATION

Timing Chart

R5112SxxxB/D Voltage Detector



R5112SxxxB/D VD Timing Chart

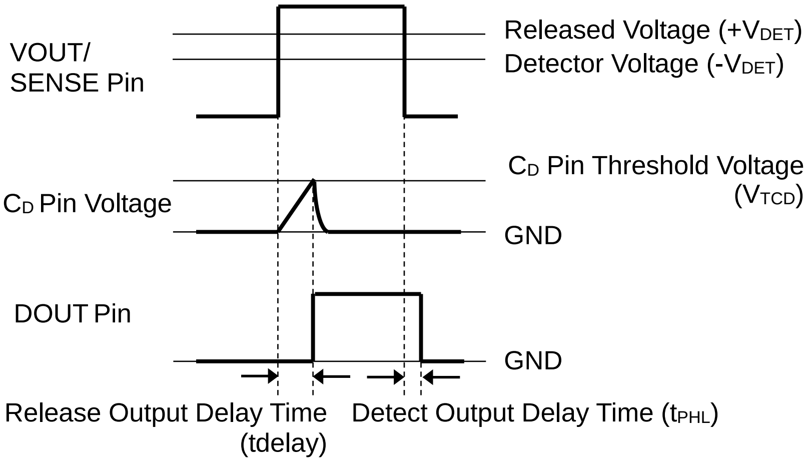
(1) When the V_{OUT} pin voltage (V_{OUT})/SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{DET}$), the D_{OUT} pin voltage (V_{DOUT}) becomes “H” after the release output delay time (tdelay).

(2) When the detect output delay time is 25 µs (Typ.) or less even if V_{OUT}/V_{SENSE} becomes lower than the detector threshold ($-V_{DET}$), the voltage detector (VD) does not go into the detecting state.

(3) When V_{OUT}/V_{SENSE} becomes lower than $-V_{DET}$, V_{DOUT} becomes "L" after the detect output delay time (t_{PHL}, Typ. 25 µs) and the VD goes into the detecting state.

(4) When V_{OUT}/V_{SENSE} becomes more than $+V_{DET}$, V_{DOUT} becomes "H" after the release output delay time (V_{TCD} = Typ. 0.73 V).

Delay Operation and Released Output Delay Time (tdelay)



Released Output Delay Timing Diagram

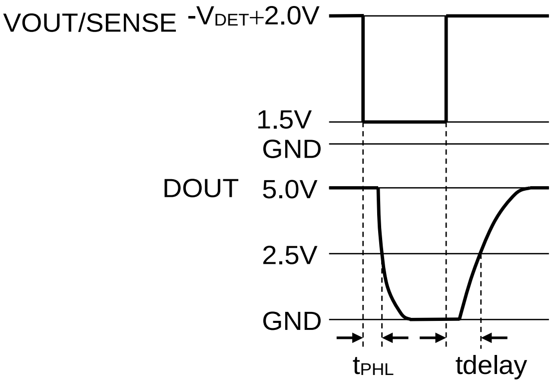
When the operating voltage higher than the released voltage is applied to VOUT pin (R5112SxxxD) or SENSE pin (R5112SxxxB), charge to an external capacitor starts, then C_D pin voltage (V_{CD}) increases. DOUT pin (R5112SxxxB/D) maintains the released output until V_{CD} reaches the threshold voltage of the release output delay pin (V_{TCD}). And when V_{CD} is over V_{TCD}, DOUT pin is inverted from “L” to “H”. That is, the charged external capacitor starts discharging.
When the operating voltage lower than the detector threshold is applied to VOUT pin/SENSE pin, the detect output delay time, which is the time until the output voltage is inverted from “H” to “L”, remains constant independent of the external capacitor.

Released Output Delay Time

Released Output Delay Time (tdelay) is determined by the following formula. C_D (F) represents capacitance of the external capacitor

$$\text{tdelay (s)} = 0.73 \times C_D \text{ (F)} / (1.2 \times 10^{-6})$$

Use 100 pF or higher C_D when allowing this device to detect VOUT/SENSE pin decreasing slower than 0.1 V/s.
Released Output Delay Time indicates the time between the instance when VOUT pin (R5112SxxxD) or SENSE pin (R5112SxxxB) shifts from “1.5 V” to “$-V_{DET}$ + 2.0 V” by the application of a pulse voltage and the instance when the output voltage reaches 2.5 V after pulled up DOUT pin (R5112SxxxB/D) to 5.0 V with a resistor of 100 kΩ.



Voltage Setting (R5112SxxxB/D)

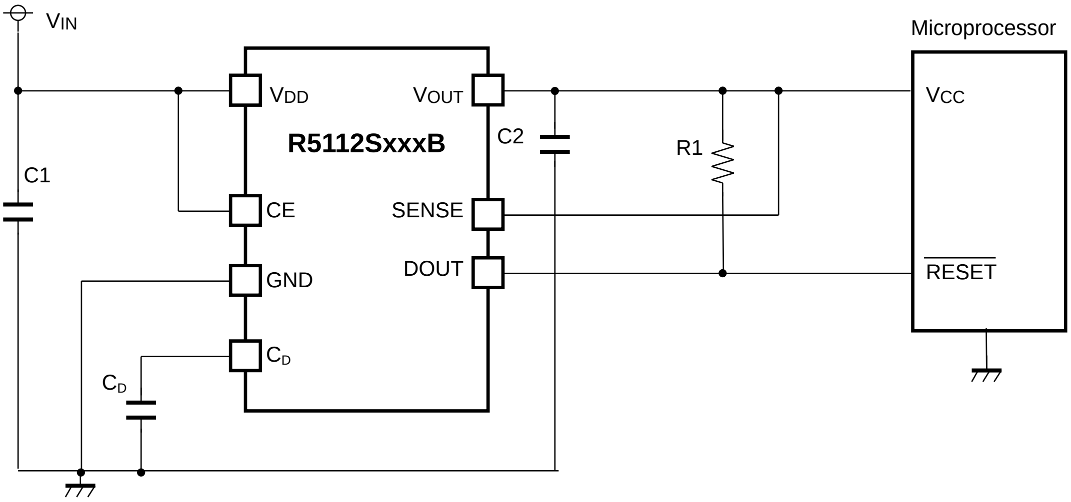
VD detects the drop of the VR output voltage (V_{OUT}). When the VD release voltage ($+V_{DET}$) is set to a voltage above the VR output voltage, the reset signal of VD is not released even if VD monitors the VR output voltage returns to the normal value after detecting the drop of VR. To prevent this issue, the following condition is required between V_{OUT} and $+V_{DET}$.

(VR Set Output Voltage) x 0.984 − 40 mV > (VD Set Detector Threshold) x 1.016 x 1.025

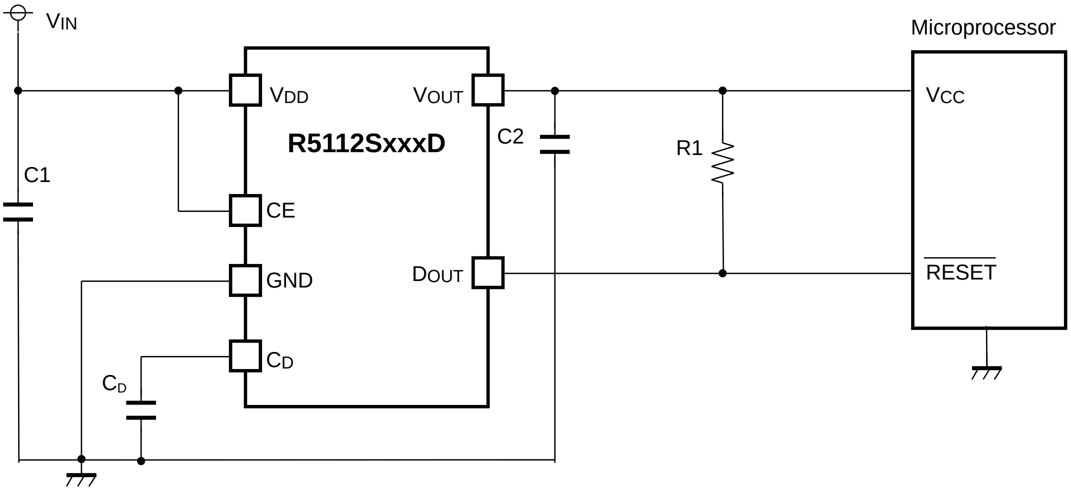
When using a device without the above conditions of V_{OUT} and $+V_{DET}$, careful consideration must be given to the system operation before use.

APPLICATION INFORMATION

TYPICAL APPLICATIONS



R5112SxxxB Typical Applications



R5112SxxxD Typical Applications

Recommended Components

Symbol	Description
C1 (C_{IN})	Ceramic Capacitor, 0.1 µF or more, 50V Rated Voltage, CGA3E3X8R1H104K080AB, TDK
C2 (C_{OUT})	Ceramic Capacitor, 0.1 µF or more, 50V Rated Voltage, CGA3E3X8R1H104K080AB, TDK
C_D	A capacitor corresponding to setting for Release Output Delay Time is required. Refer to *Delay Operation and Released Output Delay Time (tdelay)* in *THEORY OF OPERATION* for details.
R1	A resistor is required to set with consideration of the output current and the leakage current. Refer to *ELECTRICAL CHARACTERISTICS* for details.

TECHNICAL NOTES

Phase Compensation

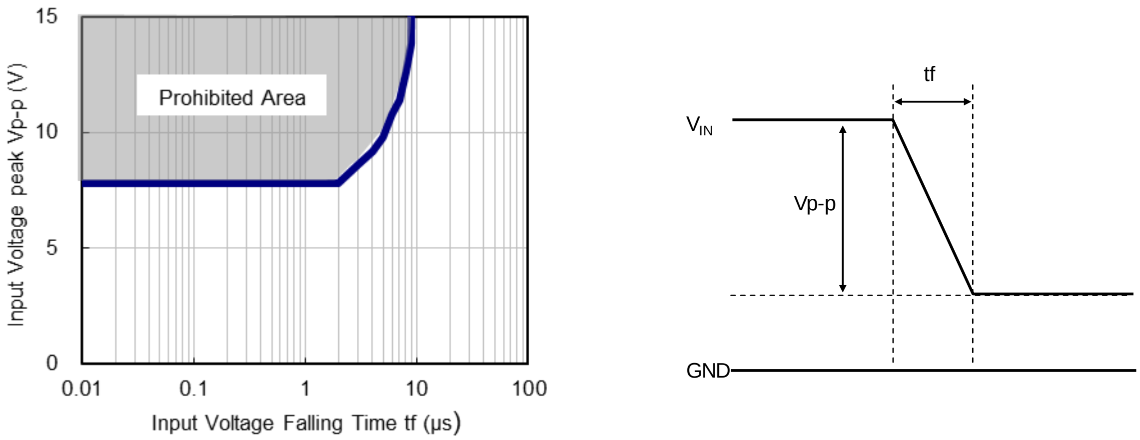
In the R5112S, phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, be sure to use 0.1 µF or more of a capacitor (C2).
In case of using a tantalum type capacitor and the ESR (Equivalent Series Resistance) value of the capacitor is large, the output might be unstable. Evaluate the circuit including consideration of frequency characteristics.

PCB Layout

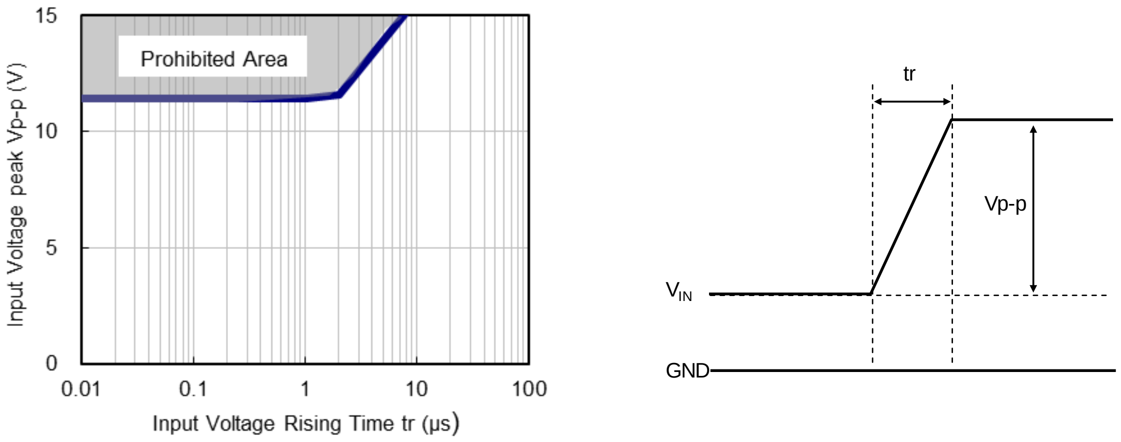
Ensure the VDD and GND lines are sufficiently robust. If their impedance is too high, noise pickup or unstable operation may result. Connect 0.1 µF or more of the capacitor C1 between the VDD and GND, and as close as possible to the pins. In addition, connect the capacitor C2 between VOUT and GND, and as close as possible to the pins.

Prohibited Area of the Input Voltage Variation

When the input voltage is steeply changed in the following prohibited area, the device may fail to detect or fail to release.



Variation Prohibited Area at Input Voltage (V_{IN}) Falling



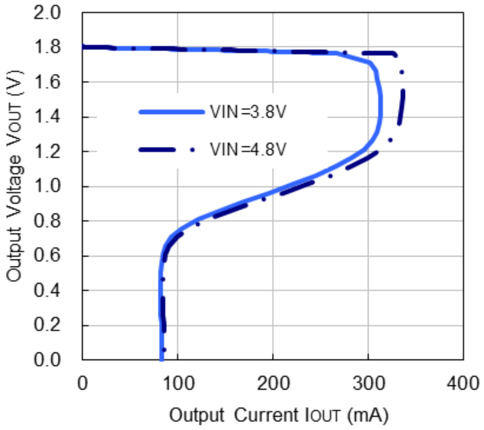
Variation Prohibited Area at Input Voltage (V_{IN}) Rising

TYPICAL CHARACTERISTICS

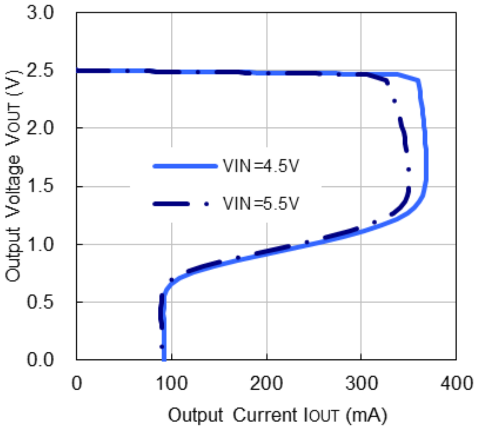
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current (Ta = 25°C)

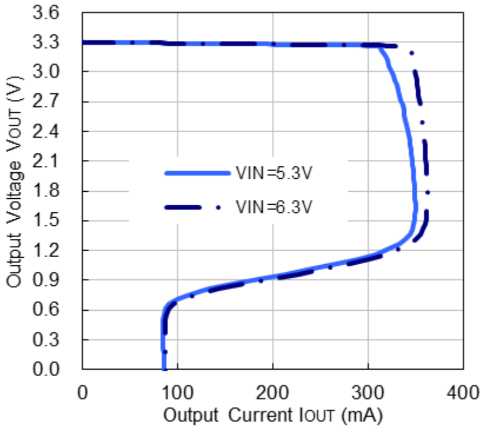
V_{SET} = 1.8 V



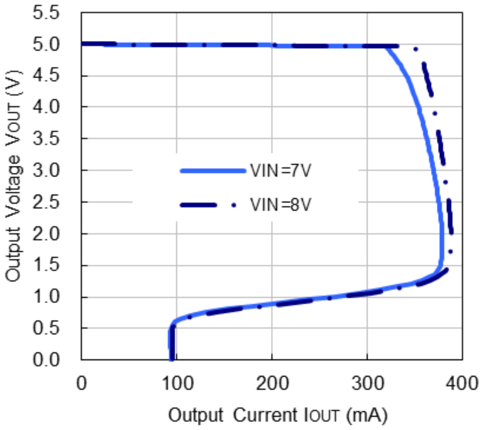
V_{SET} = 2.5 V



V_{SET} = 3.3 V

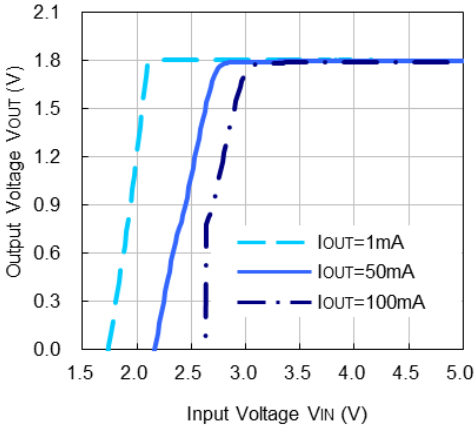


V_{SET} = 5.0 V

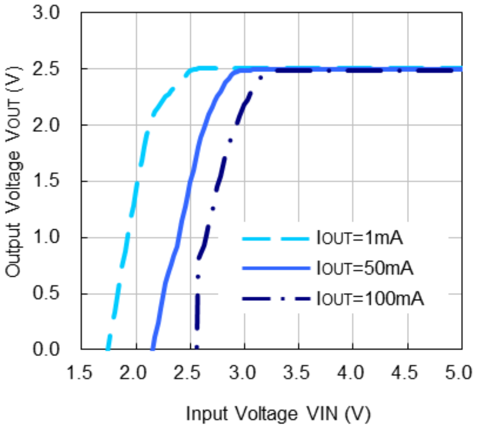


2) Output Voltage vs. Input Voltage (Ta = 25°C)

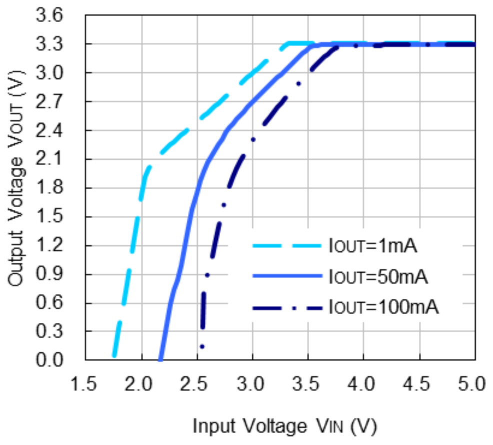
V_{SET} = 1.8 V



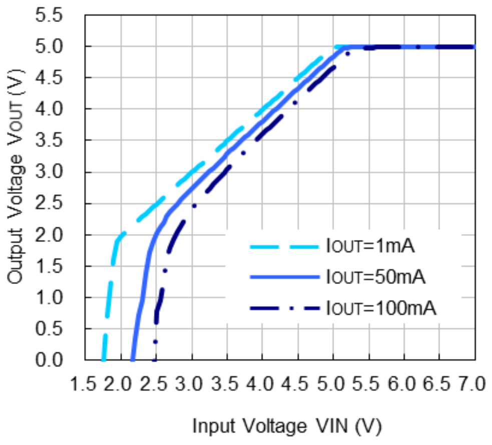
V_{SET} = 2.5 V



V_{SET} = 3.3 V

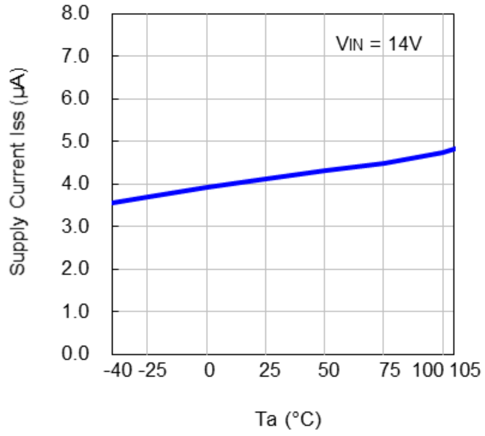


V_{SET} = 5.0 V

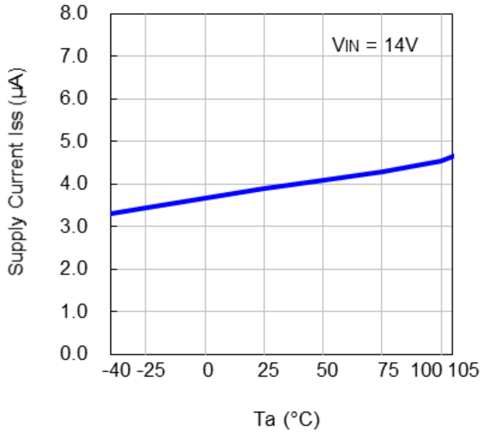


3) Supply Current vs. Temperature

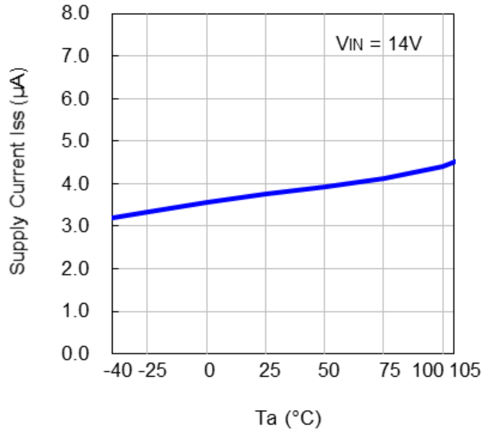
V_{SET} = 1.8 V



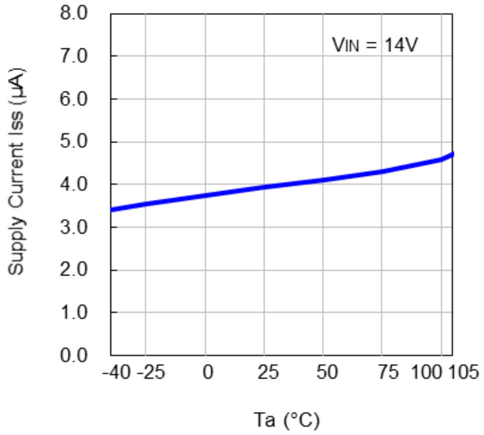
V_{SET} = 2.5 V



V_{SET} = 3.3 V

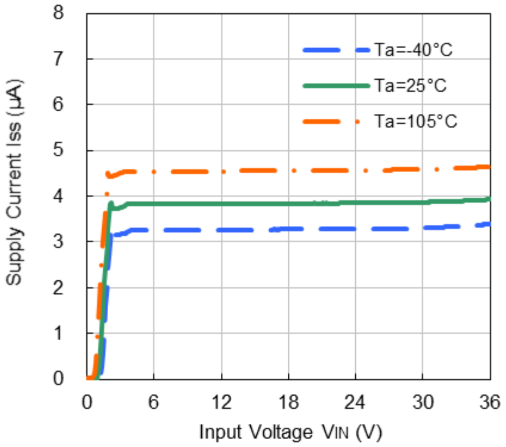


V_{SET} = 5.0 V

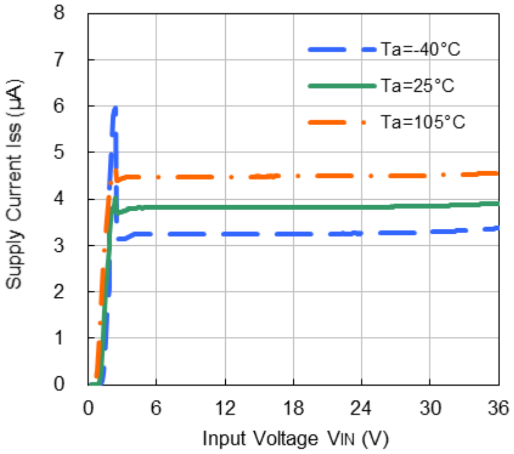


4) Supply Current vs. Input Voltage

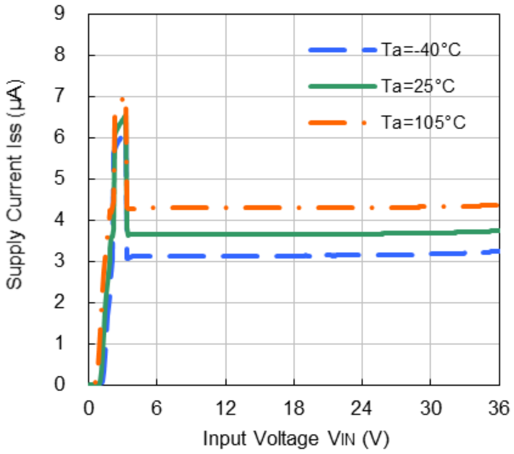
$V_{SET} = 1.8$ V



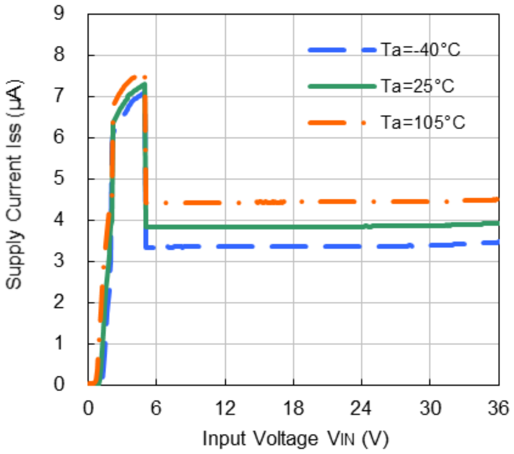
$V_{SET} = 2.5$ V



$V_{SET} = 3.3$ V

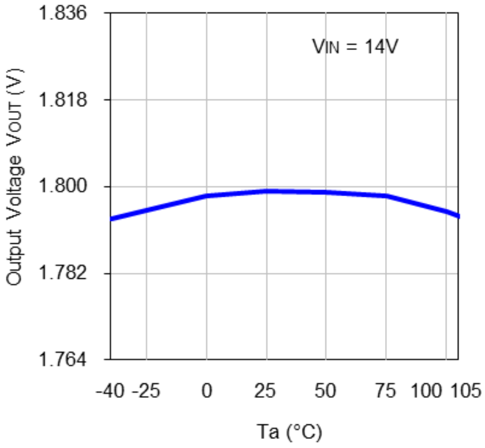


$V_{SET} = 5.0$ V

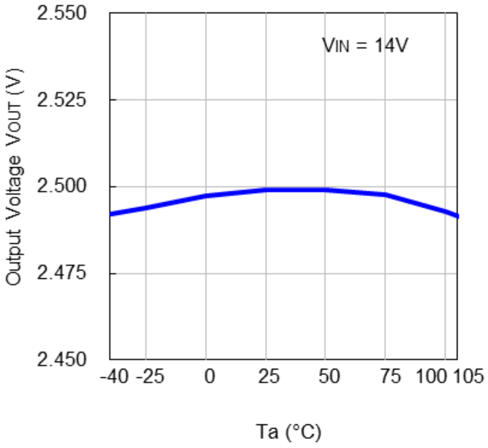


5) Output Voltage vs. Temperature

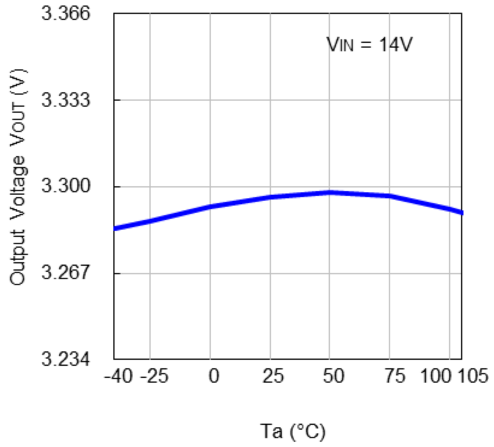
$V_{SET} = 1.8$ V



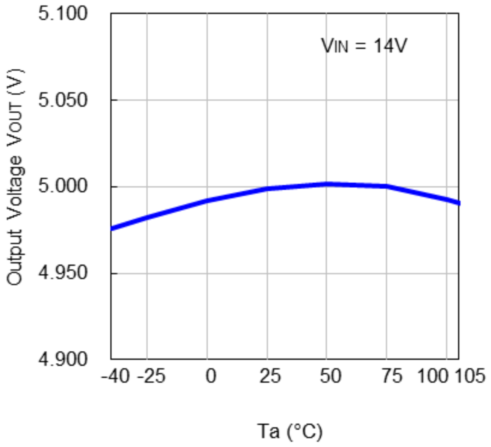
$V_{SET} = 2.5$ V



V_{SET} = 3.3 V

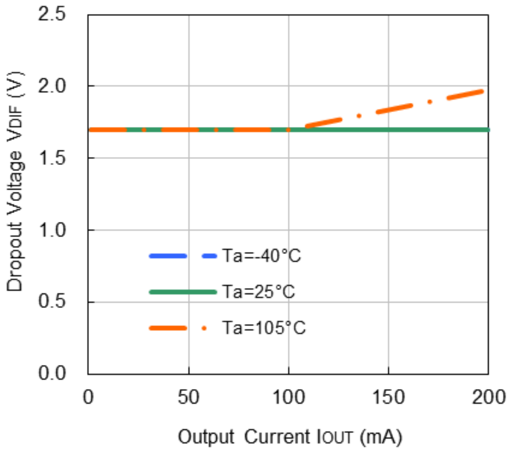


V_{SET} = 5.0 V

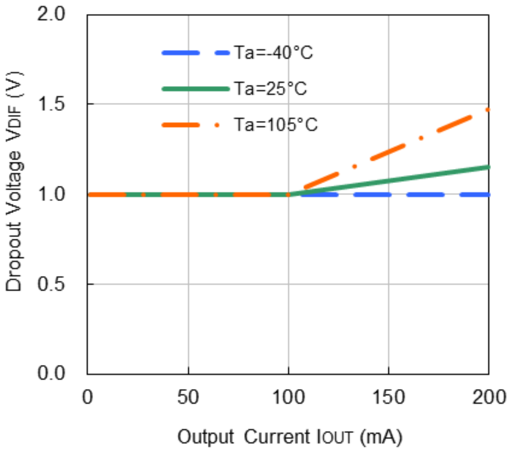


6) Dropout Voltage vs. Output Current

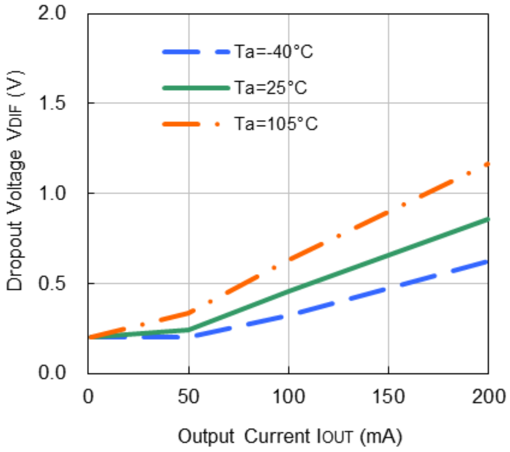
V_{SET} = 1.8 V



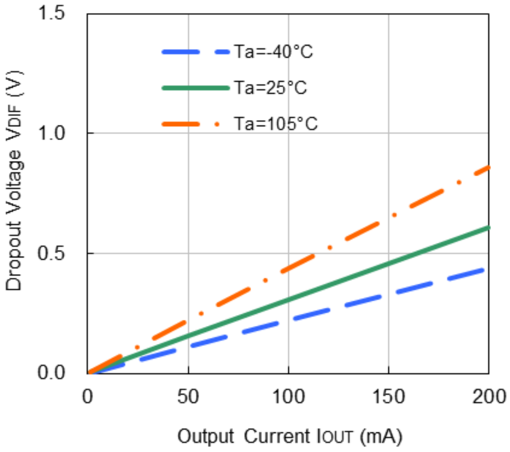
V_{SET} = 2.5 V



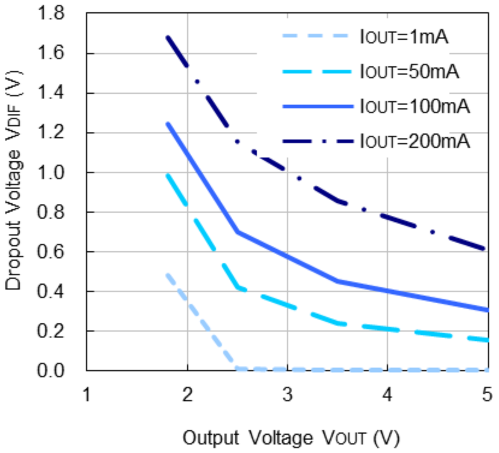
V_{SET} = 3.3 V



V_{SET} = 5.0 V

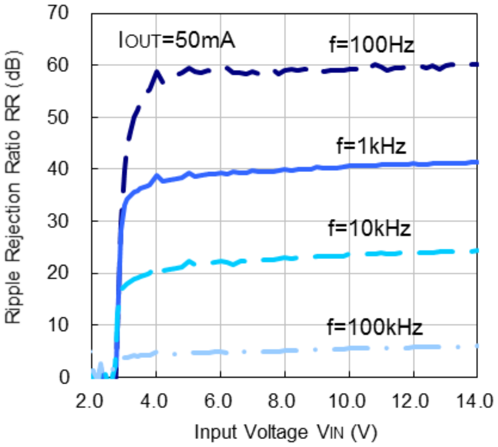


7) Dropout Voltage vs. Output Voltage (Ta = 25°C)

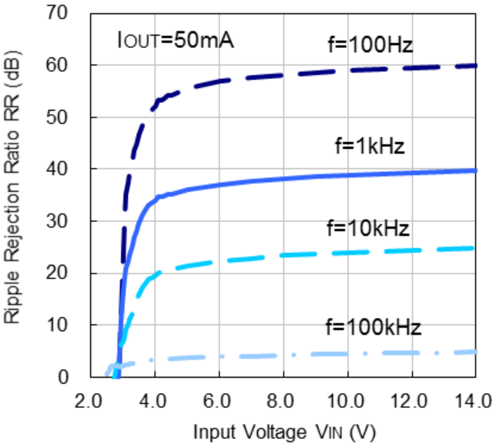


8) Ripple Rejection vs. Input Voltage (Ta = 25°C, Ripple = 0.2 Vpp)

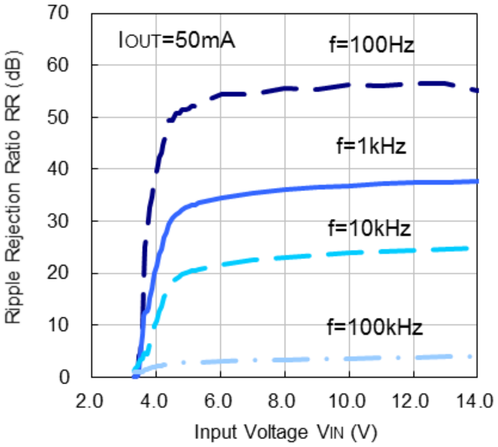
V_{SET} = 1.8 V



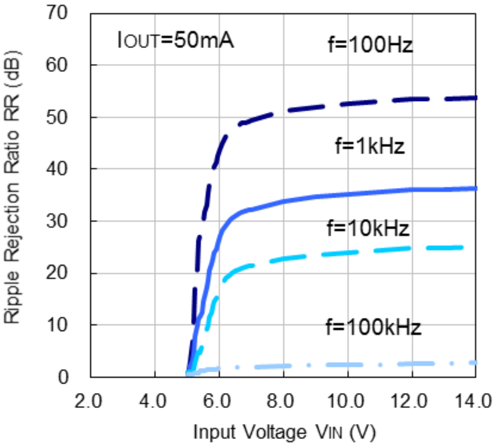
V_{SET} = 2.5 V



V_{SET} = 3.3 V

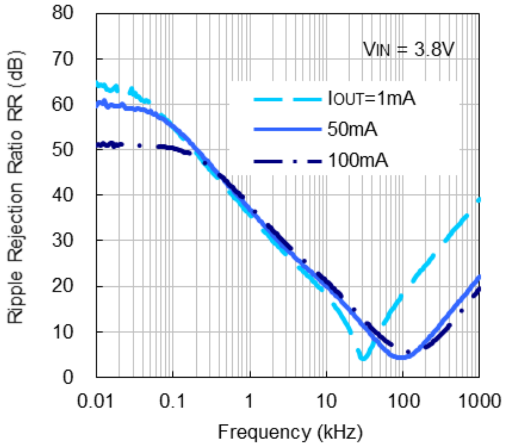


V_{SET} = 5.0 V

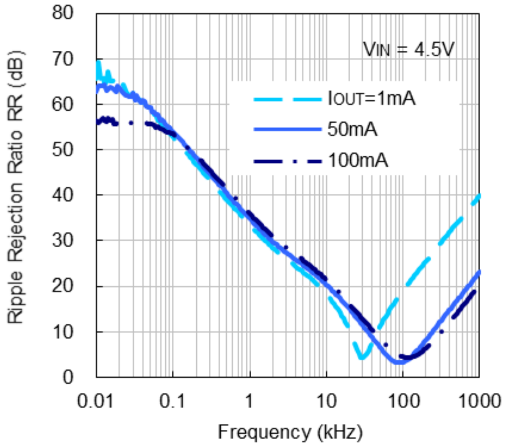


9) Ripple Rejection vs. Frequency (Ta = 25°C, Ripple = 0.2 Vpp)

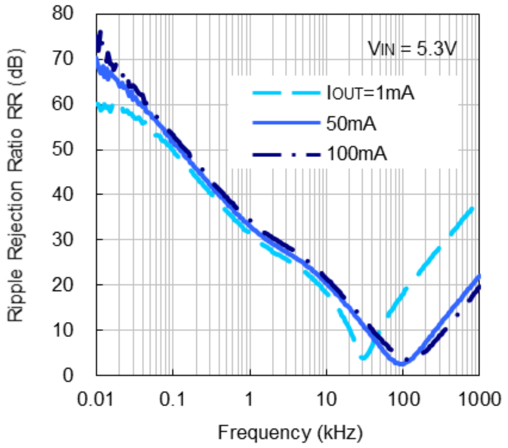
V_{SET} = 1.8 V



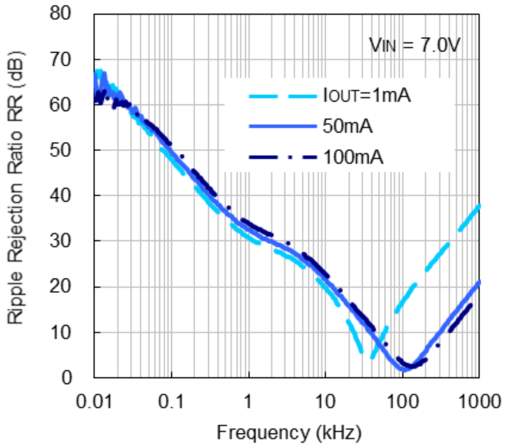
V_{SET} = 2.5 V



V_{SET} = 3.3 V

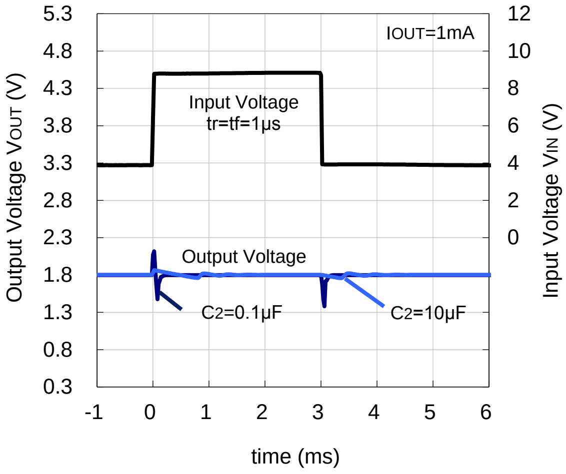


V_{SET} =5.0 V

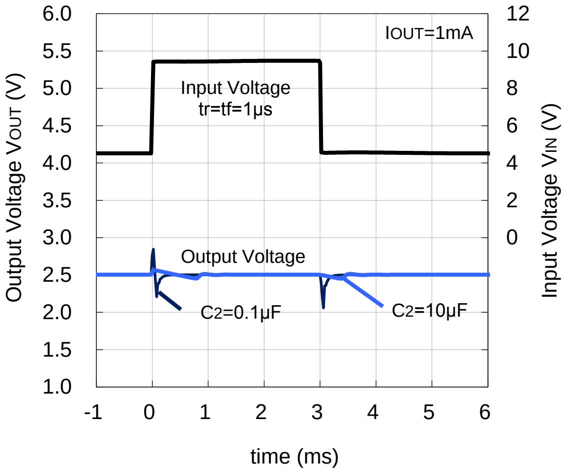


10) Input Transient Response (Ta = 25°C)

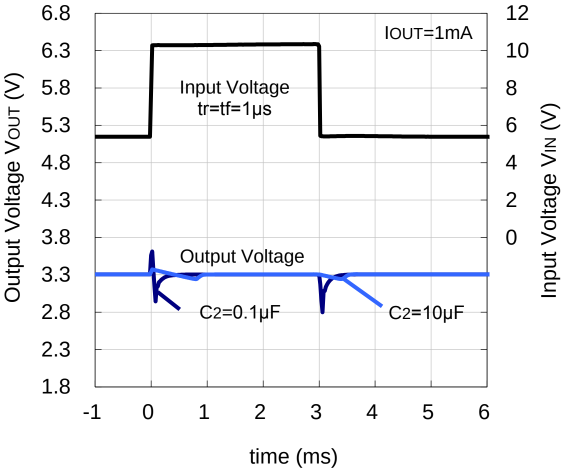
V_{SET} = 1.8 V



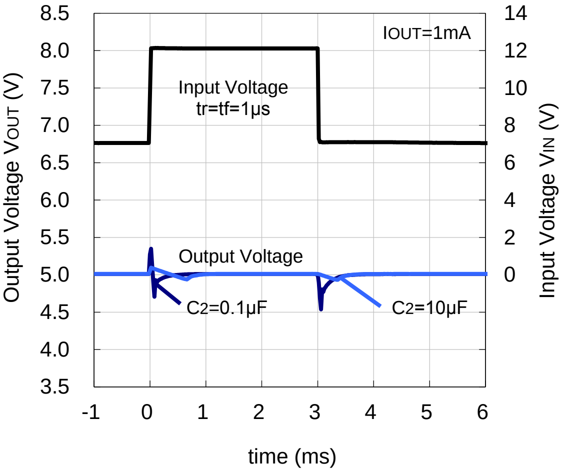
V_{SET} = 2.5 V



V_{SET} = 3.3 V

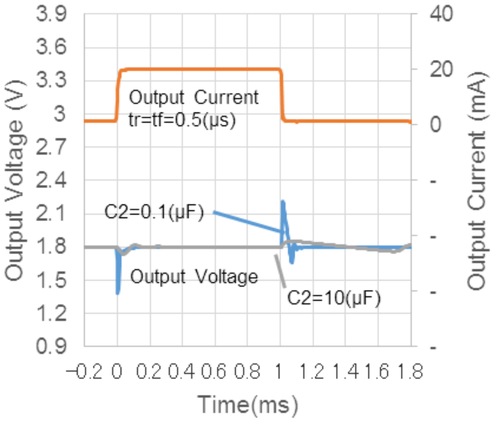


V_{SET} = 5.0 V

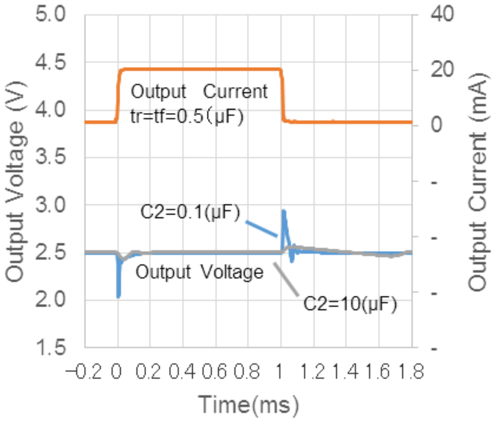


11) Load Transient Response (Ta = 25°C)

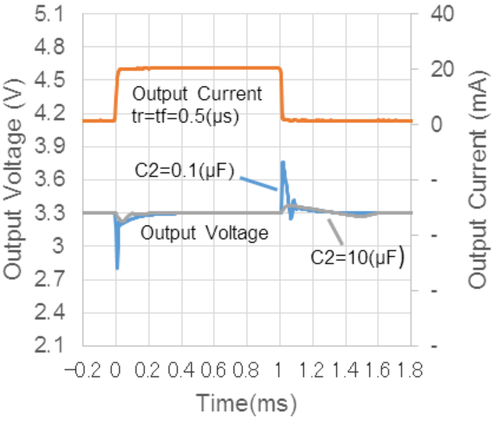
V_{SET} = 1.8 V



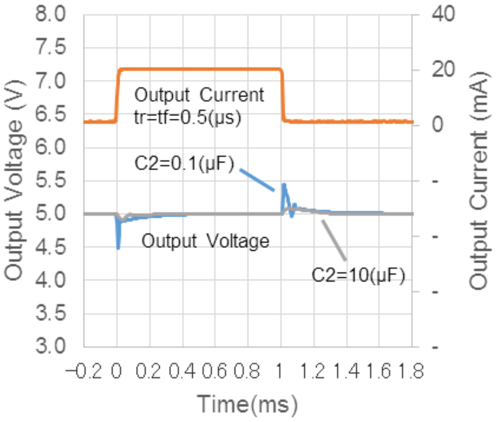
V_{SET} = 2.5 V



V_{SET} = 3.3 V

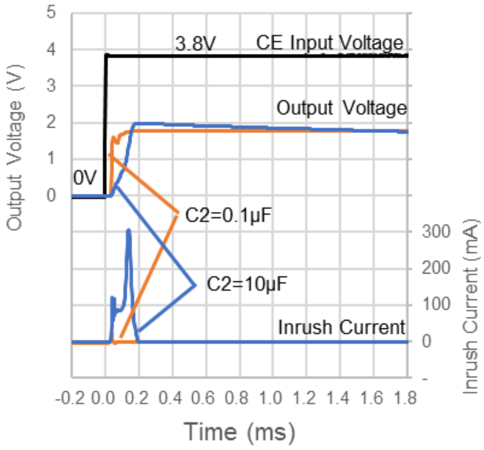


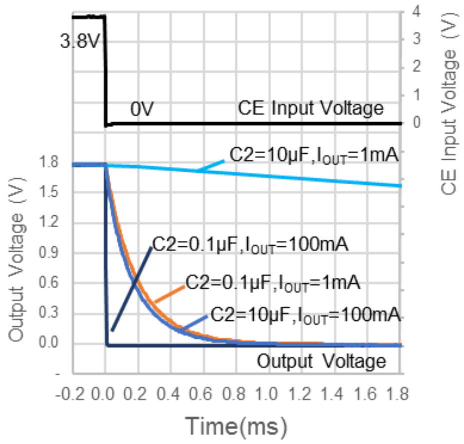
V_{SET} = 5.0 V



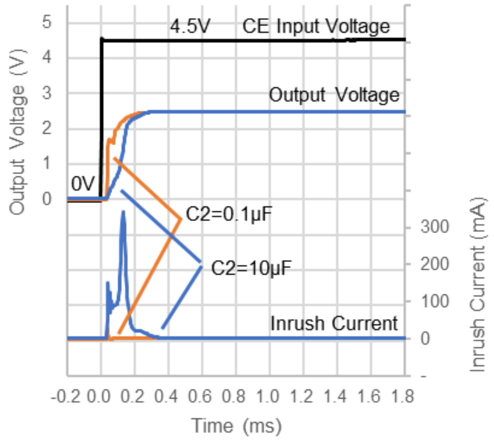
12) CE Transient Response (Ta = 25°C)

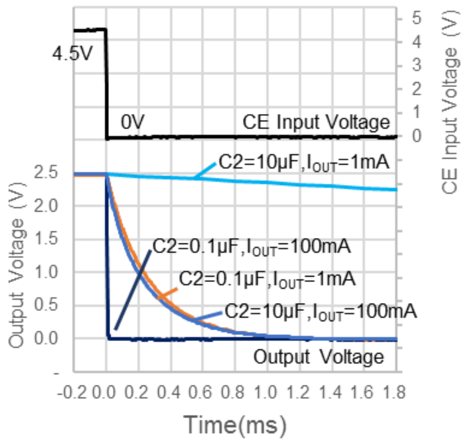
V_{SET} = 1.8 V



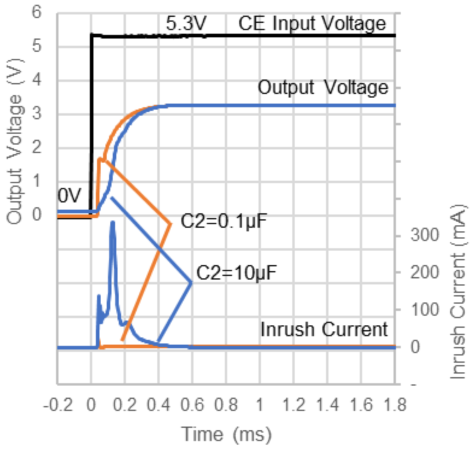


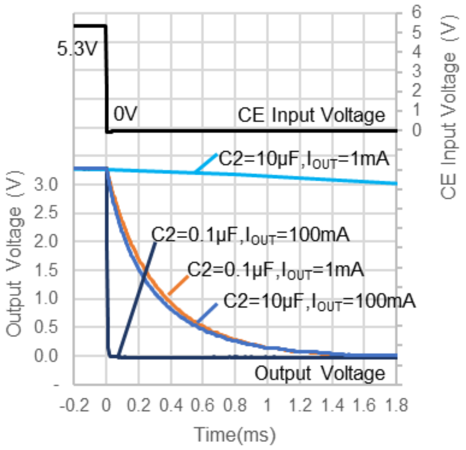
V_{SET} = 2.5 V



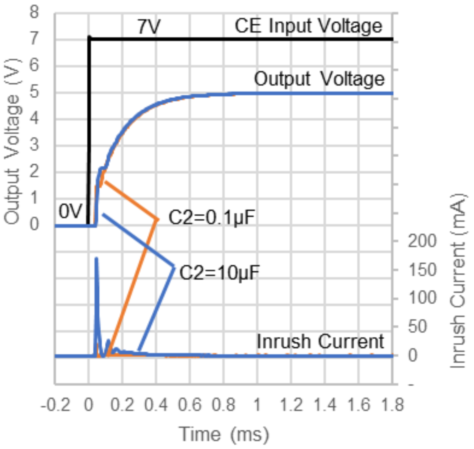


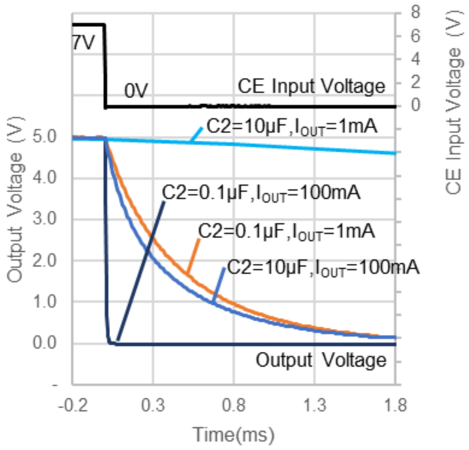
V_{SET} = 3.3 V





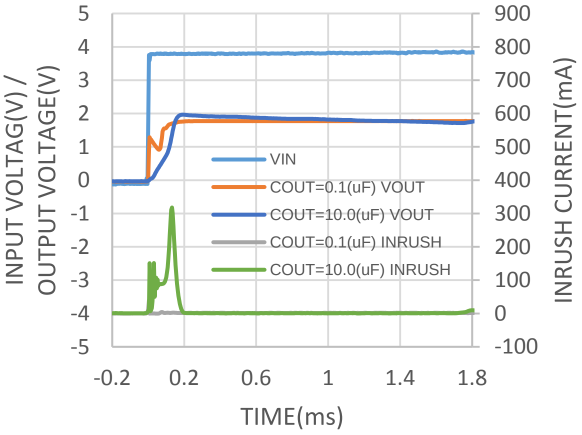
V_{SET} = 5.0 V


7V
CE Input Voltage
Output Voltage
0V
C2=0.1μF
C2=10μF
Inrush Current
Output Voltage (V)
8
7
6
5
4
3
2
1
0
Inrush Current (mA)
200
150
100
50
0
-0.2
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
Time (ms)

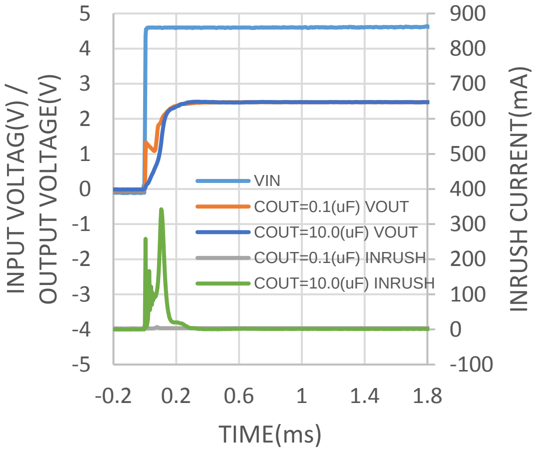

7V
0V
CE Input Voltage
C2=10μF,I_{OUT}=1mA
C2=0.1μF,I_{OUT}=100mA
C2=0.1μF,I_{OUT}=1mA
C2=10μF,I_{OUT}=100mA
Output Voltage
Output Voltage (V)
5.0
4.0
3.0
2.0
1.0
0.0
CE Input Voltage (V)
8
6
4
2
0
-0.2
0.3
0.8
1.3
1.8
Time(ms)

13) Power-on Transient Response (Ta = 25°C)

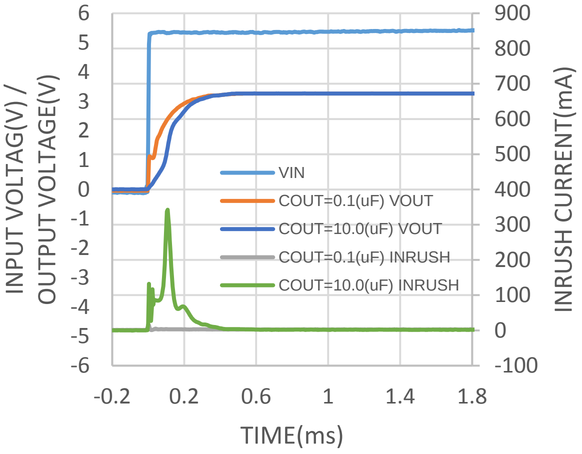
V_{SET} = 1.8 V



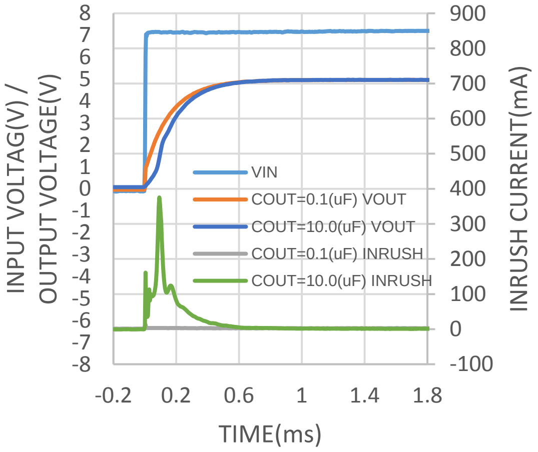
V_{SET} = 2.5 V



V_{SET} = 3.3 V

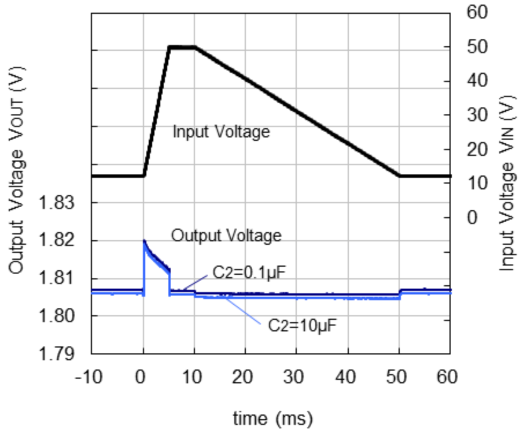


V_{SET} = 5.0 V

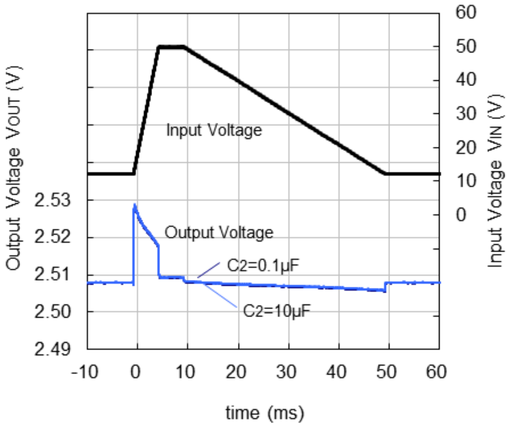


14) Load Dump (Ta = 25°C)

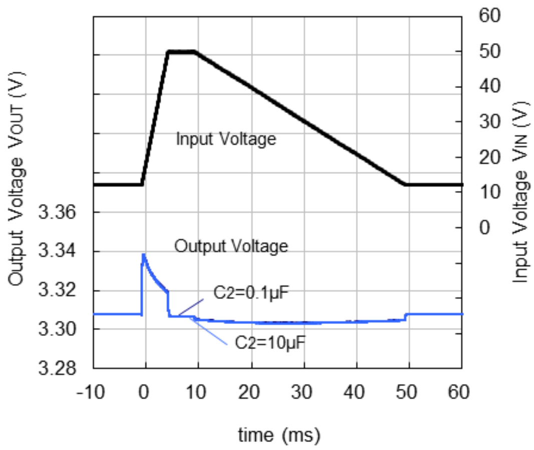
V_{SET} = 1.8 V



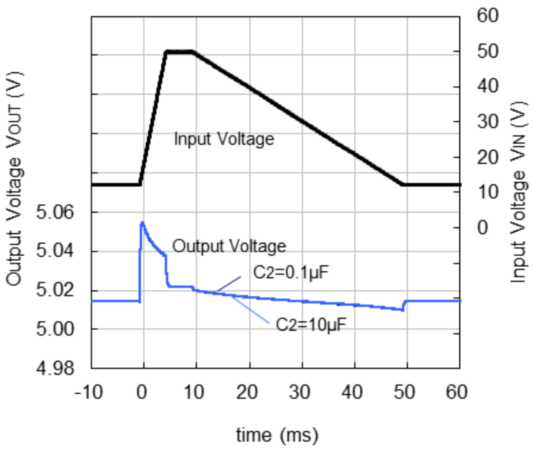
V_{SET} = 2.5 V



V_{SET} = 3.3 V

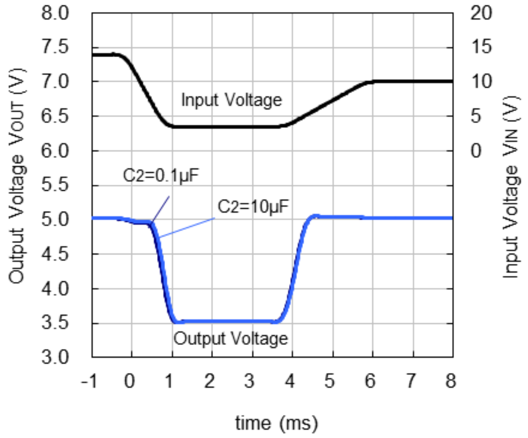


V_{SET} = 5.0 V



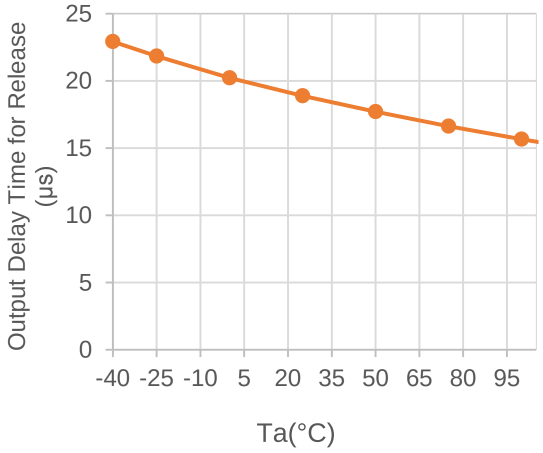
15) Cranking (Ta = 25°C)

V_{SET} = 5.0 V

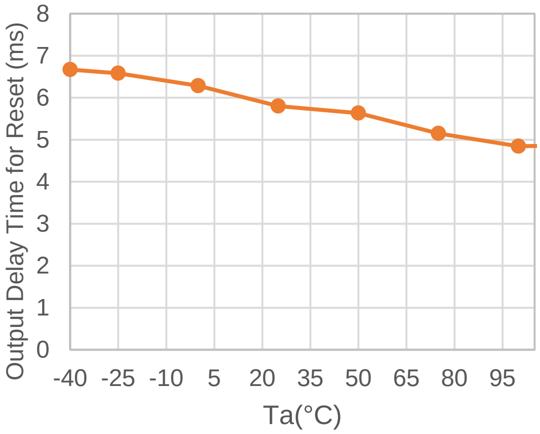


16) Detect/Release Delay Time vs. Temperature

Detect Output Delay Time



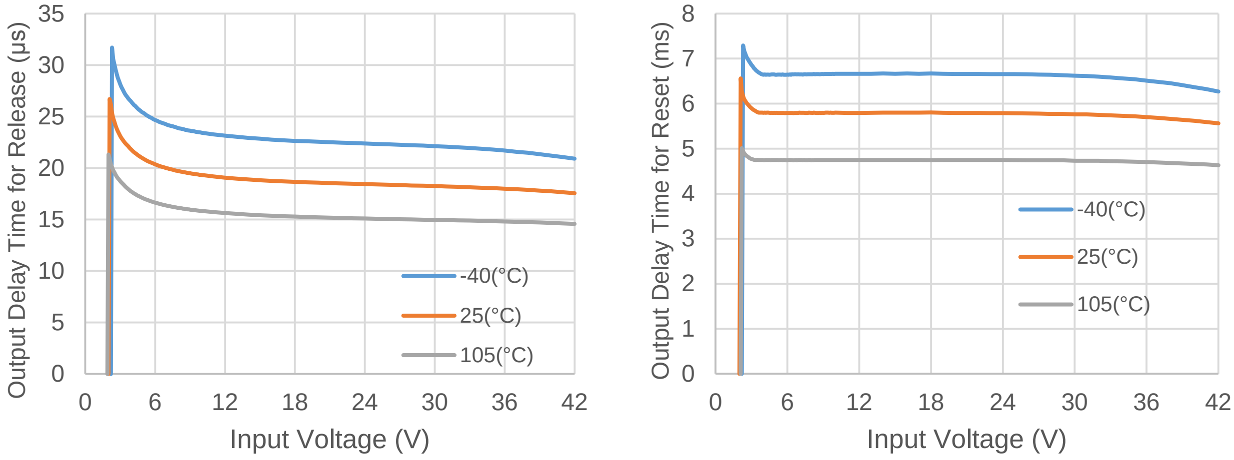
Release Output Delay Time



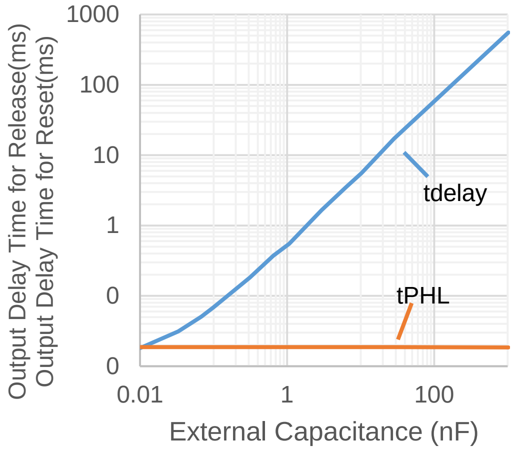
17) Detect/Release Delay Time vs. Input Voltage

Detect Output Delay Time

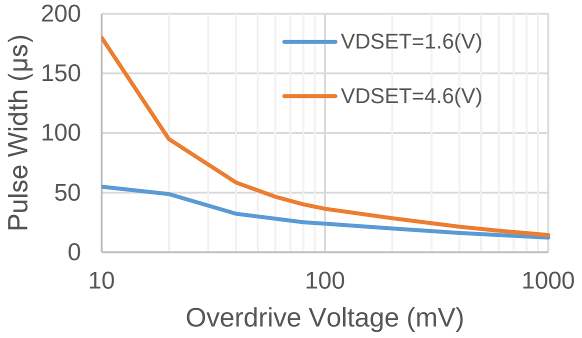
Release Output Delay Time



18) Detect (Release) Delay Time vs. External Capacitance for CD Pin (Ta = 25°C)

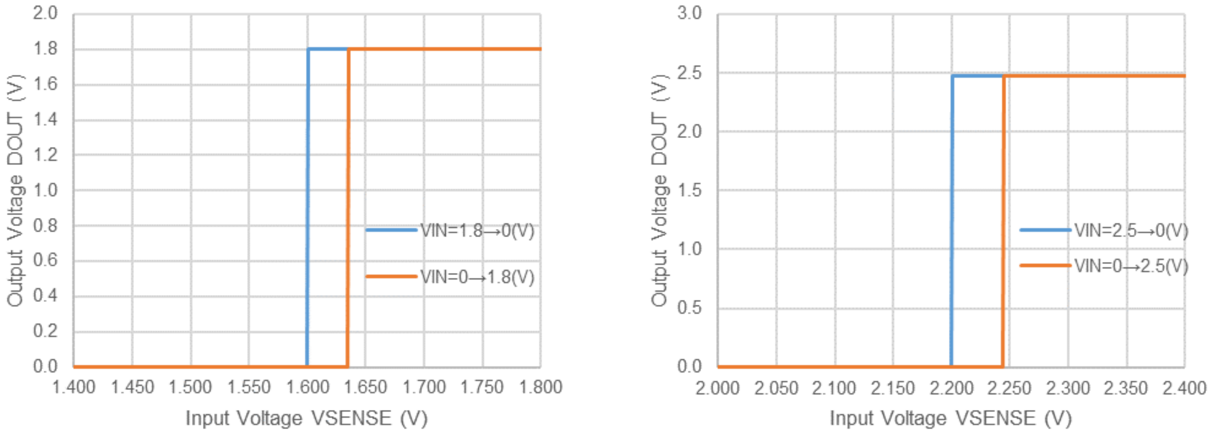


19) Pulse Width vs. Overdrive Voltage (Ta = 25°C)

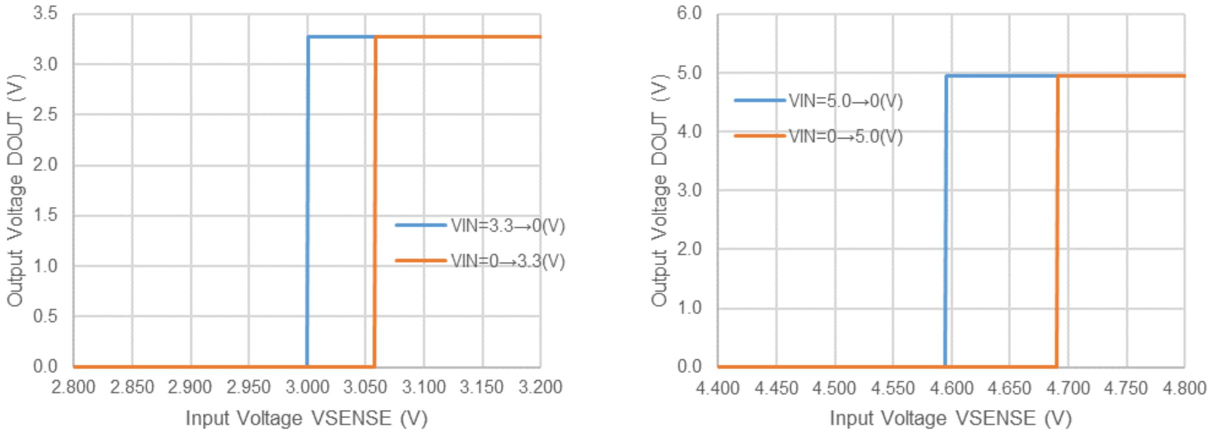


20) D_{OUT} Pin Voltage vs. SENSE Pin Input Voltage (Ta = 25°C)

-V_{SET} = 1.6 V -V_{SET} = 2.2 V

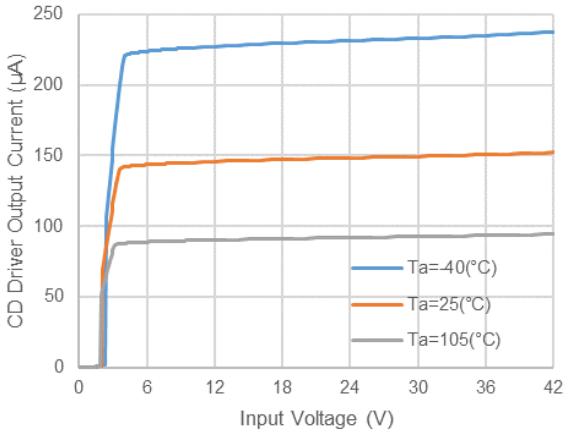


-V_{SET} = 3.0 V -V_{SET} = 4.6 V



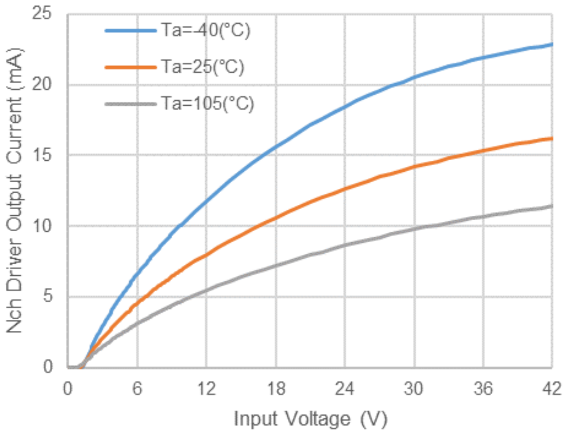
21) C_D Driver Output Current vs. Input Voltage

CE = 5.0 V, SENSE = 5.5 V



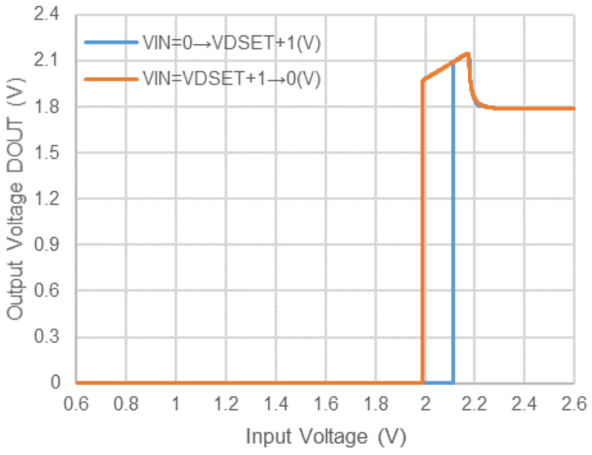
22) Nch Driver Output Current vs. Input Voltage

D_{OUT} = 0.1 V

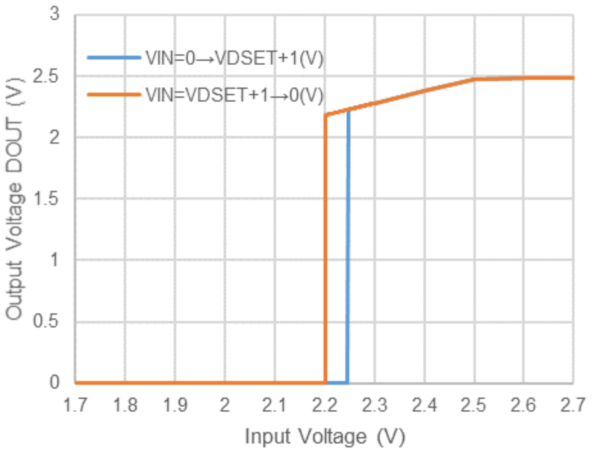


23) D_{OUT} Pin Voltage vs. Input Voltage (V_{OUT} Detection) (Ta = 25°C)

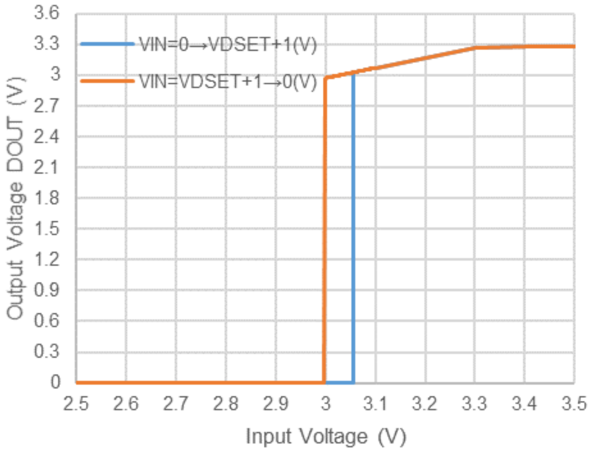
-V_{SET} = 1.6 V



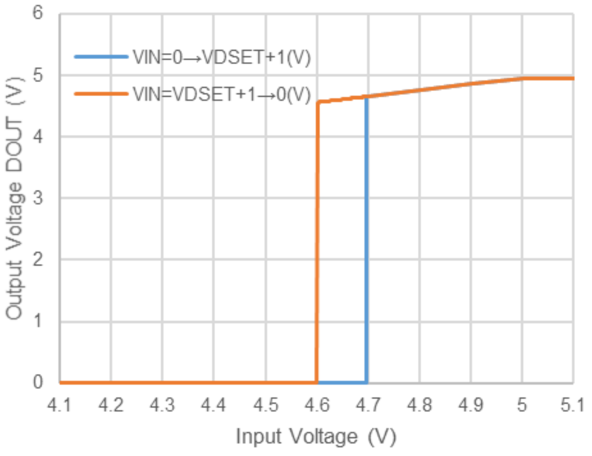
-V_{SET} = 2.2 V



-V_{SET} = 3.0 V



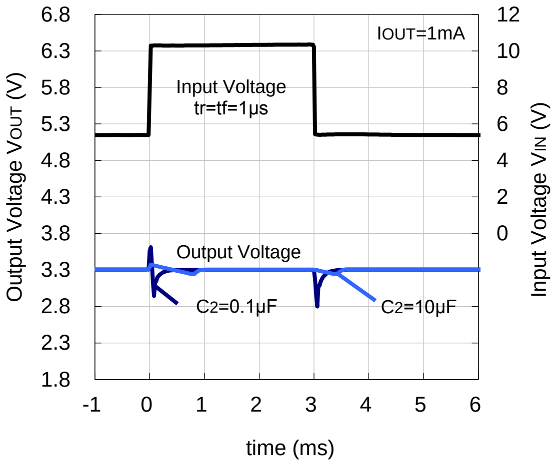
-V_{SET} = 4.6 V



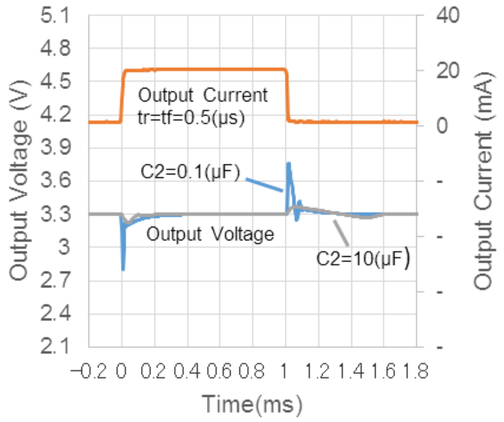
Input Transient/Load Transient vs. Output Capacity (C2)

R5112 performs a stable operation by using 0.1 µF of ceramic capacitor as the output capacitor. However, the variation of output voltage may not meet the demand of the system when input voltage and load current vary. In such cases, the variation of output voltage can be minimized significantly by using 10 µF or higher ceramic capacitor. When using a high-capacity electrolytic capacitor for the output line, place the electrolytic capacitor a few centimeters apart from the IC after arranging the ceramic capacitor close to the IC.

Input Transient Response (V_{SET} = 3.3 V)

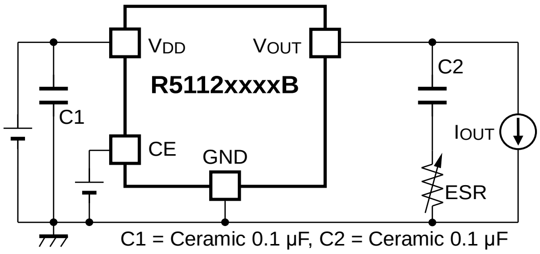


Load Transient Response (V_{SET} = 3.3 V)



ESR vs. OUTPUT CURRENT

It is recommended that a ceramic type capacitor be used for this device. However, other types of capacitors having lower ESR can also be used. The relation between the output current (I_{OUT}) and the ESR of output capacitor is shown below.



Measurement Conditions

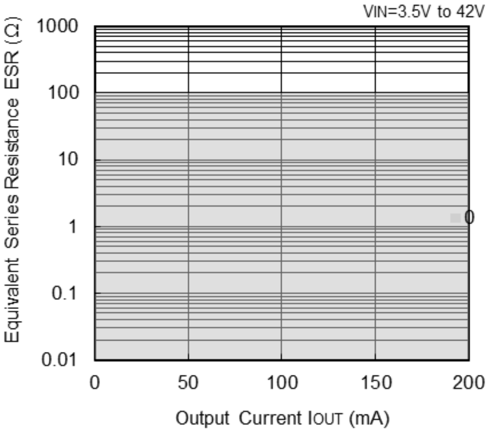
Frequency Band: 10 Hz to 2 MHz

Measurement Temperature: −40°C to 125°C

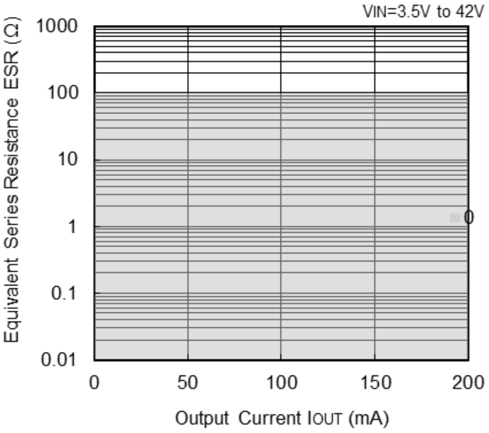
Hatched Area: Noise level is 40 µV (average) or below

Ceramic Capacitors: C1 = 0.1 µF, C2 = 0.1 µF

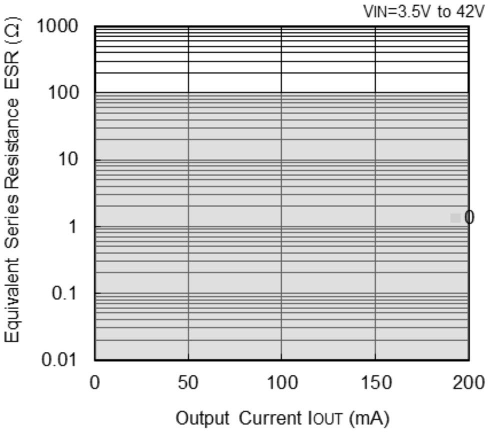
V_{SET} = 1.8 V



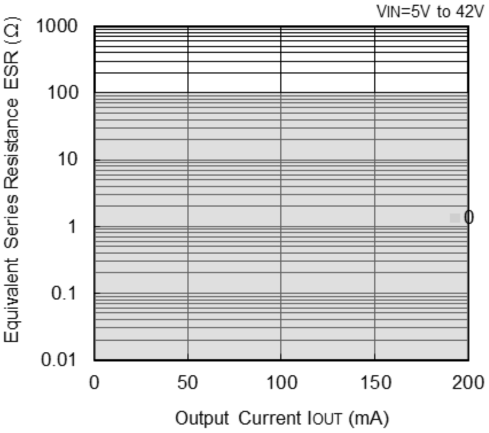
V_{SET} = 2.5 V



V_{SET} = 3.3 V



V_{SET} = 5.0 V



Ver. A

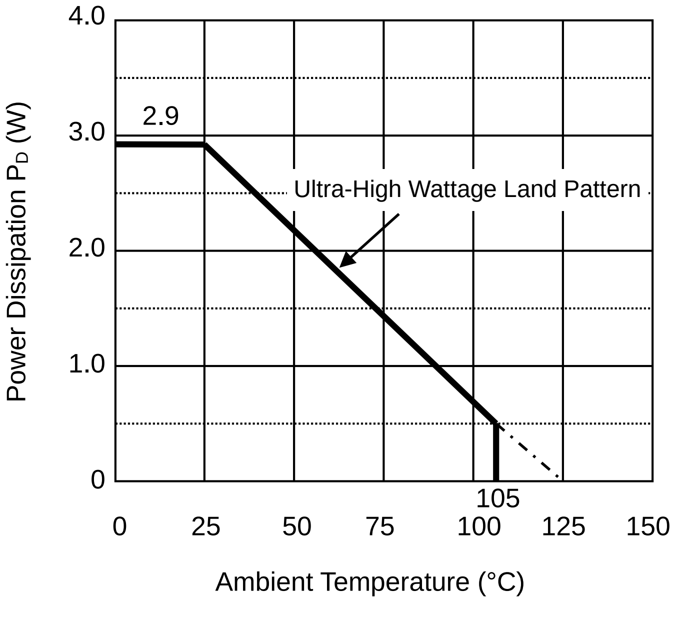
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

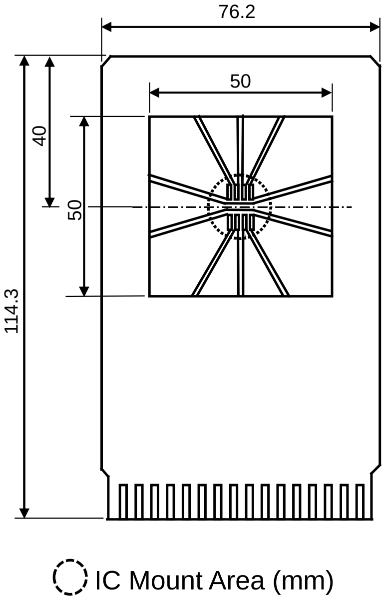
	Ultra-High Wattage Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Approx. 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.4 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Ultra-High Wattage Land Pattern
Power Dissipation	2.9 W
Thermal Resistance	θja = (125 − 25°C) / 2.9 W = 35°C/W θjc = 10°C/W

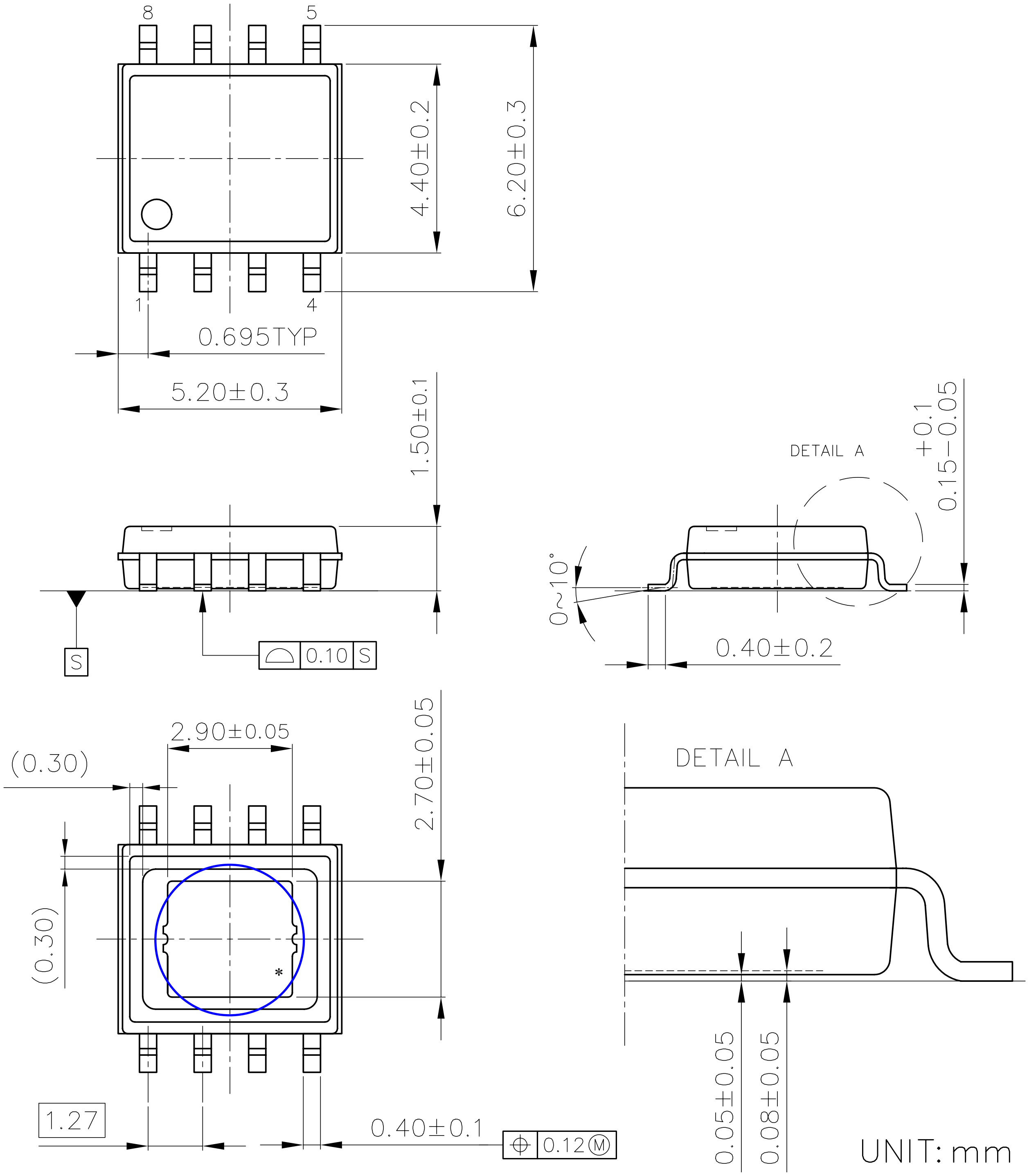


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

PACKAGE DIMENSIONS HSOP-8E



HSOP-8E Package Dimensions

∗ The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

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