Ordering number : ENA0991

SANYO Semiconductors
DATA SHEET

LV8071LP — Bi-CMOS IC Piezoelectric Actuator Driver IC

Overview

The LV8071LP is a piezoelectric autofocus actuator driver IC for use in cell phone cameras. It internally generates drive waveforms, which reduces DSP load and makes it possible to control piezoelectric actuators by simple control signals.

Features

The actuator using the piezoelectric device is driven by the external CLK input and simple control signal.

- The 39MHz (CLK1 pin input) CLK input is divided into quarters internally to generate the 9.75MHz input. The operation time is generated using this as a base CLK to ensure the output appropriate for piezoelectric drive. The CLK2 input of 9.75MHz is input to be used, as it is, for the base CLK either.
- IC start/stop is controlled by the EN input. Initialization is made according to the built-in sequence at startup.
- The actuator drive time is determined by inputting the pulse to the DRIVE pin.
- To recognize operation/stop of the actuator, the BUSY signal is output while the OUT pin performs any output.

Specifications

Maximum Ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		-0.5 to 6.0	V
Output current	I_O max		300	mA
Input signal voltage	V_{IN} max		-0.5 to V_{CC}+0.5	V
Allowable loss	Pd	Mounted on a specified board*	700	mW
Operating temperature range	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

Note *: Mounted on a specified board: 40.0mm×50.0mm×0.8mm, glass epoxy board

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Allowable Operating Condtions at GND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		2.5 to 3.3	V
Input signal voltage	V_{IN}		0 to V_{CC}	V
Input CLK1 frequency	FCLK1	CLK1 pin	39	MHz
Input CLK2 frequency	FCLK2	CLK2 pin	9.75	MHz
DRIVE “H” minimum pulse width	DH min	1clk=1/4CLK1=CLK2	96	clk
DRIVE “L” minimum pulse width	DL min	1clk=1/4CLK1=CLK2	96	clk
Maximum operation cycle frequency	Ct max	1 cycle = 87clk	140 cycles × 170	times

Electrical Characteristics at Ta = 25°C, V_{CC} = 2.8V, GND=0V, unless otherwise specified.

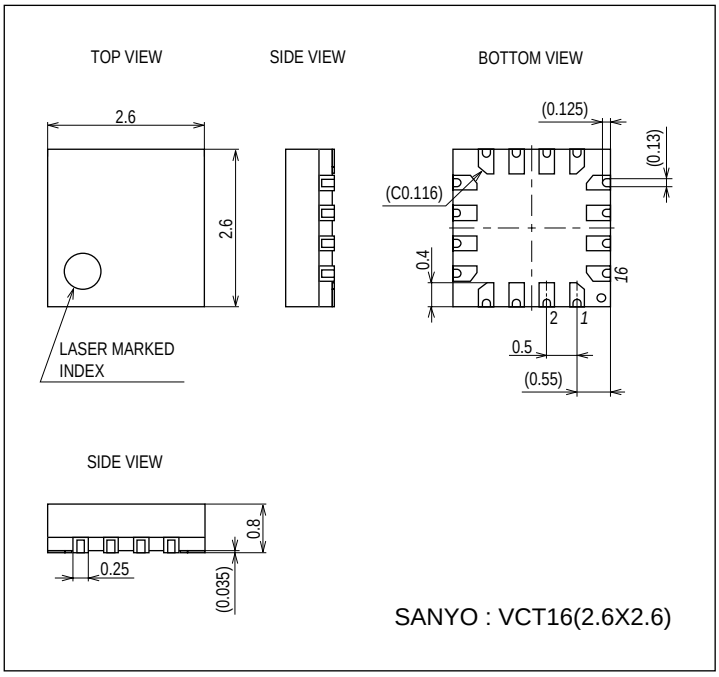
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain at standby 0	$I_{CC}0$	No CLK input			1.0	μA
Current drain during operation	$I_{CC}1$	At CLK1=39MHz		0.4	0.7	mA
“H” level input voltage	V_{IH}	2.5V ≤ V_{CC} ≤ 5.5V	0.8 × V_{CC}		V_{CC}	V
“L” level input voltage	V_{IL}	2.5V ≤ V_{CC} ≤ 5.5V	0		0.1 × V_{CC}	V
Output block upper-side ON resistance	RonP			1.0	1.5	Ω
Output block lower-side ON resistance	RonN			1.0	1.5	Ω
Turn-ON time	TPLH	at no load *			0.2	μs
Turn-OFF time	TPHL	at no load *			0.2	μs

Note: The time for 10→90% at rise and 90→10% at fall is specified.

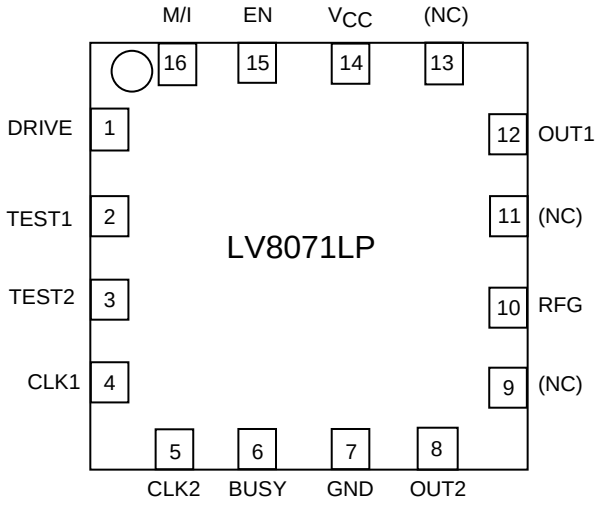
Package Dimensions

unit : mm (typ)

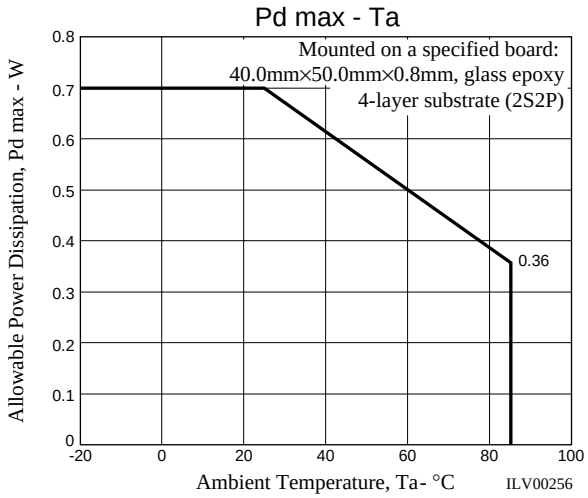
3318



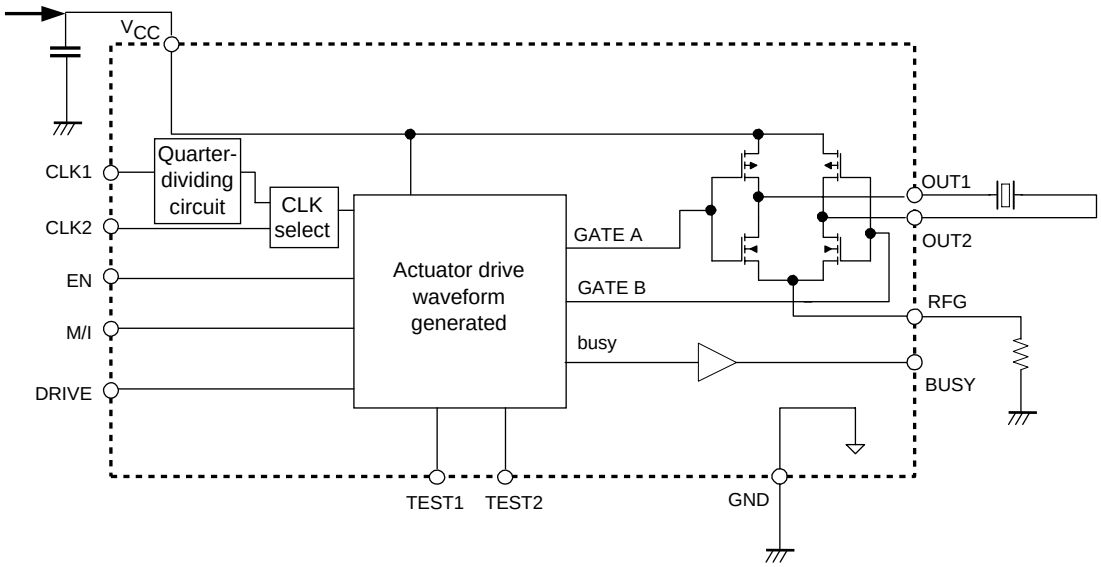
Pin Assignment



Top view



Block Diagram



Resistance to be provided to the RFG pin

In LV8071LP, insertion of the resistor between RFG and GND pins enables suppression of the inrush current to the piezoelectric element.

Since the resistance value exerts influence on the actuator operation, determine the constant within the 0Ω to 3.3Ω range while checking the operation.

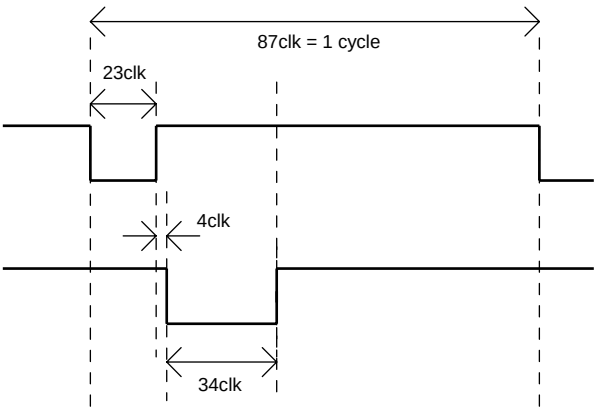
Description of the Operation

- CLK1 and CLK2 inputs

  CLK1 incorporates the quarter-dividing circuit. To input 39MHz directly, input it directly to the CLK1 pin.
  When the dividing circuit is provided externally, input 9.75MHz to the CLK2 pin.
  Short-circuit the unused CLK pin to GND.

- 1 cycle:

  One cycle (8.923µs for CLK1=39MHz or CLK2=9.75MHz) of OUT waveform operation is used as one unit of output operation.
  The drive waveform appropriate to piezoelectric drive as shown below is generated in IC. (1clk=1/4CLK1=1CLK2)



- EN input:

  L input causes the IC functions to stop to suppress the current drain in the standby state.
  H input causes IC to start. After initialization according to the start sequence, the DRIVE pin is ready to accept the input.

- Initialization:

  Internal sequence to move the actuator to the initial position at start of IC.
  After the operation of 140 cycles × 170 times in the ∞ direction, the standby time of 140 cycles × 4 times is secured.
  Then, 140 cycles × 2 times of return operation is made in the macro direction.

- DRIVE input:

  Operation time setting pin. The pin performs 140 cycles of operation per pulse at pulse input.
  To prevent noise-induced error, the input with the pulse H/L width of 96clk (9.85µs when CLK = 39MHz) respectively is not accepted.

- M/I input:

  Actuator operation direction setting pin. Actuator is set in the macro direction at the input H and in the ∞ direction at the input of L. The actuator stops operation if M/I is changed over even when it is operating with the DRIVE pulse.

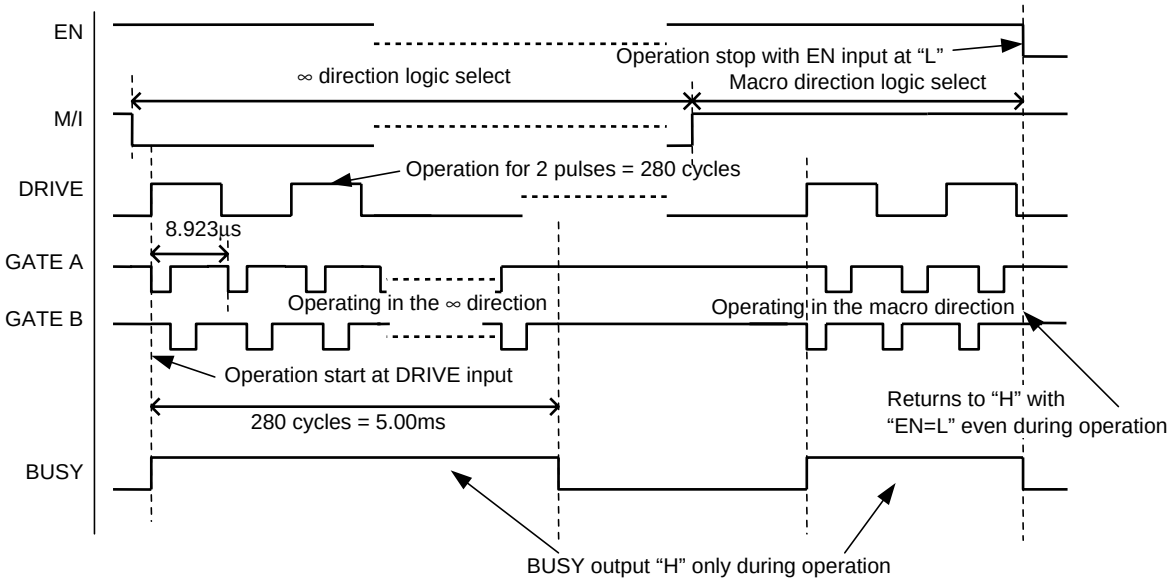
- TEST1/2

  Setting pin for IC inspection. Short-circuit this pin with GND during actual use.

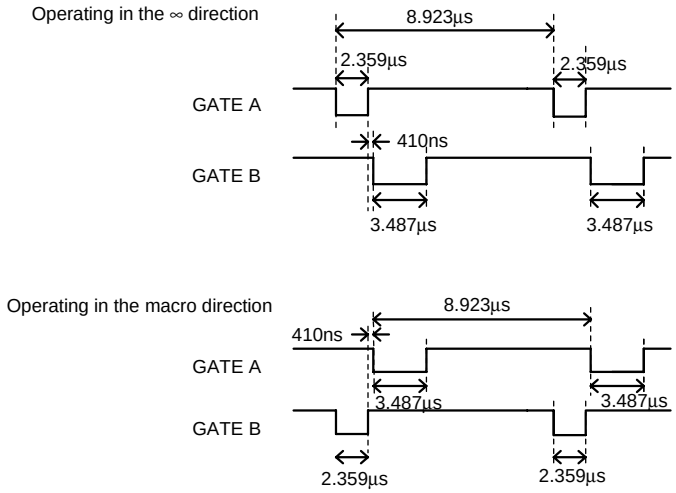
- BUSY output:

  The signal output pin, which outputs “H=VCC voltage while the actuator is operating and “L” when the actuator is stopped.

Timing Chart **(For CLK1=39MHz)**



Enlarged view of gate signal sequence



Initialization sequence at startup