High Temperature, Low Drift, Micropower 2.5 V Reference

Data Sheet **ADR225**

FEATURES

- **Extreme high temperature operation**
  - **−40°C to +210°C, 8-lead FLATPACK**
  - **−40°C to +175°C, 8-lead SOIC**
- **Temperature coefficient**
  - **40 ppm/°C, 8-lead FLATPACK**
  - **10 ppm/°C, 8-lead SOIC**
- **High output current: 10 mA**
- **Low supply current: 50 µA maximum**
- **Initial accuracy: ±0.4% (±10 mV maximum), 8-lead SOIC**
- **Low dropout voltage**
- **Wide supply range: 3.3 V to 16 V**

APPLICATIONS

- **Down-hole drilling and instrumentation**
- **Avionics**
- **Heavy industrial**
- **High temperature environments**

PIN CONFIGURATION

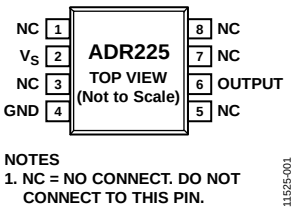

Figure 1. Pin Configuration for SOIC and FLATPACK Packages

GENERAL DESCRIPTION

The ADR225 is a precision 2.5 V band gap voltage reference specified for a high temperature operation of 175°C and 210°C. It uses a micropower core topology and laser trimming of highly stable, thin film resistors to achieve a temperature coefficient of 30 ppm/°C (maximum) up to 175°C and an initial accuracy of 0.4% (±10 mV maximum). A maximum operating current of 50 µA and a low dropout voltage allow the ADR225 to function very well in battery-powered equipment.

The ADR225 voltage reference is offered in an 8-lead SOIC package with an operating temperature range of −40°C to +175°C. It is also available in an 8-lead ceramic flat pack (FLATPACK) with an operating temperature range of −40°C to +210°C. Both devices are designed for robustness at extreme temperatures and are qualified for 1000 hours of operation at the maximum temperature rating.

The ADR225 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of the available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

Rev. B **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support**

www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

11/13—Rev. A to Rev. B

Change to Features Section 1
Added Caption to Figure 1 1
Changes to Table 1 3
Added Figure 6, Figure 7, Figure 8, Figure 12, Figure 13, Figure 14, Figure 18, and Figure 19; Renumbered Sequentially 5

9/13—Rev. 0 to Rev. A

Changes to Data Sheet Title and Added Wide Supply Range: 3.3 V to 16 V to Features Section 1
Changed Supply Voltage from −0.3 V to +15 V to −0.3 V to +18 V; Table 2 4

7/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 3.3 V, V_{OUT} = 2.5 V, $T_{MIN} < T_A < T_{MAX}$, unless otherwise noted.

Table 1.

			8-Lead SOIC −40°C ≤ T_A ≤ +175°C			8-Lead FLATPACK −40°C ≤ T_A ≤ +210°C			
Parameter	**Symbol**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SUPPLY CURRENT	I_{SY}	No load		30	50		40	60	µA
INITIAL ACCURACY[1]	V_O	I_{OUT} = 0 mA		±2	±10		±5	±60	mV
TEMPERATURE COEFFICIENT[2]	TCV_{OUT}	I_{OUT} = 0 mA		10	30		40	80	ppm/°C
REGULATION									
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		0.025	0.1		0.25	1.5	mV/V
Load Regulation[3]	$\Delta V_{OUT}/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 10 mA		0.025	0.1		0.25	1.5	mV/mA
VOLTAGE									
Dropout Voltage	$V_S - V_{OUT}$	I_{LOAD} = 10 mA			1.00			1.00	V
Noise Voltage	e_N	0.1 Hz to 10 Hz		25			25		µV p-p

[1] For proper operation, a 1 µF capacitor is required between the OUTPUT pin and the GND pin of the device.

[2] TCV_{OUT} is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_{OUT} = (V_{MAX} - V_{MIN})/V_{OUT}(T_{MAX} - T_{MIN})$$

[3] Load regulation specification includes the effect of self-heating.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	−0.3 V to +18 V
OUTPUT to GND	−0.3 V to V_S + 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
8-Lead SOIC	−40°C to +175°C
8-Lead FLATPACK	−40°C to +210°C
Junction Temperature Range	
8-Lead SOIC	−40°C to +200°C
8-Lead FLATPACK	−40°C to +245°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PREDICTED LIFETIME vs. OPERATING TEMPERATURE

Comprehensive reliability testing is performed on the ADR225. Product lifetimes at extended operating temperature are obtained using high temperature operating life (HTOL). Lifetimes are predicted from the Arrhenius equation, taking into account potential design and manufacturing failure mechanism assumptions. HTOL is performed to JEDEC JESD22-A108. A minimum of three wafer fab and assembly lots are processed through HTOL at the maximum operating temperature. Comprehensive reliability testing is performed on all Analog Devices, Inc., high temperature (HT) products.

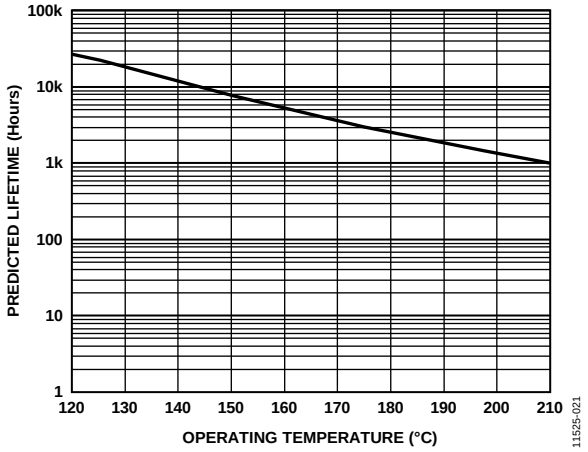

Figure 2. Predicted Lifetime vs. Operating Temperature

THERMAL RESISTANCE

θ_{JA} is specified for worst-case conditions; that is, θ_{JA} is specified for the device soldered in the circuit board.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	121	43	°C/W
8-Lead FLATPACK	100	15	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 3.3 V, V_{OUT} = 2.5 V, $T_{MIN} \le T_A \le T_{MAX}$ for 8-lead SOIC package, unless otherwise noted.

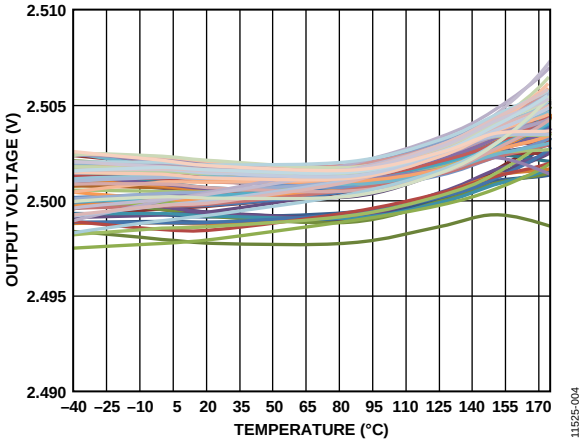

Figure 3. Output Voltage (V_{OUT}) vs. Temperature

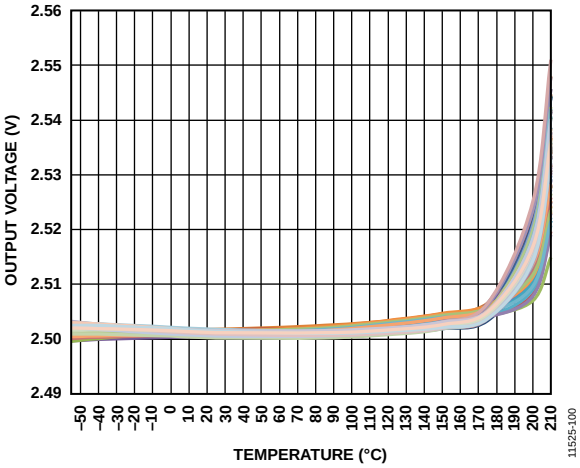

Figure 6. Output Voltage (V_{OUT}) vs. Temperature, FLATPACK Package

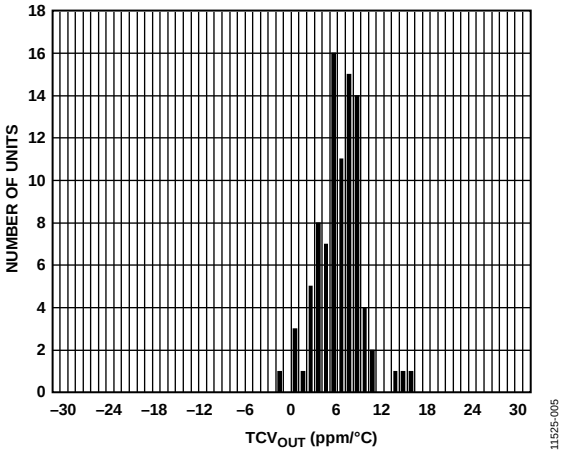

Figure 4. TCV_{OUT} Distribution, −40°C to +175°C

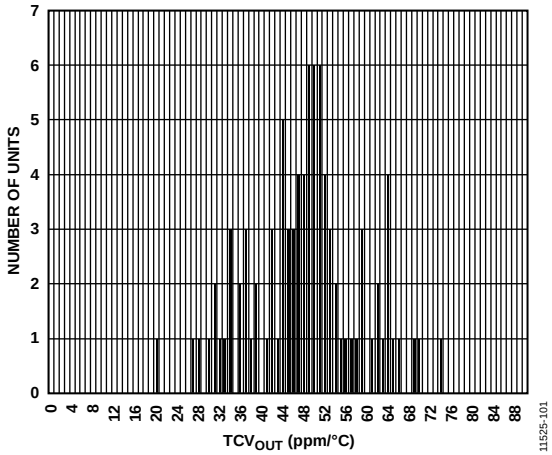

Figure 7. TCV_{OUT} Distribution, −40°C to +210°C, FLATPACK Package

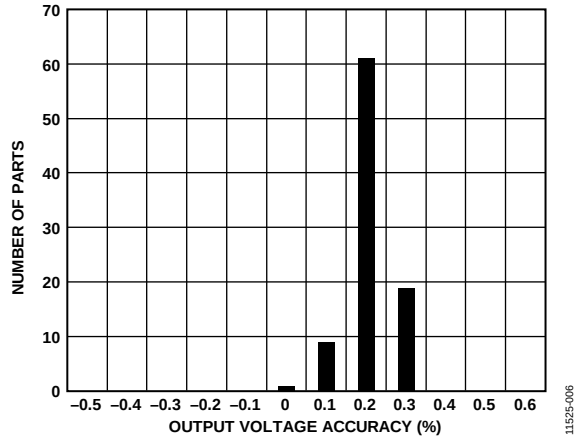

Figure 5. Output Voltage Accuracy at 175°C

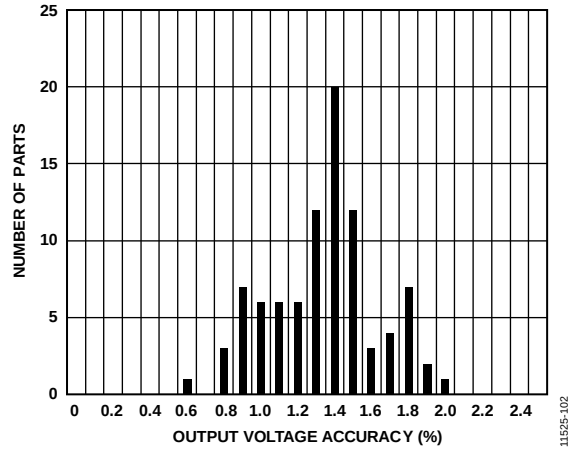

Figure 8. Output Voltage Accuracy at 210°C, FLATPACK Package

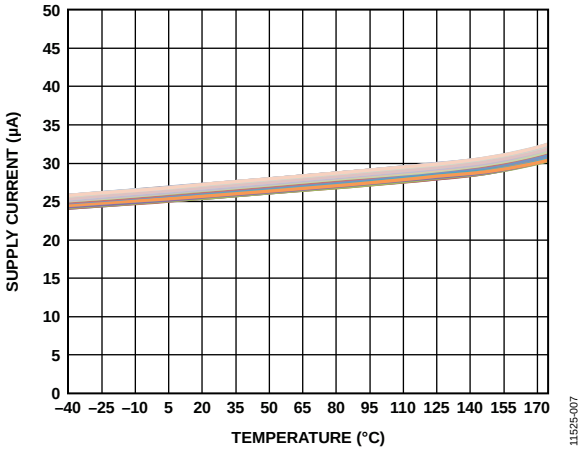

Figure 9. Supply Current (I_{SY}) vs. Temperature

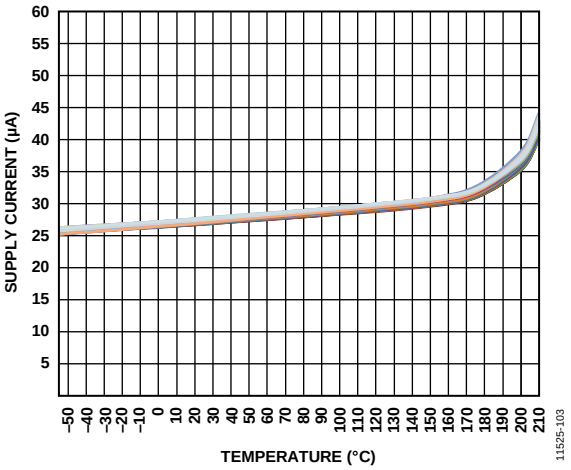

Figure 12. Supply Current (I_{SY}) vs. Temperature, FLATPACK Package

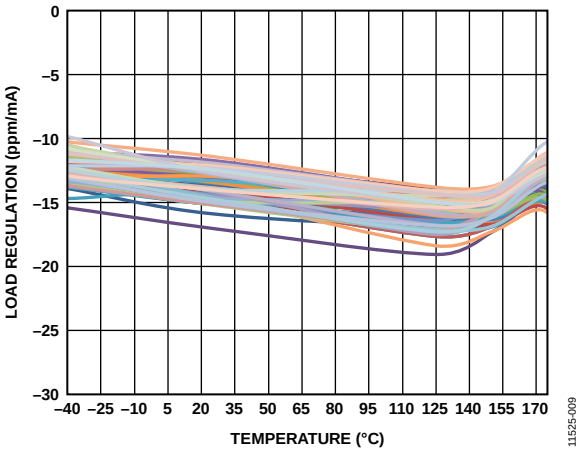

Figure 10. Load Regulation vs. Temperature (I_{LOAD} = 0 mA to 10 mA)

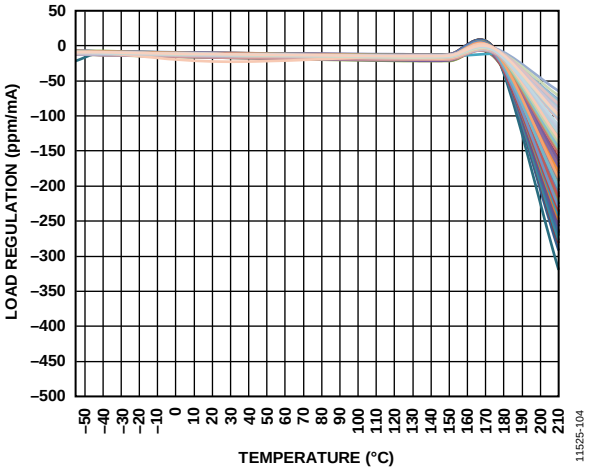

Figure 13. Load Regulation vs. Temperature (I_{LOAD} = 0 mA to 10 mA), FLATPACK Package

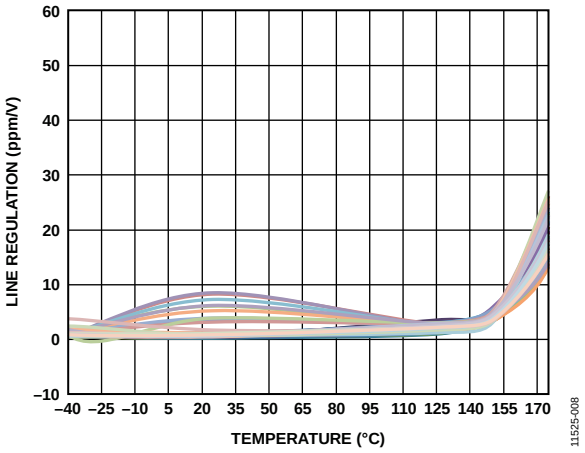

Figure 11. Line Regulation vs. Temperature

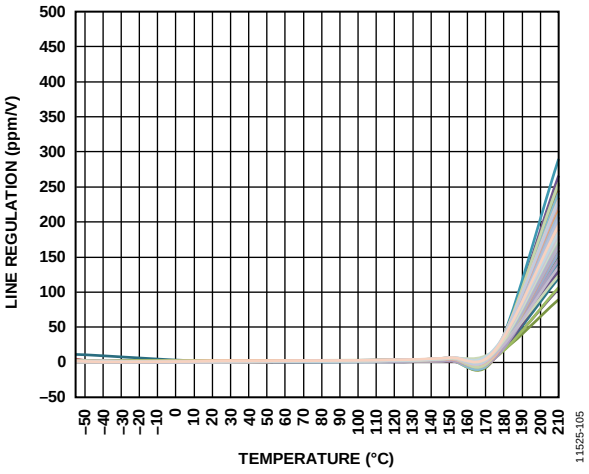

Figure 14. Line Regulation vs. Temperature, FLATPACK Package

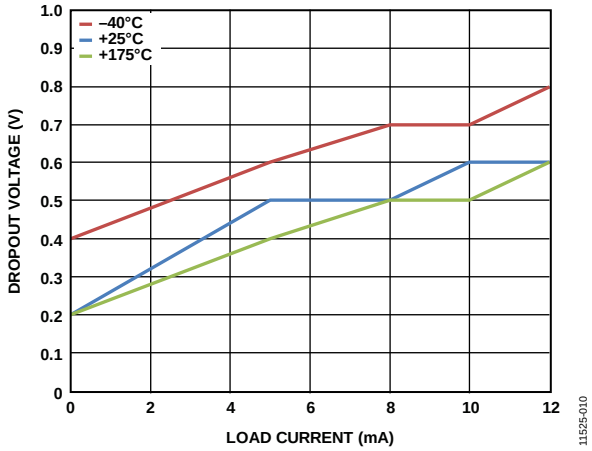

Figure 15. Dropout Voltage vs. Load Current (I_{LOAD})

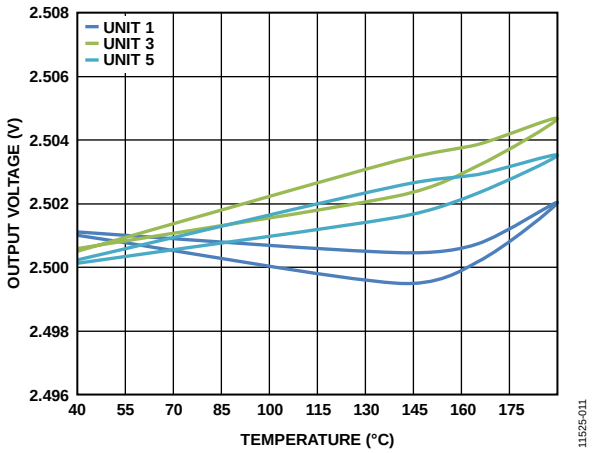

Figure 16. Thermal Hysteresis, I_{LOAD} = 0 mA

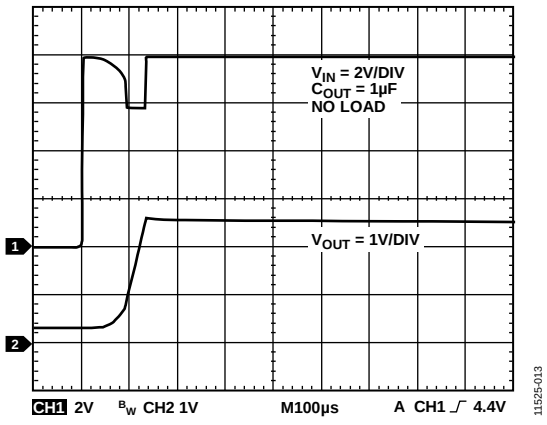

Figure 17. Power-On Response (see Figure 25)

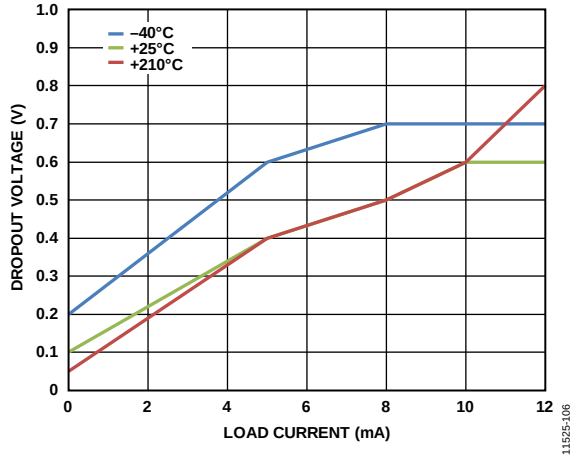

Figure 18. Dropout Voltage vs. Load Current (I_{LOAD}), FLATPACK Package

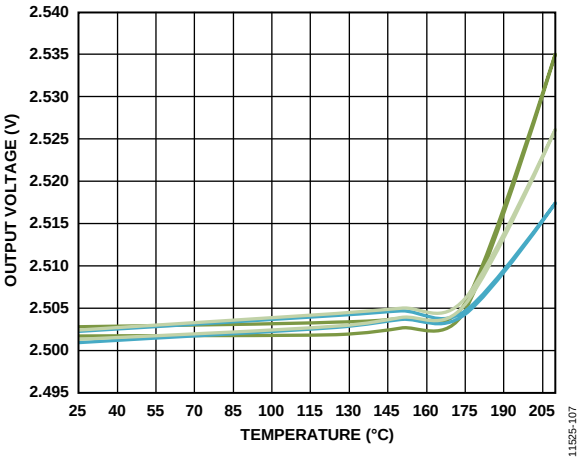

Figure 19. Thermal Hysteresis, I_{LOAD} = 0 mA, FLATPACK Package

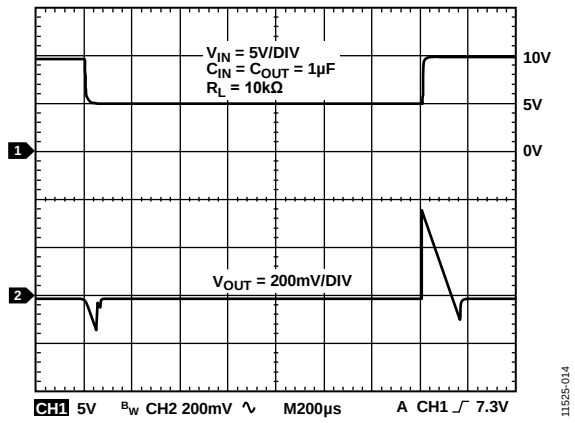

Figure 20. Line Transient Response (see Figure 25)

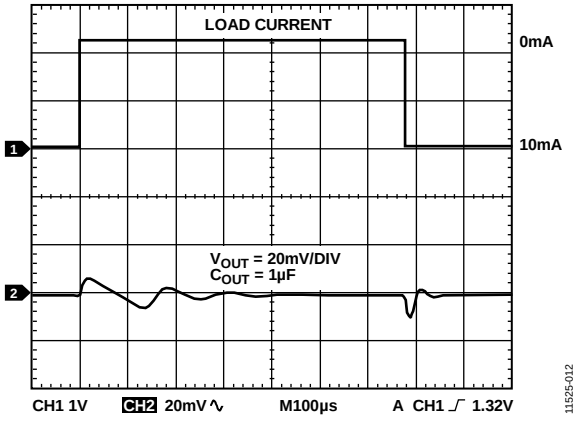

Figure 21. Load Transient Response

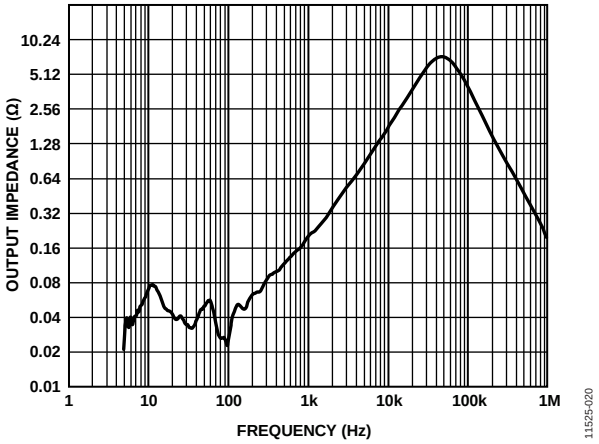

Figure 23. Output Impedance (Z_{OUT}) vs. Frequency, $C_{IN} = C_{OUT} = 1\ \mu F$

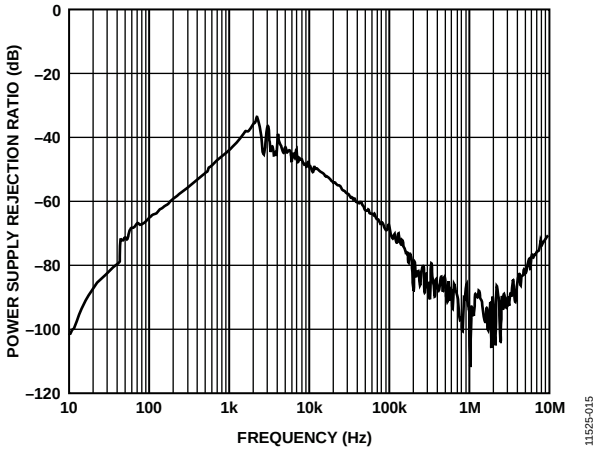

Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency, $C_{LOAD} = 1\ \mu F$

THEORY OF OPERATION

BASIC VOLTAGE REFERENCE CONNECTIONS

The circuit shown in Figure 24 is the basic configuration for the ADR225. Note that a 10 µF and 0.1 µF bypass network on the input and at least a 1 µF bypass capacitor on the output are required for proper device operation. It is recommended that no connections be made to Pin 1, Pin 3, Pin 5, Pin 7, and Pin 8.

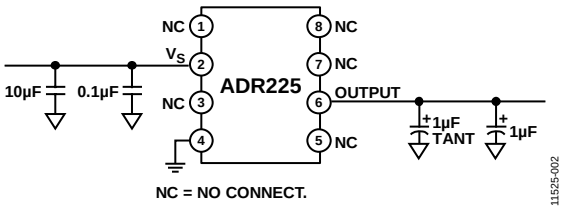

Figure 24. Basic Voltage Reference Connections

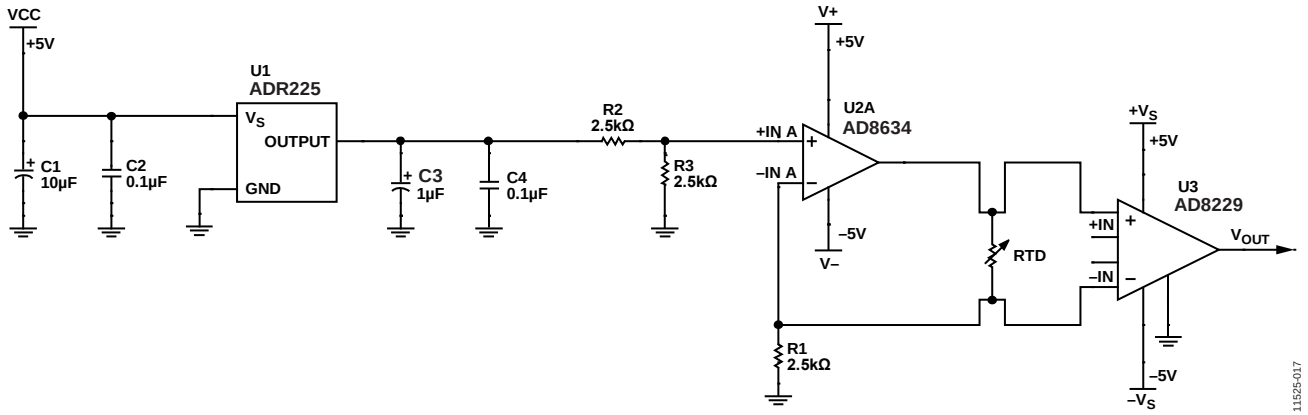

Figure 25. Typical High Temperature Resistance Temperature Detector (RTD) Signal Conditioning Circuit

OUTLINE DIMENSIONS

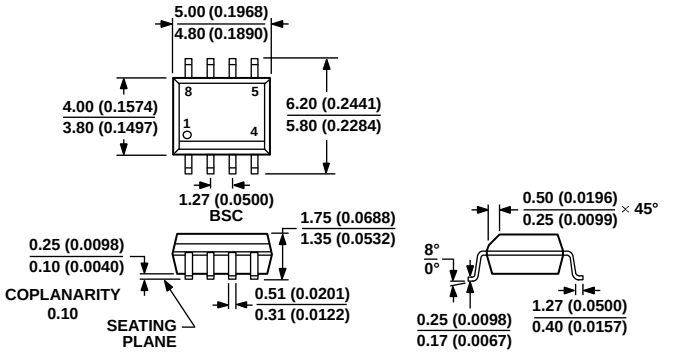

Figure 26. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

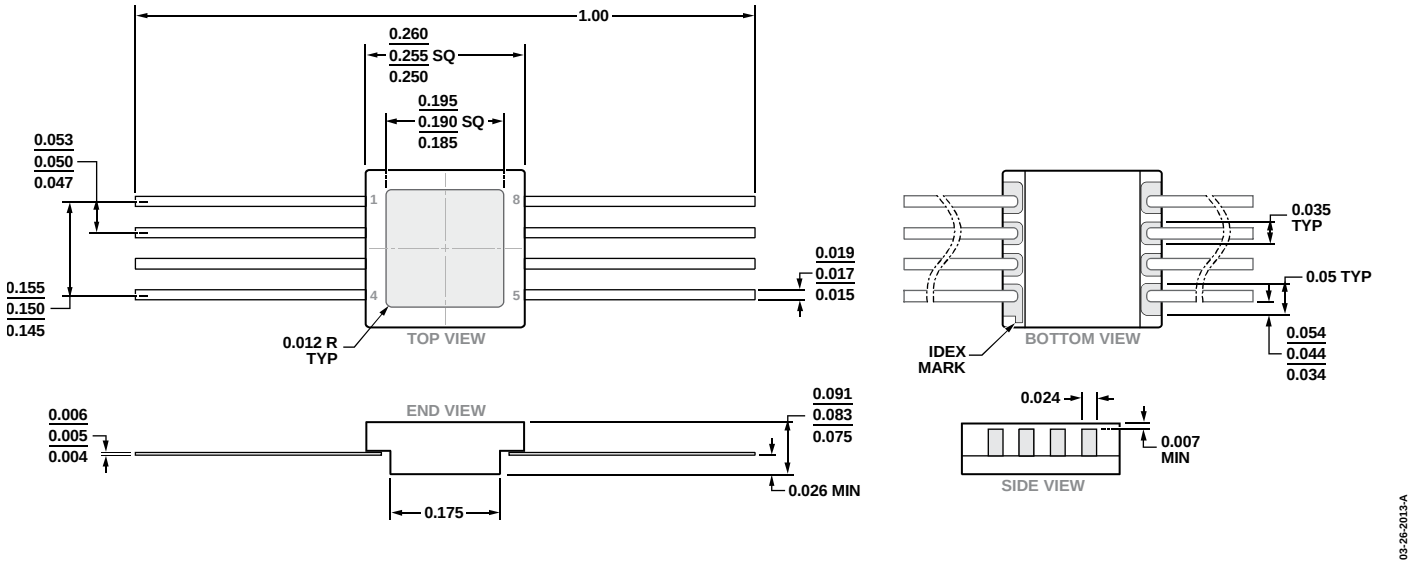

Figure 27. 8-Lead Ceramic Flat Package [FLATPACK]
(F-8-2)
Dimensions shown in inches

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADR225HRZN	−40°C to +175°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADR225HFZ	−40°C to +210°C	8-Lead Ceramic Flat Package [FLATPACK]	F-8-2

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D11525-0-11/13(B)