

# Keysight U4431A

## MIPI M-PHY Protocol Analyzer

Deep insight to help you win the race to M-PHY

Data Sheet



# Accelerate M-PHY Products with Deep Insight Across your Entire Design

The image displays the Keysight U4431A MIPI M-PHY Protocol Analyzer software interface, annotated with red circles and numbers 1 through 12, highlighting key features:

- 1**: Main data table showing packet details such as Time, Direction, Depth, Number, and Data.
- 2**: Overview diagram showing the system architecture and signal paths.
- 3**: Settings panel for the selected protocol or channel.
- 4**: Lane configuration table for the selected protocol.
- 5**: Hexadecimal data view for the selected packet.
- 6**: ASCII data view for the selected packet.
- 7**: Traffic Overview table showing protocol statistics.
- 8**: Waveform view showing signal timing and eye diagrams.
- 9**: Trigger configuration dialog for capturing specific events.
- 10**: Trigger configuration dialog for capturing specific events.
- 11**: Error log table showing detected errors and their details.
- 12**: Performance analysis graph showing signal quality metrics over time.

## Accelerate M-PHY Products with Deep Insight Across your Entire Design (Continued)

1. Link multiple windows together or track correlated events with markers
2. Any number of filters and views can be applied. Organize them easily in the overview GUI
3. Peel-off tabs let you isolate packet details
4. Lanes
5. Headers
6. Payload
7. Get the “big picture” with the Overview tab
8. Raw Mode lets you see the “why” behind your protocol. Integrate with any Infiniium oscilloscope
9. Quickly customize simple drag-and-drop trigger macros
10. Use advanced if-then-else triggers to branch in any direction to up to eight different conditions. Add counters, timers, and flags for even more control
11. Transaction decode shows what packets mean at the application layer. Track bus events from waveforms to bytes to packets to transactions
12. Performance overview gives you insight into trending system behavior like bandwidth, credit values, and link utilization

### Key features:

- Track multiple M-PHY® busses from the PHY to the Application layer
- Up to HS Gear 3 data rates
- Up to 16 GB trace depth
- Up to 4 data lanes
- Raw Mode 8 b/10 b data views
- N-way trigger branching
- Performance analysis view for optimizing designs
- Transaction level decode view for insight from signals to the application layer
- Packet generation option for conformance and compliance testing of UniPro<sup>SM</sup> and UFS

### Target users:

#### Designers and validators of

- M-PHY
- IP
- Application processors
- Memory/chipsets
- Mobile devices
- Mobile embedded systems

### Broad and deep insight into your mobile computing designs.

Time correlate multiple busses and views. Up to 5 modules (M-PHY, D-PHY<sup>SM</sup>, PCI, DDR, and high-speed logic,) can be integrated in one mainframe, and multiple frames can be connected for even greater flexibility. Modules and protocols can be correlated and cross-triggered. This makes it easy to see how different parts of your design interact. Link multiple windows together (6) or track correlated events with up over 1,000 user-defined markers.

Customize your display in seconds. Isolate any packet’s header (5), or data as a packet payload (6) or individual lanes (4) with “peel off” tabs. Adjust data columns just like you would in a spreadsheet – drag and drop columns, double click dividers to resize, right-click to add/delete content.

Raw Mode (8) lets you see the “why” behind your protocol. Raw 8b/10b data that is acquired by the analyzer can be displayed as a time-correlated waveform view. Look even deeper by adding time-correlated traces from your Infiniium oscilloscope.

Get the “big picture” with analysis tools. The Overview tab (7) generates a count of the various types of traffic in any period of time, including errors; then step through each occurrence with embedded navigation tools. Use global markers to make time and occurrence measurements across all display views.

The Transaction Decoder converts MIPI® packets into the high-level application traffic they transport. This makes it easier to understand traffic flow in context. The Performance Overview tab (12) lets you see the long-term trends of key performance parameters like flow control and up/down data rates and bus utilization. Both tabs are fully integrated with other views with markers and window lock stepping.

Want to try out the UI? Download a copy of the interface at [www.keysight.com/find/la-sw-download](http://www.keysight.com/find/la-sw-download), and load the built-in demo files.

## Accelerate M-PHY Products with Deep Insight Across your Entire Design (Continued)

### Isolate events with protocol-aware triggers.

Simple drag-and-drop trigger macros can be quickly customized by clicking on the blue hyperlink. Or choose advanced if-then-else triggers to branch in any direction to up to 8 different conditions, and add a variety of qualifying conditions.

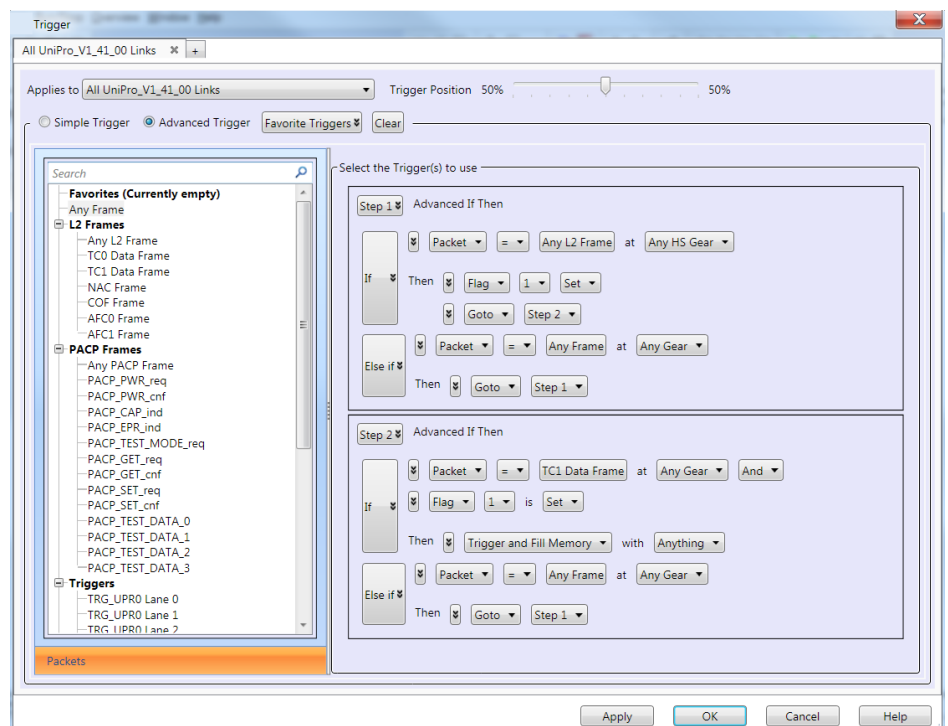
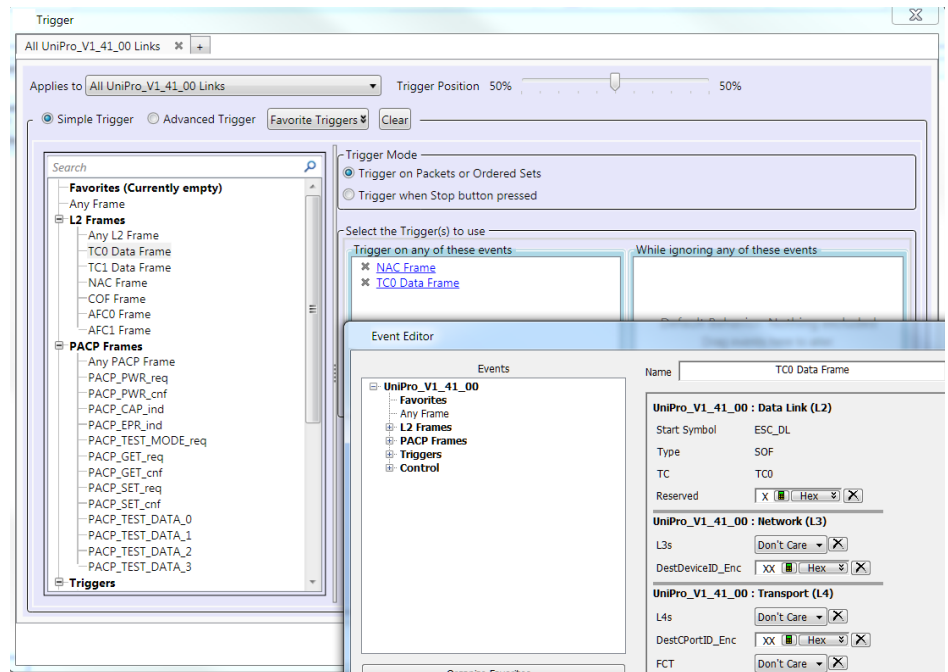
Trigger on packet types, PHY and stack errors, payload data (up to 32 bytes), flags, counters, and time delays. You can also specify speed, transmission type, and link state.

### Probing that leverages Keysight's high-speed oscilloscope and high-speed logic analysis technologies.

The U4433A high-Z MIPI M-PHY differential probe connects to Keysight's 12 GHz ZIF tips to ensure a flexible, yet non-intrusive connection. U4433A is the recommended probe for most applications.

The U4432A is an impedance-matched SMA probe for use with the packet generator option (613). It is not intended for mid-bus probing.

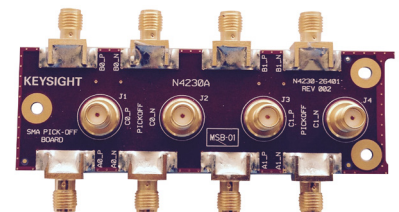
However, the N4230A breakout board can be used to give U4432A the impedance characteristics of the U4433A flying probe. As a result, you can connect your host and device boards with SMA cables, and they do not require a solder-in connection. Please refer to the U4431A Hardware and Probing guide (publication number U4431-97001) for proper use and topography.



U4432A SMA probe



U4433A differential probe



N4230A SMA breakout board for U4432A

## Packet Generator (Option 613) and Conformance Testing for UFS/UniPro

The U4431A MIPI M-PHY analyzer also offers an optional packet generator (Option 613). This option allows the analyzer to emulate host system behavior while interacting with a UFS/UniPro device. The packet generator can bring up the UFS link, configure the device, and make read/write requests to the device. This makes it possible to test UFS conformance under a variety of conditions.

The analyzer can also capture the traffic sent to the target system, as well as all responses from the device – and can trigger on these responses. In this manner, Option 613 allows the analyzer to act as either a bi-directional mid-bus analyzer (Option 612) or as a packet generator + 1½ direction analyzer (packets-only capture in Tx direction + full analyzer features in Rx direction).

The packet generator is controlled at the command line and includes a library of functions and test scripts that can be customized by the user.

This packet generator is compatible with Protocol Insight's UFS20COMP Test Executive™ for UFS and UNI16COMP Test Executive™ for UniPro. These software packages automate hundreds of test specification cases and can be expanded and customized for user-specific requirements. You can learn more at [www.protocolinsight.com](http://www.protocolinsight.com).

The screenshot shows the Agilent Command Line Packet Generator interface. On the left is a tree view of functions categorized by file names like 'AgSpaceAccess.tcl', 'AgIntrusion.tcl', 'AgHostControl.tcl', etc. The main pane displays details for selected functions such as DME\_ENABLE, DME\_ENDPOINTRESET.req, DME\_HIBERNATE\_ENTER.req, DME\_HIBERNATE\_EXIT.req, and DME\_LINKSTARTUP.cnf. A text area on the right shows a test script with comments and commands like 'proc DME\_ENABLE', 'proc DME\_ENDPOINTRESET.req', etc., along with configuration paths and traffic control instructions.

The screenshot shows the Protocol Insight Test Executive interface. The top pane displays a list of test cases under the category 'Test: 8.3.2 UFS BOOT 02 (3 items)'. The bottom pane shows a detailed test results table with columns for Status, Rule, Failure, Packet, Byte, Test#, LUN, Speed, and Link Width. The results show several failures related to reserved flag bits and response success conditions. A detailed packet decode view on the right shows the structure of a packet, including Transaction Code (NOPOUT), LUN (NON), and various reserved fields.

Status	Rule	Failure	Packet	Byte	Test#	LUN	Speed	Link Width
Warning	Reserved Flag Bits shall be 0x00	0x0e	1	1	226	NONE (LUN...)	PWM G1	X1
Warning	Reserved (byte 7) shall be 0x00	0x07	1	7	226	NONE (LUN...)	PWM G1	X1
Warning	Reserved (byte 9) shall be 0x00	0x0b	1	9	226	NONE (LUN...)	PWM G1	X1
Warning	Reserved (bytes 24-27) shall be 0x0000...	0x10000000	3	24	226	NONE (LUN...)	PWM G1	X1
Warning	Reserved (bytes 24-27) shall be 0x0000...	0x10000000	5	24	226	NONE (LUN...)	PWM G1	X1
Failed	Response shall be SUCCESS	0x06	1	6	226	NONE (LUN...)	PWM G1	X1
Failed	Device Information shall be 0x00	0x0b	1	9	226	NONE (LUN...)	PWM G1	X1
Failed	Query Response shall be SUCCESS	0x07	3	6	226	NONE (LUN...)	PWM G1	X1
Failed	IDN shall be 0x01	0x09	3	13	226	NONE (LUN...)	PWM G1	X1
Failed	Query Function shall be STANDARD R...	0x81	5	5	226	NONE (LUN...)	PWM G1	X1
Failed	Query Response shall be SUCCESS	0x0f	5	6	226	NONE (LUN...)	PWM G1	X1
Failed	OPCODE shall be READ FLAG	0x06	5	12	226	NONE (LUN...)	PWM G1	X1
Failed	IDN shall be 0x01	0x09	5	13	226	NONE (LUN...)	PWM G1	X1
Failed	FLAG VALUE shall be 0x00	0x01	5	23	226	NONE (LUN...)	PWM G1	X1

## U4431A – Performance Characteristics

<b>Electrical</b>	
Minimum Vdiff	100 mV
Input impedance (DC)	
– U4433A probe + N5246A ZIF tips	700 Ω, typical
– U4432A SMA harness	128 Ω, typical
<b>Topological</b>	
Lane width	Up to 4 with option 414. Analyze 1, 2, 3, or 4-lane systems
Clocking architecture	Type I
Analysis direction	Processor-peripheral or peripheral-processor (Both directions with option 612)
Lane remapping	User-selectable
Lane polarity	User-selectable
Multiple blade support	Up to 5 time-correlated blades in one frame (configured as up to 3 separate busses), multiple frames can be correlated
<b>Performance</b>	
HS Modes supported	G1 to G3
PWM Modes supported	G0 to G7 (subject to limitations of individual protocol)
Rate Series supported (HS and PWM)	A and B
Symbol lock time (subject to protocol spec limit)	
– HS-G1	1 symbol, typical
– HS-G2, HS-G3	< 128 symbols
Auto speed detection and tracking	Supported (with no RSE-PO-TX support)
<b>Memory</b>	
	<b>User allocated (shared among analyzer and raw mode)</b>
Standard	1 GB
Option M04	4 GB
Option M16	16 GB
<b>Data views</b>	
Protocol version support	
– UniPro	Unified Protocol (UniPro) 1.60
– UFS	Universal Flash Storage (UFS) 2.0 (JESD220B)
– Physical Layer	M-PHY 3.0
– CSI-3	Camera Serial Interface 3, 1.1
– SSIC	Super Speed Inter-Chip(Inter-Chip Supplement to the USB Revision 3.0 Specification)
– M-PCIe	ECR to PCIe® Specification 3.0, May 2013
– Protocol views	Packets, header, lanes, payload, and traffic overview
– Packet hierarchy views	Data, Link, Network, Transport, Protocol
– Protocol details	Speed, CRC, direction, errors
Waveform view	Yes, raw 8 b and 10 b data
Listing data view	Yes
Correlation markers	> 1,000 user-defined
Marker measurements	Yes, user-defined time and count measurements
Window correlation lock	Yes, user-defined
<b>Triggering</b>	
Trigger on protocol commands	Yes, with > 50 macros
Simple trigger	Drag and drop
Advanced trigger	
– Sequence levels	Up to 8
– Logical branching	N-way
– Advanced trigger events	Timer, counter with timeout, flags, AND/OR
Protocol triggers	
– Trigger on protocol patterns	Yes
– Protocol pattern customization	Yes, with bit-level editing
– Payload pattern matcher	Up to 8 4-byte patterns
– Transmission type (HS/PWM)	Yes
– Specific transmission speed	Yes
– Link state	Yes

## U4431A – Performance Characteristics (Continued)

### Triggering (Continued)

Real-time error detection	
– 8 b/10 b	Yes
– Disparity	Yes
– CRC	CRC32,16,5
– Flow control	Yes

### Analysis

LED indicators	Sub-link state and lane width
Traffic overview	Packet count with occurrence navigation
Filters	User-defined packet and error filters
Search	User-defined packet and error search

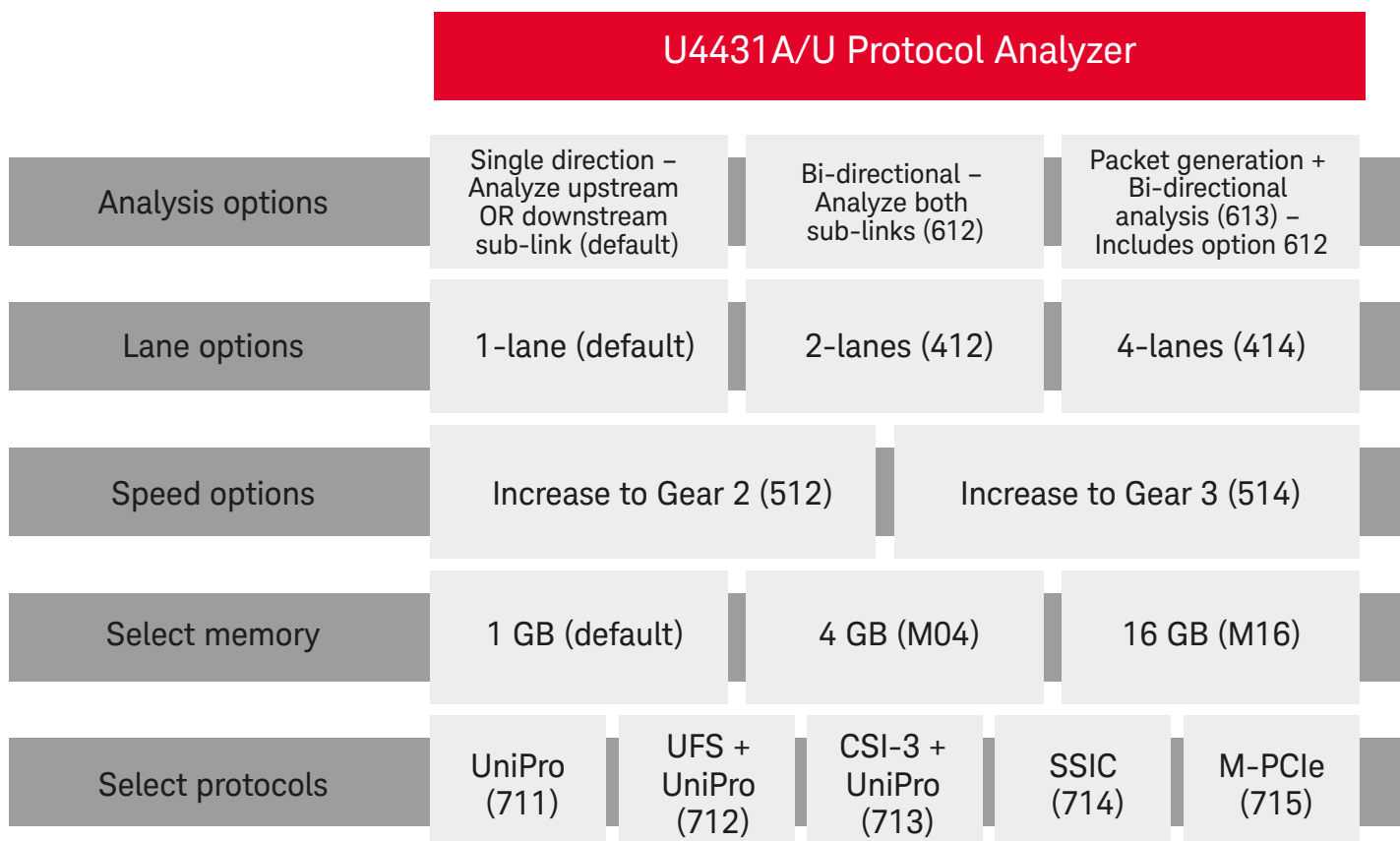
### Command Line Packet Generator

Protocol version support	
– UniPro	Unified Protocol (UniPro) 1.60
– UFS	Universal Flash Storage (UFS) 2.0 (JESD220B)
– Physical Layer	M-PHY 3.0
HS modes supported	G1 to G3
PWM data rates (Series A and B), Mbps	
– G0	0.9, 1.1
– G1	5.2, 6.1
– G2	10.4, 12.1
– G3	20.8, 24.3
– G4	41.6, 48.6
– G5	83.2, 97.2
– G6	166, 194
– G7	499, 583
Symbol lock time	
– HS-G1	1 symbol, typical
– HS-G2, HS-G3	< 128 symbols
Link width	1, 2, 3, or 4 links per sub-link
Link mapping	Manual width, static mapping
Traffic class	TCO
Preemption support	Not supported
CPort support	1
Automatic flow control	Not supported
Endpoint support	Host only
Timing control	Fixed prepare, sync, and sleep/stall idle time. User-defined idle between packets
Voltage control	LA/HA only
Error insertion	
– M-PHY	8b/10b, disparity
– UniPro	CRC, incorrect reserved bits
– UFS	User-defined payload via TCL script
User interface	User-defined TCL scripts with function library

### Environmental specifications

Radiated emissions (RE)	CISPR 11/EN55001	Group 1 Class A
Radiated immunity (RI)	EN/IEC 61000-4-3 frequency range at V/m	80 MHz to 2 GHz at 3 V/m; 2 to 2.7 GHz at 1 V/m
Electrostatic discharge	(EN/IEC 61000-4-2)+ discharge air/contact (kV)	8/4
Operating temperature	Operating range: Min-max (°C)	+5 to +40
Storage temperature	Storage range: Non-operating min-max (°C)	–40 to +70
Operating humidity	Max % RH at temperature °C	80 at 40
Storage humidity	Max % RH at temperature °C	90 at 65
Random vibration, Operating	5 to 500 Hz random, Grms	0.21
Random vibration, Survival	5 to 500 Hz random, Grms	2.09
Half sine shock	2 mS half sine delta velocity m/sec (in/sec)	1.6 (60)
Trapezoidal shock	24 mS trapezoidal delta velocity m/sec (in/sec)	8.00 (315)
Operating altitude	Kilo feet/kilo meters	10/3.1
Storage altitude	Non-operating (kilo feet/kilo meters)	15/4.6
Operating magnetic field immunity	A/m rms	30
Safety	IEC 61010-1 (3rd edition)	Single fault condition

## Module Configuration



## Chassis and Probing Configuration

<b>Chassis options</b>	
M9502A	2-slots
M9505A	5-slots
M9502A-020	USB 2.0 host connection for either chassis
M9505A-020	Lower-speed alternative to PC control options, not recommended for > 1 GB memory
<b>PC control options</b>	
M9536A	Embedded PC module (no cables or adapters needed)
<b>Connecting via PCIe to a desktop PC</b>	
M9048A	PCIe desktop adapter
Y1202A	PCIe cable (x8 to x8)
<b>Connecting via PCIe to a laptop PC</b>	
M9045A	ExpressCard adapter
Y1200B	PCIe cable (x4 to x8)
<b>Analyzer probes</b>	
U4432A	SMA cable, MIPI, M-PHY (one probe for each sub-link (analyzer))
U4433A <sup>1</sup>	Probe, ZIF flying leads, MIPI M-PHY (one probe for each sub-link (analyzer))
N5426A	ZIF tip for U4433A, 12 GHz InfiniiMax – Kit of 10
N4230A	SMA breakout board for U4432A

1. Recommended probe for most cases.





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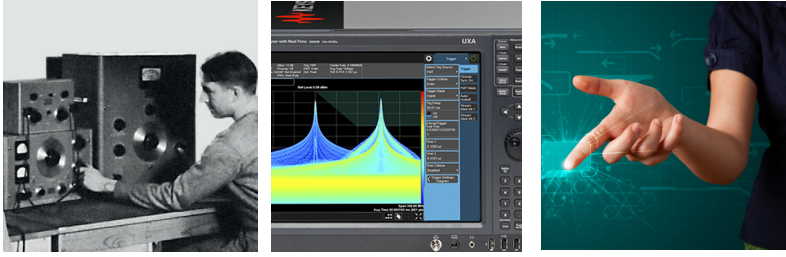


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