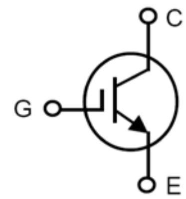
Advance Technical Information

High Voltage XPT™ IGBT

IXYF40N450

V_{CES} = 4500V
I_{C110} = 32A
$V_{CE(sat)}$ ≤ 3.9V

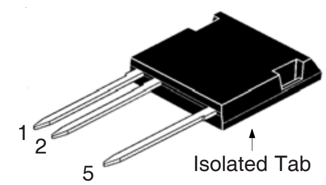
(Electrically Isolated Tab)



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_C = 25°C to 150°C	4500	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	4500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	T_C = 25°C	60	A
I_{C110}	T_C = 110°C	32	A
I_{CM}	T_C = 25°C, 1ms	350	A
SSOA (RBSOA)	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 10Ω Clamped Inductive Load	I_{CM} = 120 3600	A V
P_C	T_C = 25°C	290	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10 seconds	260	°C
F_C	Mounting Force	20..120 / 4.5..27	Nm/lb.in.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		5	g

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	4500			V
$V_{GE(th)}$	I_C = 250μA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			25	μA
	Note 2, T_J = 100°C		100		μA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±200	nA
$V_{CE(sat)}$	I_C = 40A, V_{GE} = 15V, Note 1		3.2	3.9	V
	T_J = 125°C		4.0		V

ISOPLUS i4-Pak™



1 = Gate
2 = Emitter
5 = Collector

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

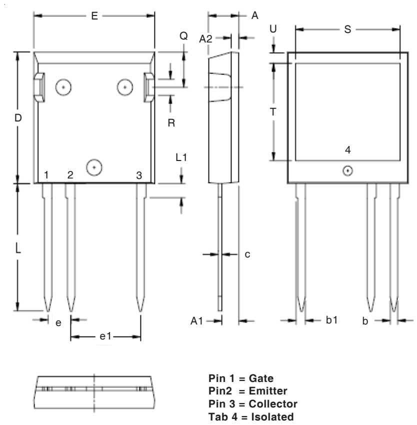
- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.
g_{fs}	I_C = 40A, V_{CE} = 10V, Note 1	18	30	S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		3550	pF
C_{oes}			146	pF
C_{res}			67	pF
Q_g	I_C = 40A, V_{GE} = 15V, V_{CE} = 1000V		170	nC
Q_{ge}			19	nC
Q_{gc}			70	nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C** I_C = 40A, V_{GE} = 15V, V_{CE} = 960V, R_G = 2Ω		36	ns
t_r			330	ns
$t_{d(off)}$			110	ns
t_f			1120	ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C** I_C = 40A, V_{GE} = 15V, V_{CE} = 960V, R_G = 2Ω		46	ns
t_r			740	ns
$t_{d(off)}$			118	ns
t_f			1010	ns
R_{thJC}				0.43 °C/W
R_{thCS}			0.15	°C/W

ISOPLUS i4-Pak™ (HV) Outline



Pin 1 = Gate
Pin2 = Emitter
Pin 3 = Collector
Tab 4 = Isolated

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

Notes:

1. Pulse test, t < 300μs, duty cycle, d < 2%.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

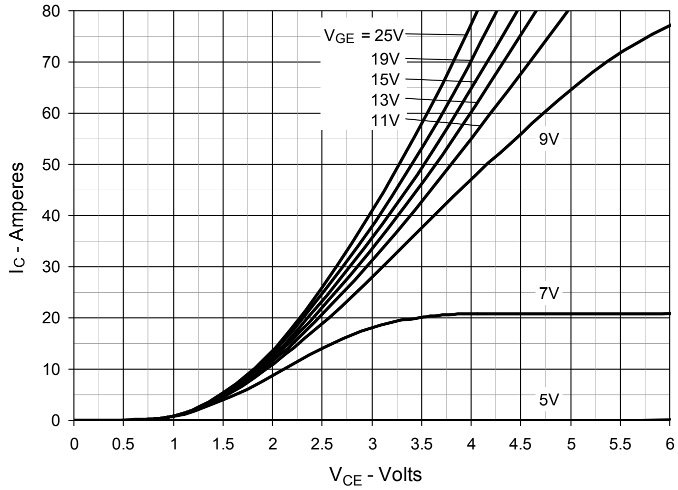


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

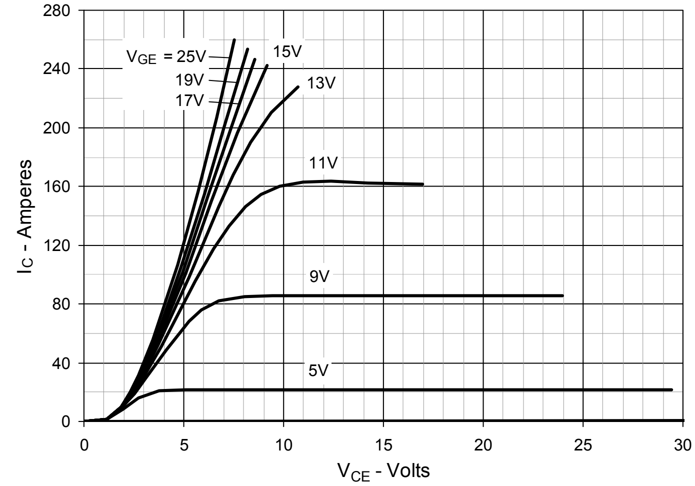


Fig. 3. Output Characteristics @ T_J = 125ºC

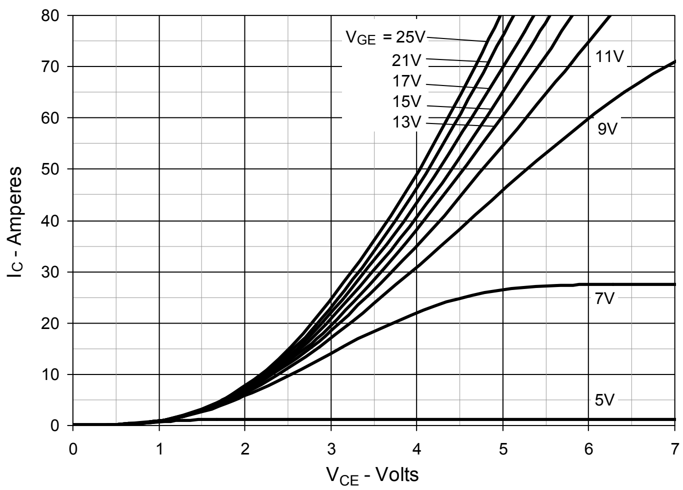


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

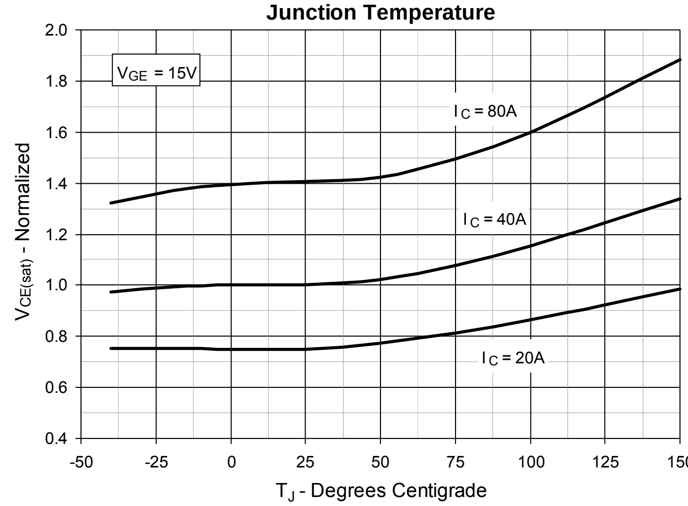


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

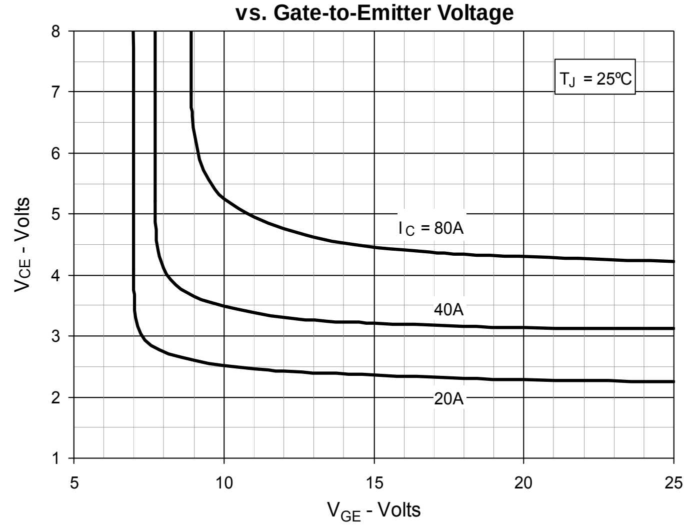


Fig. 6. Input Admittance

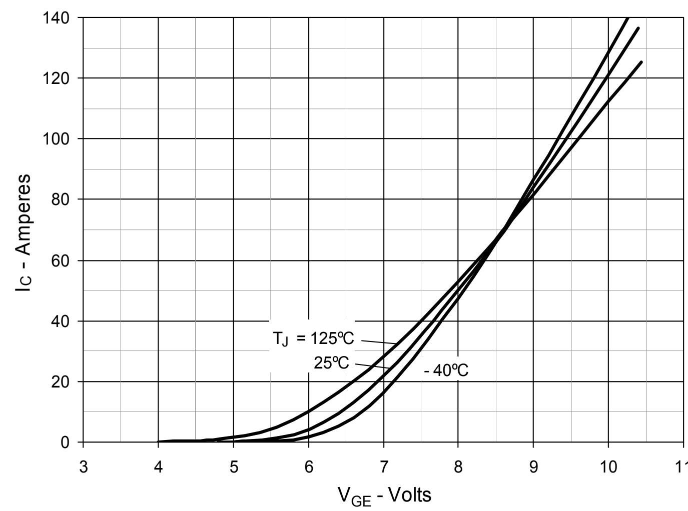


Fig. 7. Transconductance

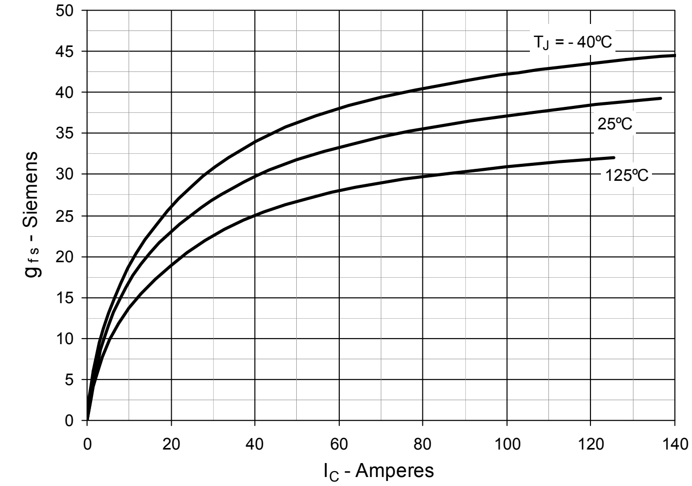


Fig. 8. Gate Charge

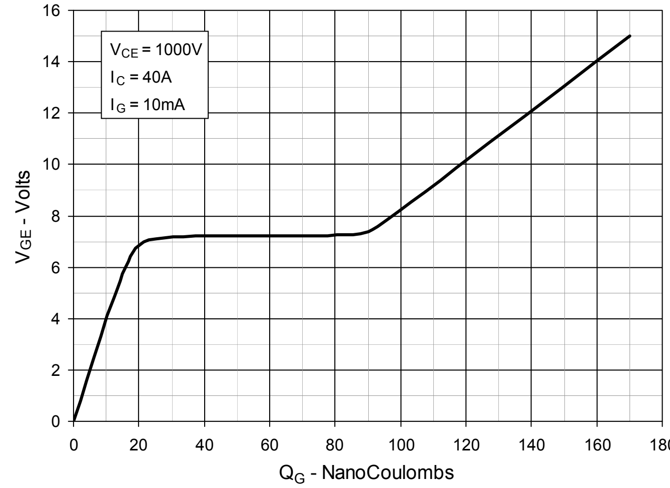


Fig. 9. Capacitance

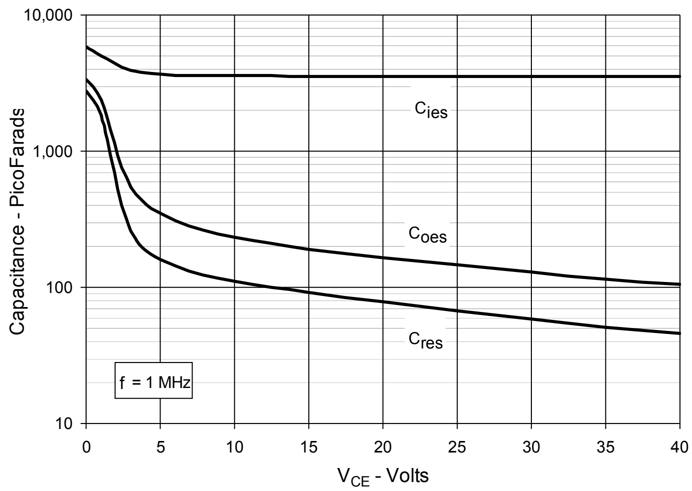


Fig. 10. Reverse-Bias Safe Operating Area

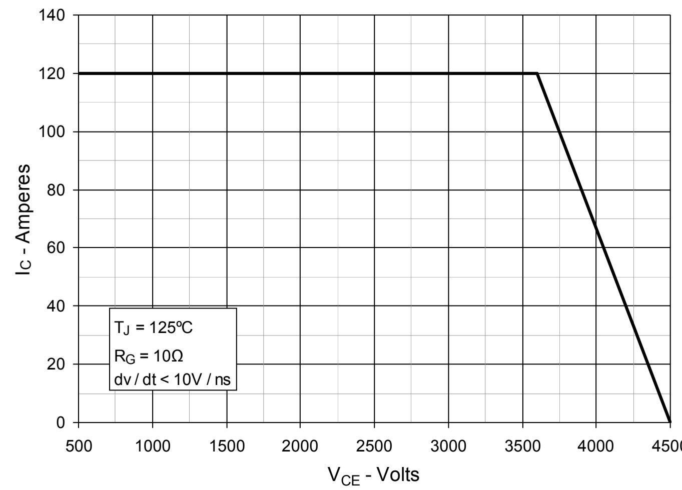
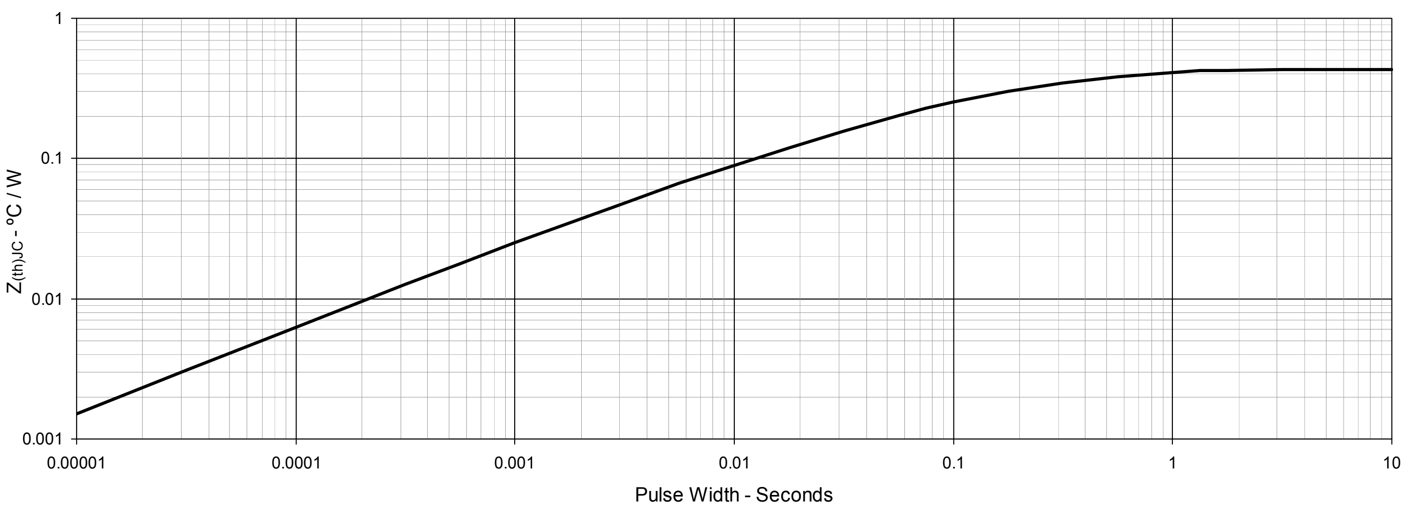


Fig. 11. Maximum Transient Thermal Impedance



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