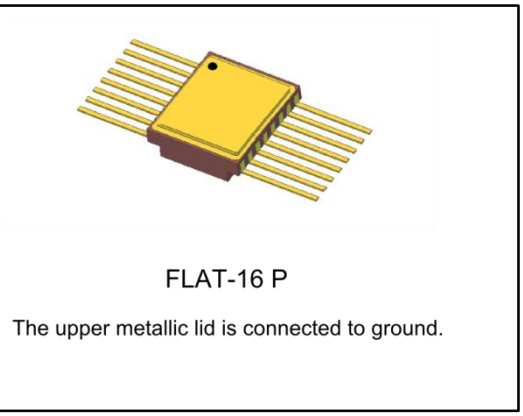
RHFL6000A

2 A rad-hard adjustable positive voltage regulator

Datasheet - preliminary data



FLAT-16 P

The upper metallic lid is connected to ground.

Features

- Input voltage range from 2.5 V to 12 V
- 2 A guaranteed output current
- Low dropout voltage: 0.3 V typ. @ 0.4 A
- Embedded overtemperature and overcurrent protection
- Adjustable overcurrent limitation
- Output overload monitoring/signalling
- Adjustable output voltage
- Internal control loop accessible via an external pin, optional
- Inhibit (ON/OFF) TTL compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Rad-hard: guaranteed up to 300 krad MIL-STD-883J Method 1019.9 high dose rate and 0.01 rad/s in ELDRS conditions
- Radiation environment (SET/SEL/SEB):
  - SEL free @ LET=120 MeV*cm2/mg
  - SET: less than 3.3% of V_{OUT} @ 120 MeV
- Heavy Ions SET dedicated internal circuitry implemented for absorbing output transient
- Operating junction temperature range: -55 °C to 125 °C

Description

The RHFL6000A high-performance adjustable positive voltage regulator provides exceptional radiation performance. It is tested in accordance with MIL-STD-883J Method 1019.9, in ELDRS conditions. The device is available in the FLAT-16P, a hermetic ceramic package, and the QML-V die is specifically designed for space and harsh radiation environments. A dedicated internal circuitry is implemented for absorbing output transients during SET events. The operating input voltage goes from 2.5 V to 12 V.

Table 1: Device summary

Device	Quality level	EPPL	Package	Lead finish	Mass (g)
RHFL6000AKP1	Engineering model	-	FLAT-16P	Gold	0.70
RHFL6000AKP01V (1)	QML-V Flight	Target			
RHFL6000AKP02V (1)	QML-V Flight	Target		Tin	

Notes:

(1)Qualification ongoing.

Contact ST sales office for information about the specific conditions for products in die form and other quality levels.

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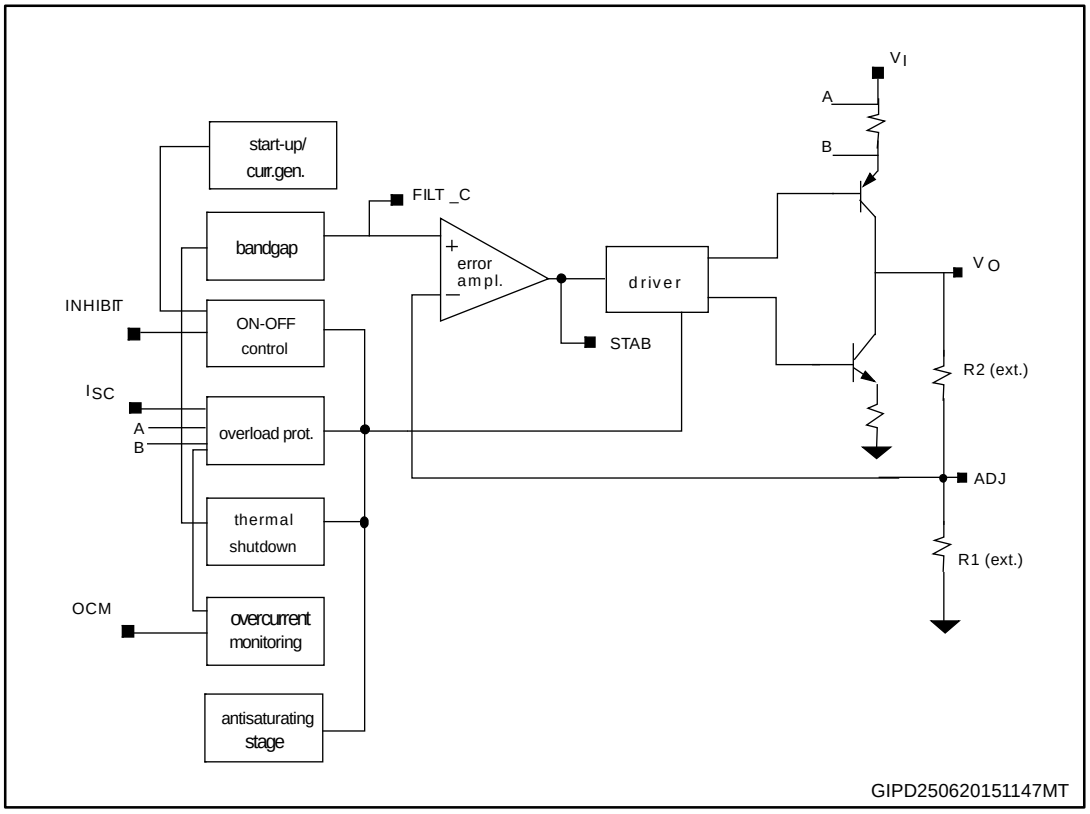
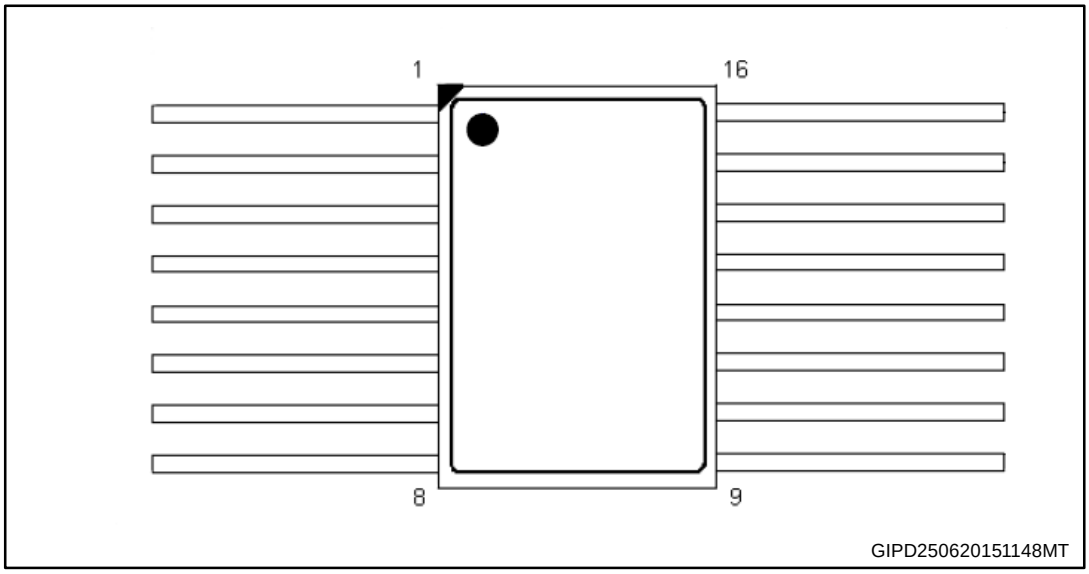
1 Diagram

Figure 1: Block diagram



2 Pin configuration

Figure 2: Pin configuration (top view)



The upper metallic package lid is connected to ground. The bottom metallization is electrically floating.

Table 2: Pin description

Pin name	FLAT-16P	Pin description
V_O(1)	1, 2, 6, 7	Output port of the regulator.
V_I(2)	3, 4, 5	Input port of the regulator.
GND	12, 13	Ground.
I_{SC}	8	Current limit setting pin. Connect a resistor between this pin and V_I to set the current limit threshold.
OCM	10	Overcurrent monitor flag. Open collector, internally pulled up. The signal on this pin goes to low logic level when the current limit activates.
INHIBIT	14	Device Inhibit pin. Internally pulled-down. The regulator is off when this pin is set at high logic level.
ADJ	15	Feedback pin. Connect to external resistor divider for output voltage setting.
FILT C	9	Filter capacitor pin. An optional capacitor can be connected between this pin and GND.
STAB	11	An optional R-C network can be connected between this pin and GND to tune the internal control loop.
NC	16	Not internally connected.

Notes:

(1)All the output pins must be connected together on the PCB.

(2)All of input pins must be connected together on the PCB.

The upper metallic package lid is connected to ground. The bottom metallization is electrically floating.

3 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage, V_I-V_{GROUND}	-0.3 to 12	V
V_O	DC output voltage range	-0.3 to (V_I + 0.3)	V
V_{ADJ}	Adjustable pin voltage	-0.3 to (V_O + 0.3)	V
I_O	Continuous output current	2	A
V_{OCM}	Over current monitor pin voltage vs GND	-0.3 to 12	V
V_{ISC}	Current limit pin voltage vs GND	-0.3 to 12	V
INHIBIT	Inhibit pin voltage	-0.3 to 12	V
STAB	Stability capacitor pin voltage	-0.3 to 2.5	V
FILT C	Filter capacitor pin voltage	-0.3 to 1.3	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{OP}	Operating junction temperature range	-55 to +125	°C
ESD	Human body model (HBM)	2	kV
	Machine model (MM)	200	V
	Charged device model (CDM)	500	V

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case, FLAT-16P	8.3	°C/W
T_{SOLD}	Maximum soldering temperature, 10 s	300	°C

4 Electrical characteristics

T_J = 25 °C, V_I = 2.5 V, V_O = V_{ADJ}, C_I = C_O = 10 µF (tantalum), unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage	I_O = 1 A, T_J = -55 to 125 °C	2.5		12	V
V_{ADJ}	Reference voltage	I_O = 5 mA to 1 A, V_O = V_{adj}, T_J = -55 to 125 °C	1.205	1.245	1.285	V
I_{SHORT}	Output current limit (1)	Adjustable by external resistor	1	3		A
$\Delta V_O/\Delta V_I$	Line regulation	V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = +25 °C		0.1	0.4	%
		V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = -55 °C		0.2	0.5	
		V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = +125 °C		0.08	0.35	
$\Delta V_O/\Delta I_O$	Load regulation	V_I = 2.5 V, I_O = 5 to 400 mA, T_J = +25 °C		0.02	0.4	%
		V_I = 2.5 V, I_O = 5 to 400 mA, T_J = -55 °C		0.2	0.5	
		V_I = 2.5 V, I_O = 5 to 400 mA, T_J = +125 °C		0.03	0.3	
		V_I = 2.5 V, I_O = 5 mA to 1 A, T_J = +25 °C		0.3	0.5	
		V_I = 2.5 V, I_O = 5 mA to 1 A, T_J = -55 °C		0.3	0.6	
		V_I = 2.5 V, I_O = 5 mA to 1 A, T_J = +125 °C		0.3	0.6	
		V_I = 2.5 V, I_O = 5 mA to 2 A, T_J = -55 to 125 °C		0.6		
Z_{OUT}	Output impedance	I_O = 100 mA DC and 20 mA rms		100		mΩ
I_q	Quiescent current (2) ON mode	V_I = 2.5 V to 12 V, I_O = 5 mA, T_J = +25 °C			7	mA
		V_I = 2.5 V to 12 V, I_O = 30 mA, T_J = +25 °C			7	
		V_I = 2.5 V to 12 V, I_O = 300 mA, T_J = +25 °C			30	
		V_I = 2.5 V to 12 V, I_O = 1 A, T_J = +25 °C			60	
		V_I = 2.5 V to 12 V, I_O = 30 mA, T_J = -55 °C			7	

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
		V_I = 2.5 V to 12 V, I_O = 300 mA, T_J = -55 °C				35	
		V_I = 2.5 V to 12 V, I_O = 1 A, T_J = -55 °C				80	
		V_I = 2.5 V to 12 V, I_O = 30 mA, T_J = +125 °C				7	
		V_I = 2.5 V to 12 V, I_O = 300 mA, T_J = +125 °C				30	
		V_I = 2.5 V to 12 V, I_O = 1 A, T_J = +125 °C				60	
I_{qOFF}	Quiescent current OFF mode	V_I = 2.5 V, V_{INH} = 2.4 V, OFF mode, T_J = -55 to +125 °C			0.2	1	mA
V_d	Dropout voltage	I_O = 400 mA, V_O = 2.5 to 9 V, (+25 °C)			300	450	mV
		I_O = 400 mA, V_O = 2.5 to 9 V, (-55 °C)			250	400	
		I_O = 400 mA, V_O = 2.5 to 9 V, (+125 °C)			350	550	
		I_O = 1 A, V_O = 2.5 to 9 V, (+25 °C)			570	800	
		I_O = 1 A, V_O = 2.5 to 9 V, (-55 °C)			470	700	
		I_O = 1 A, V_O = 2.5 to 9 V, (+125 °C)			700	900	
		I_O = 2 A, V_O = 2.5 to 9 V, (+25 °C)			550		
		I_O = 2 A, V_O = 2.5 to 9 V, (-55 °C)			500		
		I_O = 2 A, V_O = 2.5 to 9 V, (+125 °C)			700		
$V_{INH(ON)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125 °C				0.8	V
$V_{INH(OFF)}$	Inhibit voltage	I_O = 5 mA, T_J = -55 to +125 °C		2.4			
SVR	Supply voltage rejection (3)	V_I = V_O + 2.5 V ± 0.5 V, V_O = 3 V I_O = 5 mA	f = 120 Hz	60	70		dB
			f = 33 Hz	30	40		
I_{SH}	Shutdown input current	V_{INH} = 5 V			15		µA
V_{OCM}	OCM pin voltage	Sinked I_{OCM} = 24 mA active low			0.38		V
t_{PLH}	Inhibit propagation delay, turn-off (3)	V_I = V_O + 2.5 V, V_{INH} = from 0 V to 2.4 V, I_O = 400 mA , V_O = 3 V, C_I = C_O = 10 µF				30	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PHL}	Inhibit propagation delay, turn-on (3)	$V_I = V_O + 2.5$ V, V_{INH} = from 2.4 V to 0 V, I_O = 400 mA , V_O = 3 V, $C_I = C_O$ = 10 µF			100	µs
eN	Output noise voltage (3)	B = 10 Hz to 100 kHz, I_O = 5 mA to 2 A		40		µVrms

Notes:

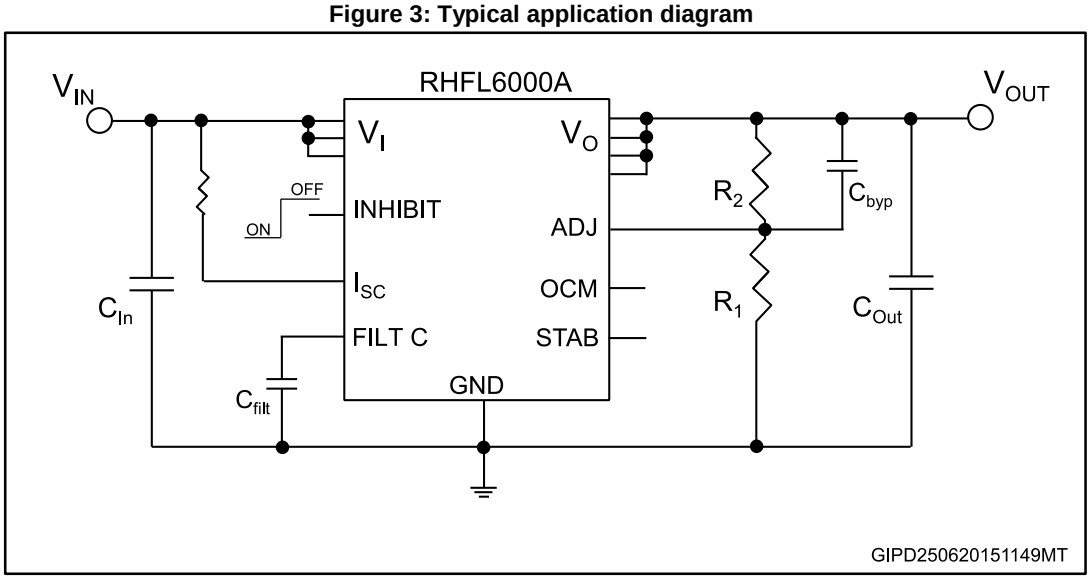
(1)These values are guaranteed by design. For each application it is strongly recommended to comply with the maximum current limit of the package used.

(2)See *Table 6: "Tid tests results"*.

(3)These values are guaranteed by design.

5 Typical application diagram

Figure 3: Typical application diagram



6 Radiations

6.1 Total ionizing dose (MIL-STD-883 test method 1019)

The products that are guaranteed in radiation within RHA QML-V system, fully comply with the MIL-STD-883 test method 1019 specification. The RHFL6000A is being RHA QML-V qualified, tested and characterized in full compliance with the MIL-STD-883 specification, both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

- Testing is performed in accordance with MIL-prf-38535 and the test method 1019 of the MIL-STD-883 for total ionizing dose (TID).
- ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Table 6: TID tests results

Type	Conditions	Value	Unit
TID	50 rad(Si)/s high dose rate up to	300	krad
	10 mrad(Si)/s low dose rate up to (1)	100	
	ELDRS free up to (1)	100	
Output voltage radiation drift	From 0 krad to 300 krad at 50 rad/s , MIL-STD-883J method 1019.9	<1.1	ppm/krad
Quiescent current (ON state)	From 0 krad to 300 krad at 50 rad/s , MIL-STD-883J method 1019.9 V_I = 2.5 V to 12 V, I_O = 5 to 30 mA, T_J = -55 to +125 °C	<15	mA

Notes:

(1)300 krad low dose rate test ongoing.

6.2 Heavy Ions

The heavy ions trials are performed on qualification lots only. No additional test is performed. Table 7 summarizes the results of heavy ions tests.

Table 7: Heavy ions results

Feature	Conditions	Value	Unit
SEL/B performance	LET = 120 MeV*cm^2/mg V_I = 12 V	No latchup/burnout	-
SET performance during events	LET = 32 MeV*cm2/mg Saturated cross-section = 6.18*10^{-5} cm² V_{IN} up to 9 V V_I - V_O ≤ 7.5 V I_{OUT} < 300 mA	± 15% max over less than 300 ns	% of V_O
	LET = 120 MeV*cm2/mg V_{IN} up to 12 V V_I - V_O < 3.0 V I_{OUT} < 300 mA	No SET above ± 3%	
	LET = 120 MeV*cm2/mg V_{IN} up to 4 V V_I - V_O < 1.5 V I_{OUT} < 1 A	No SET above ± 3.3%	

SEL and SET performances described here below are related to the circuit configuration and bias conditions shown in *Figure 4: "Heavy Ion test configuration"* and *Table 8: "Bias configurations"* and *Table 9: "Test configurations"*.

Figure 4: Heavy Ions test configuration

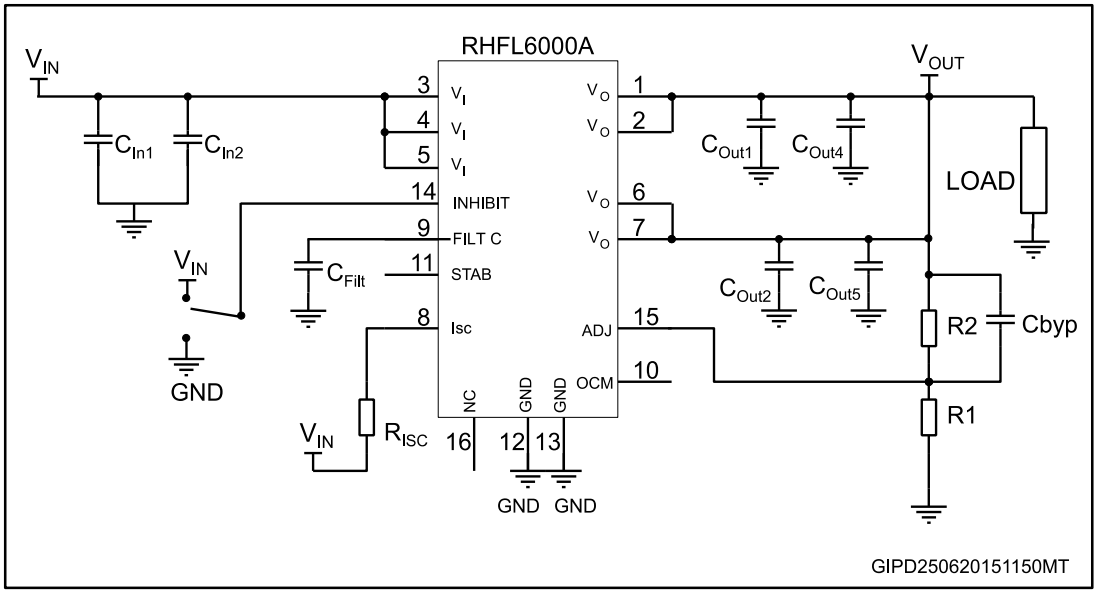


Table 8: Bias configurations

Test mode	Bias condition
SEL	V_{IN} = 12 V, V_{OUT} = 9 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 5 mA
SET	V_{IN} = 3 V, V_{OUT} = 1.5 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 1 mA
	V_{IN} = 9 V, V_{OUT} = 0 V, $V_{INHIBIT}$ = 9 V, I_{OUT} = 0 mA
	V_{IN} = 4 V, V_{OUT} = 2.5 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 1 A
	V_{IN} = 7 V, V_{OUT} = 5 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 300 mA
	V_{IN} = 12 V, V_{OUT} = 9 V, $V_{INHIBIT}$ = 0 V, I_{OUT} = 300 mA

Table 9: Test configurations

Test mode	Test configuration	
SEL	Sel configuration	C_{IN1} = 100 µF
		C_{OUT1} = C_{OUT2} = 47 µF
		C_{IN2} = C_{OUT4} = C_{OUT5} = 100 nF
		C_{byp} = 47 nF
		C_{filt} = 22 nF
		R_{ISC} = 8.2 kΩ
		R_{load} = 1.8 kΩ
SET	SET 1	C_{IN1} = 100 µF
		C_{OUT1} = C_{OUT2} = 47 µF
		C_{IN2} = C_{OUT4} = C_{OUT5} = 100 nF
		C_{byp} = 47 nF
		C_{filt} = 22 nF
		R_{ISC} = 8.2 kΩ
		R_{load} = depending on bias conditions
	SET 2	C_{IN1} = C_{OUT1} = 220 µF
		C_{OUT5} = C_{OUT2} = not connected
		C_{IN2} = C_{OUT4} = 100 nF
		C_{byp} = 47 nF
		C_{filt} = 22 nF
		R_{ISC} = 8.2 kΩ
		R_{load} = depending on bias conditions

7 Additional guidelines for SET mitigation

This section provides detailed design guidelines necessary to obtain the required performance against SET. In this respect, we can identify two main areas for intervention: ground connection and external components selection.

7.1 Ground connections

To achieve the best performance in terms of output voltage accuracy, noise immunity and robustness against single event effects, it is recommended to implement a proper PCB layout by following the suggestions described below.

According to qualitative simulations of single events, some very short SET (i.e., a duration in the 100 ns range) are strongly dependent on the stray inductances versus GND. The best solution to reduce the parasitic inductance is the adoption of a GND plane (with separate power and sense paths where possible). By minimizing the stray GND impedance, this approach is of great assistance in controlling the amplitude of the SET events near the load.

If this solution is not applicable, we suggest using a star-bus topology, where the PCB reference GND connection is close to the GND pin of the regulator.

To achieve a good GND sense, it is necessary to comply with the following rules:

- connect the regulator GND pin and load GND node both to the sense and power GND traces on the PCB using vias to minimize the path;
- an array of multiple via structures works better than a single large one;
- for GND connectors/plugs: use separate plugs for power supply and testing probes;
- connect input/output capacitors GND terminals to GND sense on the PCB.

7.2 Capacitor selection

With reference to *Figure 4: "Heavy Ion test configuration"*, a combination of capacitors must be present on the input and output ports. For the INPUT terminals, this may consist of a 100 µF bulk capacitor (C_{IN1}) in parallel with a polyester 100 nF one (C_{IN2}) used for decoupling purposes.

For each of the two OUTPUT connections (pins 1, 2 and 6, 7) we suggest using a combination of a 47µF bulk capacitor ($C_{OUT1,}$ $C_{OUT2,}$) in parallel with a polyester 100 nF one ($C_{OUT4,}$ C_{OUT5}) for decoupling purposes.

Regarding parts selection, for the 100 nF elements we suggest low-ESL and low ESR capacitors.

Concerning the selection of the three bulk capacitors, we suggest:

- using tantalum SMD;
- selecting size and ESL as small as possible;
- placing capacitors as close as possible to the input/output terminals;
- using an array of capacitors in parallel, where possible. This works better than a single capacitor against the short events.

8 Device description

The RHFL6000A adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the internal temperature-compensated band-gap and the fraction of the desired output voltage value obtained from an external resistor divider bridge. The device is protected by several functional blocks.

8.1 ADJ pin

The feedback voltage necessary for the loop regulation comes from the load through an external resistor divider (R1, R2 as in *Figure 3: "Typical application diagram"*) whose mid point is connected to the ADJ pin (allowing all possible output voltage settings as per user requirements).

8.2 Inhibit ON-OFF control

By setting the INHIBIT pin to TTL high level , the device switches off. The device is in ON state when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating whenever the inhibit function is not used.

8.3 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device turns off when a temperature of approximately 175 °C is reached, returning to ON mode when the temperature decreases down to approximately 135 °C.

It should be noted that when the internal temperature detector reaches 175 °C, the active power element can be as high as 225 °C. Prolonged operation under these conditions may exceed the maximum operating ratings and device reliability cannot be guaranteed.

8.4 Overcurrent protection

An default internal costant current limit is set at I_{SHORT} = 3 A (when V_O is at 0 V).

This value can be decreased via an external resistor (R_{SHORT}) connected between the I_{SC} and V_I pins, with a typical value range of 10 kΩ to 200 kΩ.

To maintain optimal regulation, it is necessary to set I_{SHORT} 1.6 times greater than the desired maximum operating current (I_O). When I_O reaches I_{SHORT}–300 mA, the current limiter intervenes, V_O starts to drop and the OCM flag is raised. When no current limitation adjustment is required, the I_{SC} pin must be left unbiased.

The combination of overcurrent and overtemperature circuits provides RHFL6000A with a high level of protection against destructive junction temperature excursions in all load conditions.

8.5 OCM pin

The OCM pin is an open collector flag normally pulled up at V_I by a 5 kΩ resistor.

It goes to low state when the current limit becomes active. It is buffered and can sink 10 mA.

8.6 STAB pin

The STAB pin gives user direct access to regulator internal control loop stability adjustment. Its usage is optional and it should be left unconnected when not used.

8.7 FILT C pin

The FILT C pin helps reduce SET rate when bypassed to GND through a 22 nF ceramic capacitor. Its usage is optional and it should be left unconnected when not used.

9 Application information

To adjust the output voltage, the R2 resistor must be connected between the V_O and ADJ pins. The R1 resistor must be connected between ADJ and ground. Resistor values can be derived from the following formula:

$$V_O = V_{ADJ} (R1+ R2) / R1$$

where

$$V_{ADJ} = 1.248 \text{ V typ.}$$

The minimum output voltage is therefore V_{ADJ} and minimum input voltage is 2.5 V.

The RHFL6000A operates correctly when the V_I - V_O voltage difference is slightly above the power element saturation voltage (V_d, dropout voltage).

A minimum load current of 0.5 mA must be set to ensure proper regulation under no-load condition. It is advisable to make this current flow into the resistor divider.

For this reason, we suggest selecting an R1 value not higher than 10 k Ω.

The RHFL6000 flat16 package offers multiple input and output pins.

All of the available V_I pins should always be externally interconnected. The same must be applied to all the available V_O pins, otherwise the stability and reliability of the device cannot be guaranteed.

The inhibit function switches off the output current very quickly. According to Lenz's Law, external circuitry reacts with LdI/dt terms which can be of high amplitude in case of serial inductive elements or large stray PCB inductance. Large transient voltage would develop on both device terminals. It is advisable to protect the device output with Schottky diodes to prevent negative voltage excursions. A14 V Zener diode could protect the device input.

The input and output capacitors must be connected as close as possible to the device terminals.

Since the RHFL6000A voltage regulator is manufactured with very high speed bipolar technology (6 GHz f_T transistors), the PCB layout must be designed with exceptional care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation.

On the other hand, the benefit of this technology is SVR performance extended to high frequencies.

9.1 Notes on the 16-pin hermetic flat package

The RHFL6000A adjustable voltage regulator is available in a high thermal dissipation 16-pin hermetic Flat package, whose bottom flange is metallized to allow direct soldering or glueing to a heat sink (efficient thermal conductivity). The upper metallic package lid is connected to ground. The bottom metallization is electrically floating.

9.2 FPGA supply

FPGA devices are very sensitive to VDD transients beyond a few % of their nominal supply voltage (usually 1.5 V).

The RHFL6000A includes specific integrated circuitry designed to absorb the output transients under heavy ion beams, rendering it suitable for safe FPGA supply operation.

10 Typical performance characteristics

(C_{IN} = C_{OUT} = 10 µF tantalum, unless otherwise specified)

Figure 5: Output voltage vs temperature (V_{IN} = 2.5 V, I_{OUT} = 5 mA)

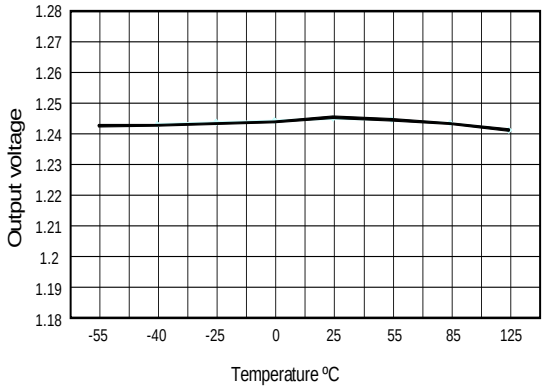


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Figure 6: Output voltage vs temperature (V_{IN} = 2.5 V, I_{OUT} = 400 mA)

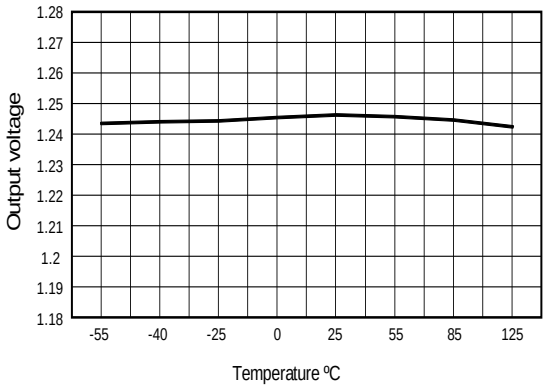

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Figure 7: Output voltage vs temperature (V_{IN} = 2.5 V I_{OUT} = 1 A)

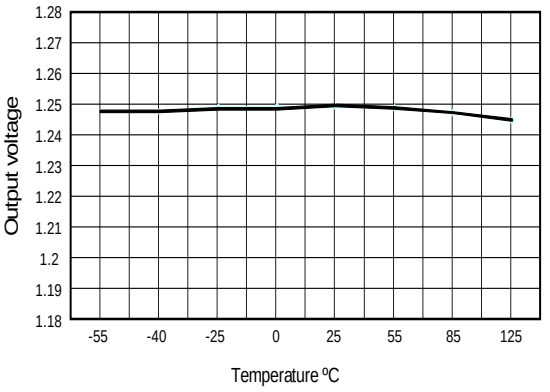

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Figure 8: Output voltage vs temperature (V_{IN} = 2.5 V I_{OUT} = 2 A)

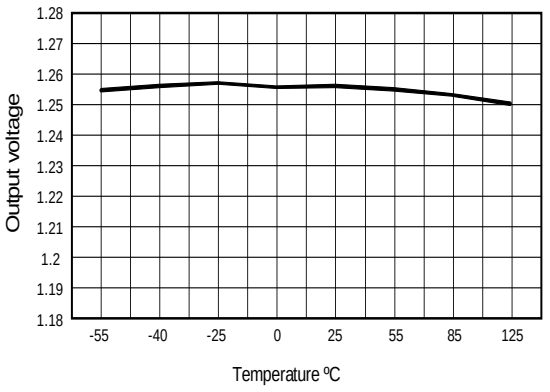

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Figure 9: Line regulation vs temperature

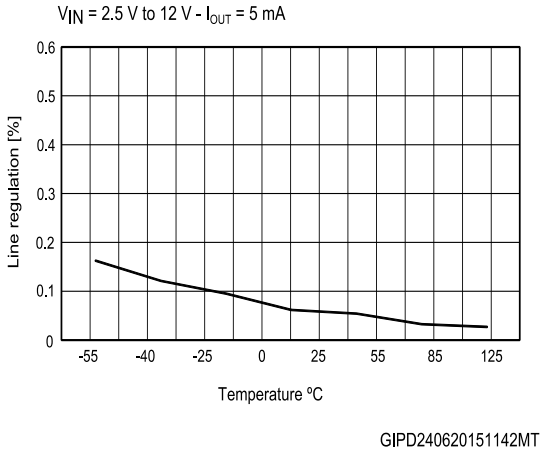

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Figure 10: Load regulation vs temperature (I_{OUT} = 5 mA to 400 mA)

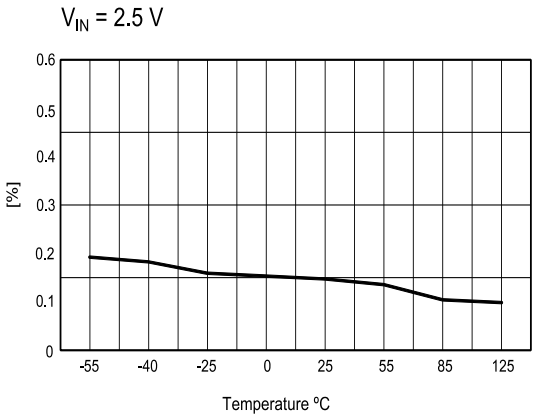

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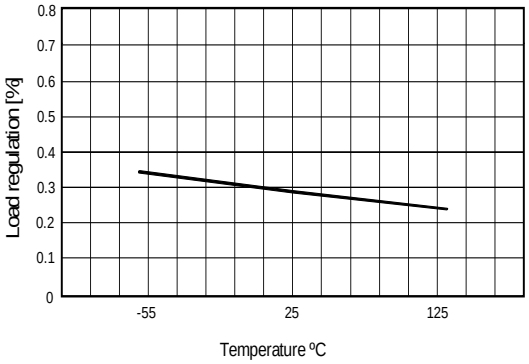
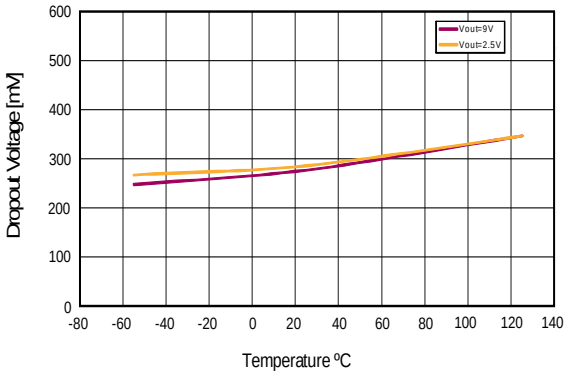
Figure 11: Load regulation vs temperature (I_{OUT} = 5 mA to 1 A, V_{IN} = 2.5 V



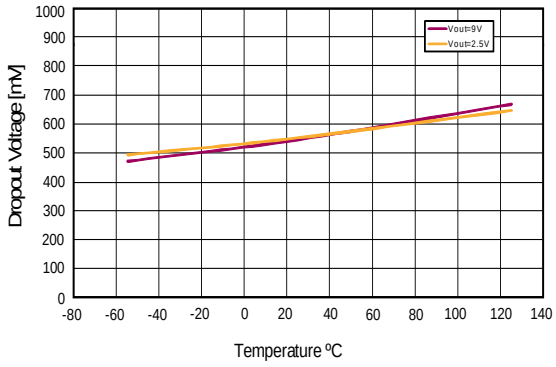
GIPD240620151125MT

Figure 12: Dropout voltage vs. temperature (I_{OUT} = 0.4 A)



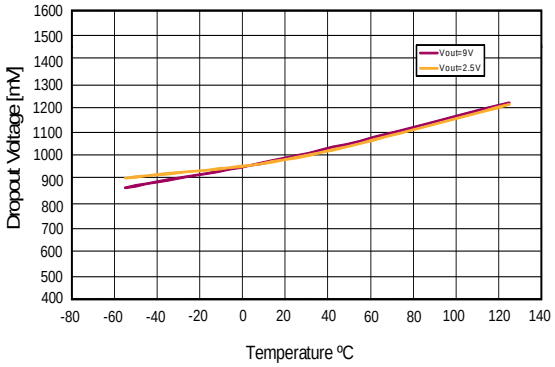
GIPD290620151104MT

Figure 13: Dropout voltage vs temperature (I_{OUT} = 1 A)



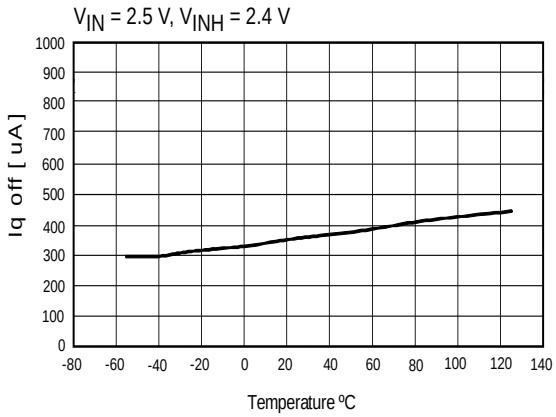
GIPD240620151103MT

Figure 14: Dropout voltage vs temperature (I_{OUT} = 2 A)



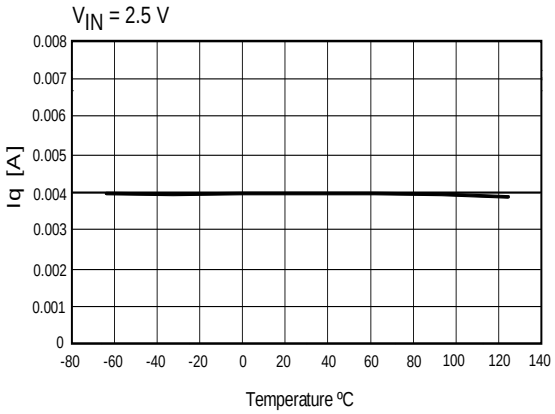
GIPD230620151454MT

Figure 15: Quiescent current (OFF mode)



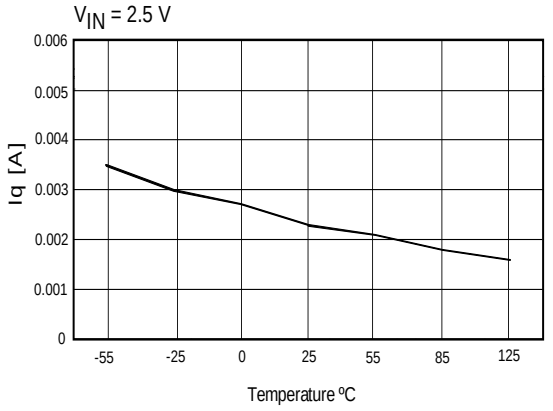
GIPD230620151442MT

Figure 16: Quiescent current (ON mode, I_{OUT} = 5 mA)



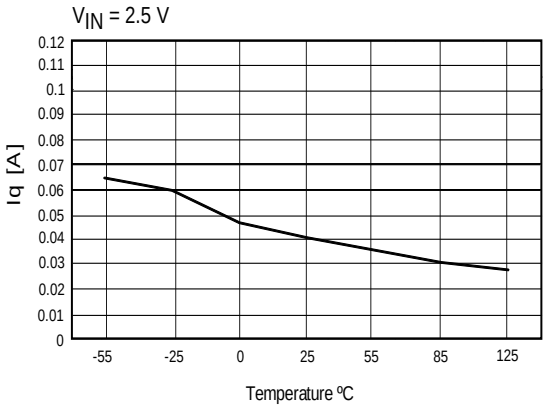
GIPD230620151432MT

Figure 17: Quiescent current (ON mode, I_{OUT} = 1 A)



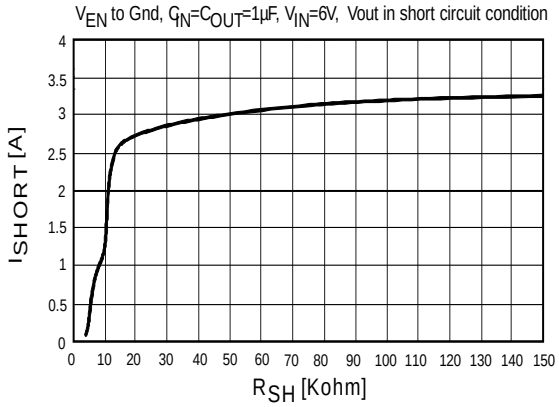
GIPD230620151152MT

Figure 18: Quiescent current (ON mode, I_{OUT} = 2 A)



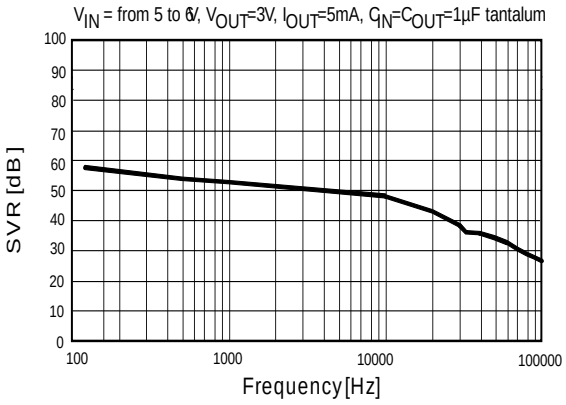
GIPD260620151051MT

Figure 19: Short circuit current vs R_{SHORT}



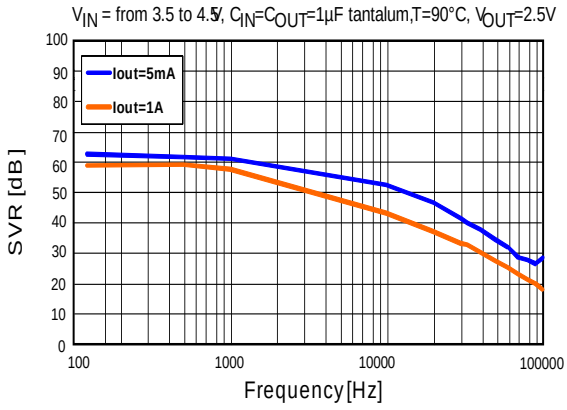
GIPD230620151141MT

Figure 20: SVR vs frequency



GIPD230620151129MT

Figure 21: SVR vs frequency (T = 90 °C)



GIPD230620151047MT

Figure 22: Turn on transient

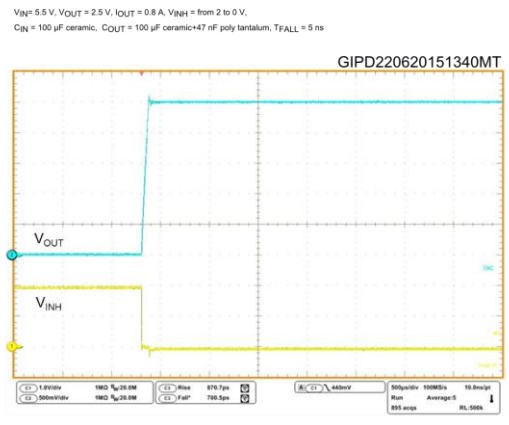


Figure 23: Turn off transient

V_{IN} = 5.5 V, V_{OUT} = 2.5 V, I= 0.8 A, V_{INH} = from 0 to 2 V,
C_{IN} = 100 µF ceramic, C_{OUT} = 100 µF ceramic+47 nF poly tantalum, T_{RISE} = 5 ns

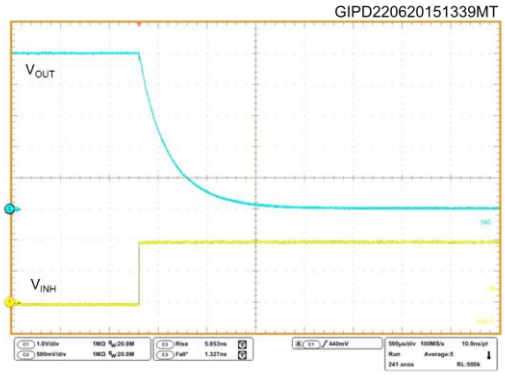


Figure 24: Line transient (I_{OUT} = 0.8 A, V_{OUT} = 3 V)

V_{INH} to Gnd, V_{IN}= from 5 V to 12 V and vice versa No C_{IN}, C_{OUT} = 10 µF tantalum

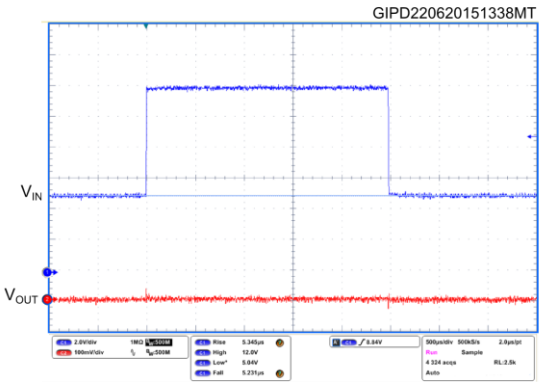


Figure 25: Line transient (I_{OUT} = 2 A, V_{OUT} = 2.5 V)

V_{INH} to Gnd, V_{IN}= from 5 V to 2 V and vice versa I_{OUT} = 2 A, No C_{IN}, C_{OUT} = 10 µF tantalum V_{OUT}= 2.5 V

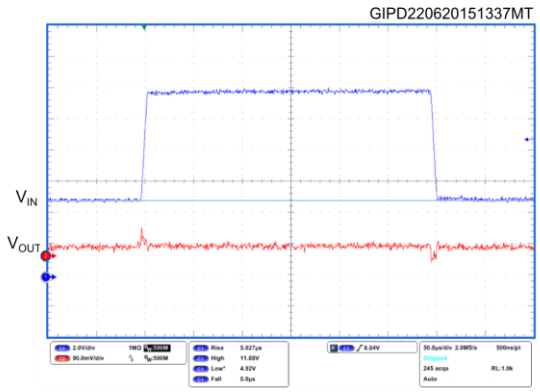


Figure 26: Load transient

V_{IN}= 5 V, I_{OUT}= from 5 mA to 2 A and vice versa, C_{IN} = C_{OUT} = 10 µF tantalum V_{OUT}= 1.24 V

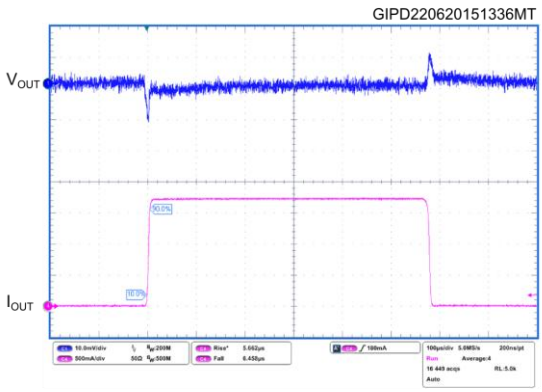


Figure 27: Stability area for ceramic capacitor

C_{IN} = 22 µF, V_{IN} = from 2.5 V to 12 V, I_{OUT} = from 10 mA to 2 A, V_{OUT} = 1.24 V, no C_{byp}, no C_{filter}

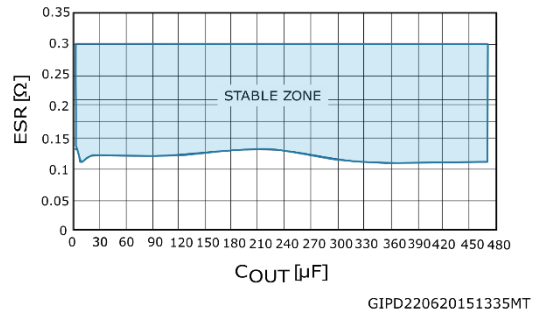
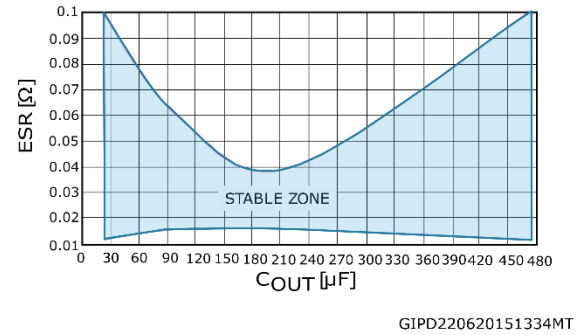


Figure 28: Stability area for tantalum capacitor

C_{IN} = 1 µF, V_{IN} = from 2.5 V to 12 V, I_{OUT} = from 10 mA to 2 A, V_{OUT} = 1.24 V, no C_{byp}, no C_{filter}



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

11.1 FLAT-16P package information

Figure 29: Flat-16P package outline

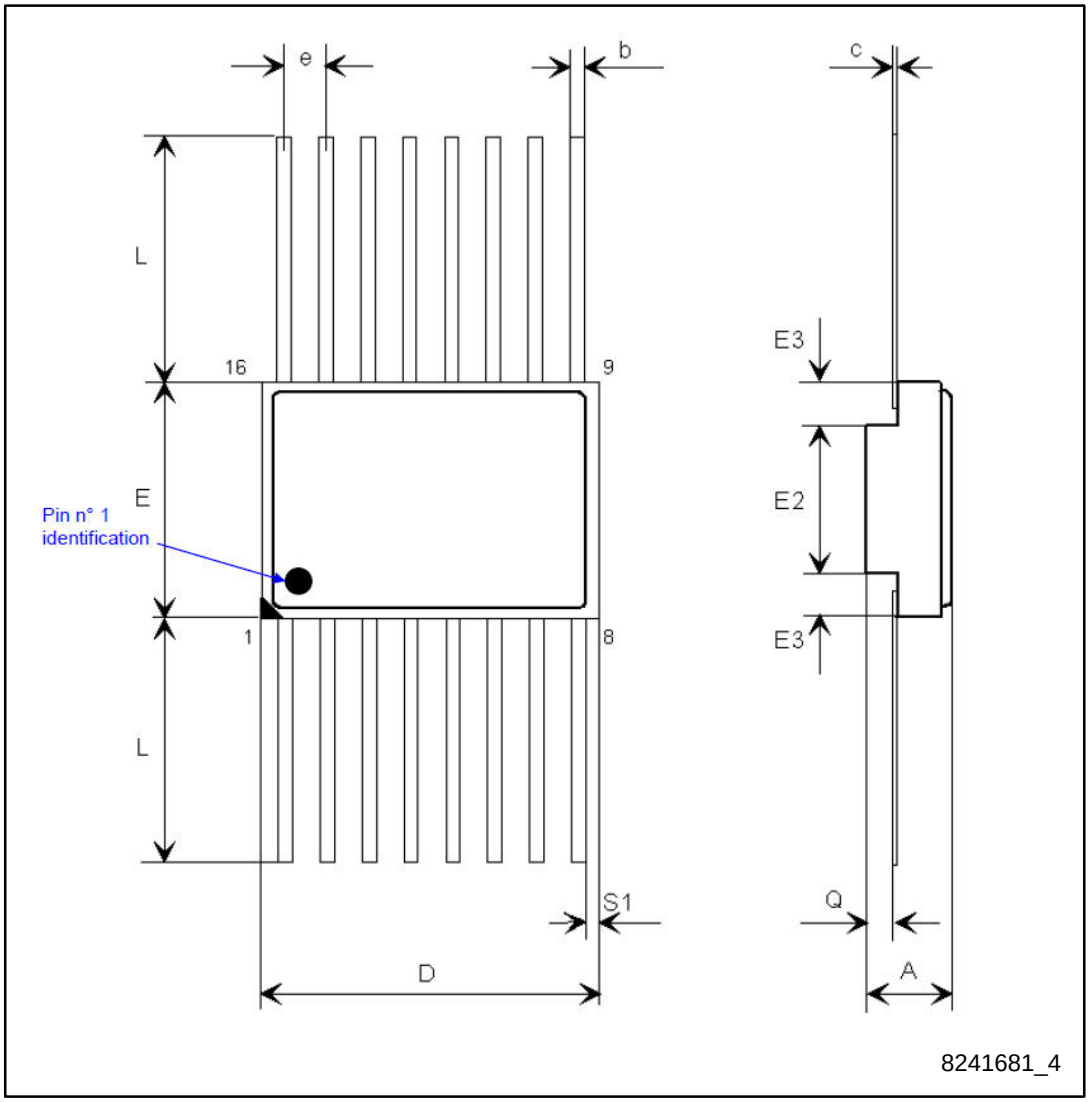


Table 10: Flat-16P package mechanical data

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.42		2.88	0.095		0.113
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.71		10.11	0.382		0.398
E	6.71		7.11	0.264		0.280
E2	3.30	3.45	3.60	0.130	0.136	0.142
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

12 Ordering information

Table 11: Order code

CPN	Quality level	EPPL	Package	Lead finish	Marking (1)	Packing
RHFL6000AKP1	Engineering model	-	FLAT-16P	Gold	RHFL6000KPA1	Strip pack
RHFL6000AKP01V (2)	QML-V flight	Target	FLAT-16P	Gold	TBD	Strip pack
RHFL6000AKP02V (2)	QML-V flight	Target	FLAT-16P	Tin	TBD	Strip pack

Notes:

(1)Specific marking only. The full marking includes in addition: - for the engineering models : ST logo, date code, country of origin (FR) - for QML flight parts : ST logo, date code, country of origin (FR), manufacturer code (CSTM), serial number of the part within the assembly lot.

(2)Qualification ongoing.

Contact ST sales office for information about the specific conditions for :

1) Products in die form

2) Other quality levels

3) Tape & reel packing

12.1 Traceability information

Date code in formation is structured as described below:

Table 12: Date codes

Model	Datecode
EM	3yywwN
QML flight	yywwN

where:

- yy = year
- ww = week number
- N = lot index in the week

12.3 Documentation

The table below gives a summary of the documentation provided with each type of products:

Table 13: Table of documentation by product

Quality level	Documentation
Engineering model	-
QML-V flight	Certificate of conformance (including group C & D reference) Precap report (100% high & low magnification) SEM report Screening summary Group A summary (quality conformance inspection of electrical tests) Group B summary (quality conformance inspection of mechanical tests) Group E (quality conformance inspection of wafer lot radiation verification test)

13 Revision history

Table 14: Document revision history

Date	Revision	Changes
21-Sep-2015	1	First release.
12-Oct-2015	2	Updated *Table 7: "Heavy ions results"*. Minor text changes.

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