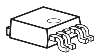
5-V Low Drop Voltage Regulator

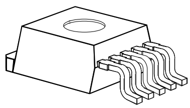
TLE 7272

Features

- Output voltage 5 V ±2%
- Ultra low current consumption: typ. 25µA
- 300 mA current capability
- Inhibit input
- Reset
- Very low-drop voltage
- Short-circuit-proof
- Suitable for use in automotive electronics



P-TO252-5-1



P-TO263-5-1

Functional Description

The TLE 7272 is a monolithic integrated low-drop voltage regulator for load currents up to 300 mA. An input voltage up to 42 V is regulated to $V_{Q,nom}$ = 5.0 V with a precision of ±2%. Due to its integrated reset circuitry featuring power on timing and output voltage monitoring the IC is well suited as µ-controller supply. The sophisticated design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions. Of course the TLE 7272 can be used also in all other applications, where a stabilized 5 V voltage is required. Due to its ultra low stand-by current consumption of typ. 20 µA the TLE 7272 is dedicated for use in applications permanently connected to V_{BAT}. In addition the IC can be switched off via the Inhibit input reducing the current consumption to typ. 5 µA. An integrated output sink current circuitry keeps the voltage at the Output pin Q below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage. For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7272. A mV-range output noise on the TLE 7272 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

Type	Ordering Code	Package
TLE 7272 D	Q67006-A9734	P-TO252-5
TLE 7272 G	Q67006-A9735	P-TO263-5

Reset

The Reset pin informs e.g. the microcontroller in case the output voltage has fallen below the lower threshold V_{RT} of typ. 4.65 V. The hysteresis is typically 100mV. Connecting the regulator to a battery voltage at first the reset signal remains LOW. When the output voltage has reached the reset threshold V_{RT} the reset output RO remains still LOW for the reset delay time t_{rd} (typ. 16 ms). Afterwards the reset output turns HIGH.

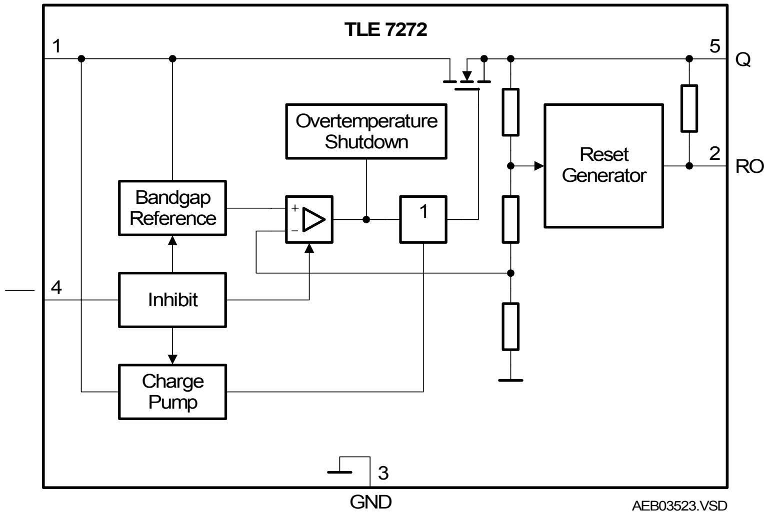


Figure 1 Block Diagram

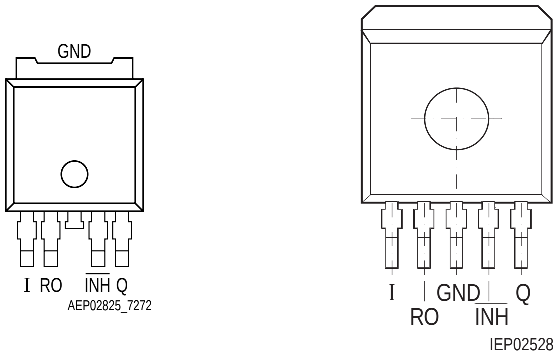


Figure 2 Pin Configuration P-TO252-5 (D-PAK), P-TO263-5 (D^2-PAK)(top view)

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	**Input;** block to ground directly at the IC with a ceramic capacitor.
2	RO	**Reset Output;** Open Collector Output with integrated pull-up resistor of typically 30kΩ. Optional external pull-up resistor of ≥ 10 kΩ to pin Q.
3	GND	**Ground;** Pin 3 internally connected to heatsink.
4	$\overline{\text{INH}}$	**Inhibit Input;** low level disables the IC. Integrated pull-down resistor.
5	Q	**Output;** block to ground with a ceramic capacitor, $C \geq 470$ nF.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Input I					
Voltage	V_I	-0.3	45	V	–
Current	I_I	-1	–	mA	–
Output Q					
Voltage	V_Q	-0.3	5.5	V	–
Voltage	V_Q	-0.3	6.2	V	t < 10 s[1)]
Current	I_Q	-1	–	mA	–
Reset Output RO					
Voltage	V_{RO}	-0.3	5.5	V	–
Voltage	V_{RO}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{RO}	-1	1	mA	–
Inhibit Input $\overline{INH}$					
Voltage	$V_{\overline{INH}}$	-0.3	45	V	Observe current limit $I_{\overline{INH}max}$[2)]
Current	$I_{\overline{INH}}$	-1	1	mA	–
Temperature					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.

2) External resistor required to keep the current below the absolute maximum rating when voltages ≥ 5.5 V are applied.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.5	42	V	–
Junction temperature	T_j	-40	150	°C	–

Note: In the operating range, the functions given in the circuit description are fulfilled.

Table 4 Thermal Resistance

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Junction case	R_{thj-c}	–	8	K/W	–
Junction ambient	R_{thj-a}	–	80	K/W	TO252[1)]
Junction ambient	R_{thj-a}	–	55	K/W	TO263[2)]

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm^3, heat sink area 300 mm^2

2) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm^3, heat sink area 300 mm^2

Application Information

Table 5 Electrical Characteristics

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		Min.	Typ.	Max.		
Output Q						
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA< I_Q <300 mA; 6 V < V_I < 16 V
Output voltage	V_Q	4.9	5.0	5.1	V	0.1 mA< I_Q <100 mA; 6 V < V_I < 40 V
Output current limitation	I_Q	320	–	–	mA	1)
Output current limitation	I_Q	–	–	800	mA	V_Q = 0V
Current consumption; $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.1 mA; T_j = 25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	40	µA	I_Q = 0.1 mA; $T_j \leq$ 80 °C
Quiescent current inhibited	I_q	–	5	9	µA	$V_{\overline{INH}}$ = 0 V; T_J < 80°C
Drop voltage	V_{dr}	–	250	500	mV	I_Q = 200 mA $V_{dr} = V_I - V_Q$ 1)
Load regulation	$\Delta V_{Q,lo}$	– 40	15	40	mV	I_Q = 5 mA to 250 mA
Line regulation	$\Delta V_{Q,li}$	– 20	5	20	mV	V_I = 10 V to 32 V; I_Q = 5 mA
Power supply ripple rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–
Output Capacitor	C_Q	470	–	–	nF	ESR < 3 Ω

Inhibit $\overline{INH}$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Measuring Condition
Turn-on Voltage	$V_{\overline{INH}\ ON}$	3.1	–	–	V	$V_Q \geq$ 4.9 V
Turn-off Voltage	$V_{\overline{INH}\ OFF}$	–	–	0.8	V	$V_Q \leq$ 0.3 V
H-input current	$I_{\overline{INH}\ ON}$	–	3	4	µA	$V_{\overline{INH}}$ = 5 V
L- input current	$I_{\overline{INH}\ OFF}$	–	0.5	1	µA	$V_{\overline{INH}}$ = 0 V, T_J < 80°C

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

Reset Output RO

Reset switching threshold	V_{RT}	4.50	4.65	4.80	V	V_Q decreasing V_I = 6V
Reset Read Room	V_{RH}	–	160	–	mV	
Reset output low voltage	V_{ROL}	–	0.2	0.4	V	R_{RO} = 10 kΩ; V_Q > 1 V
Internal reset pull up resistor	$R_{R,int}$	15	30	45	kΩ	
External reset pull up resistor	$R_{R,ext}$	10		∞[1]	kΩ	see Fig. 3
Reset delay time	t_{rd}	10	16	22	ms	
Reset reaction time	t_{rr}	–	–	12	µs	

1) An external reset pull up resistor is not required.

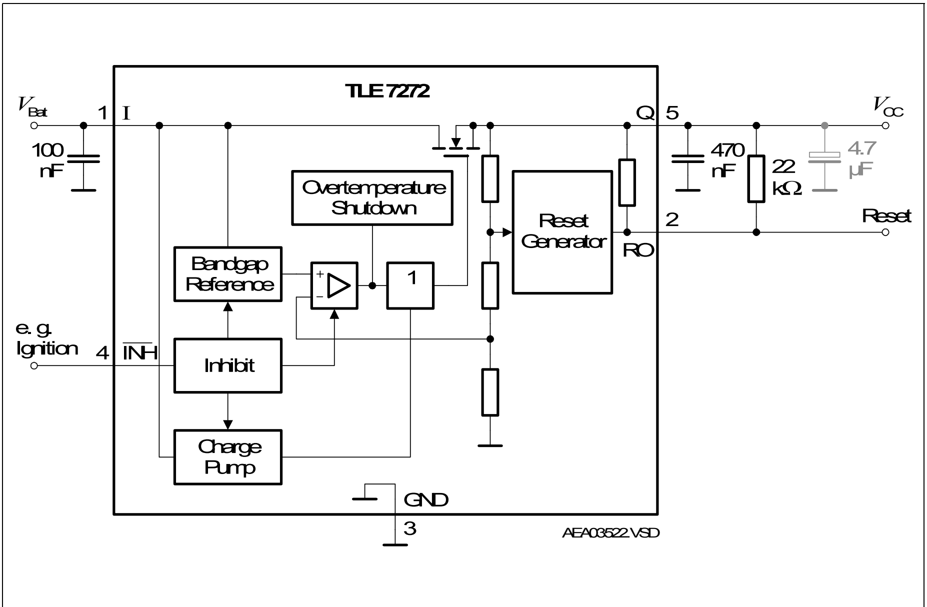


Figure 3 Application Diagram

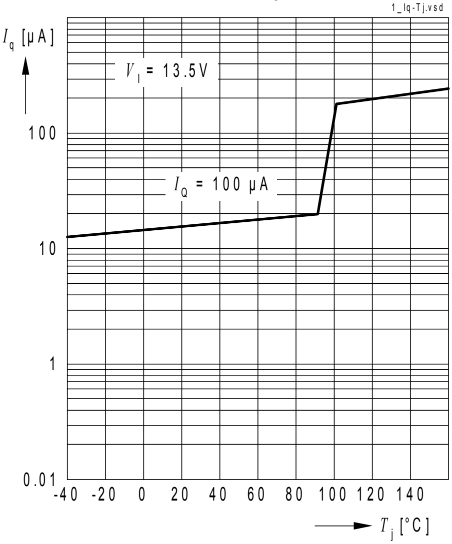
Input, Output

An input capacitor is necessary for damping line influences. A resistor of approx. 1 Ω in series with C_I, can damp the LC of the input inductivity and the input capacitor.

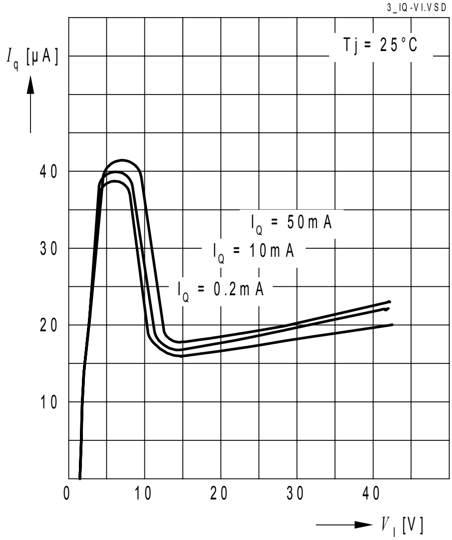
The TLE 7272 requires a ceramic output capacitor of at least 470 nF to assure stability of the regulation loop. In order to damp influences resulting from load current surges it is recommended to add an additional electrolytic capacitor of 4.7 µF to 47 µF at the output as shown in **Figure 3**.

Typical Performance Characteristics

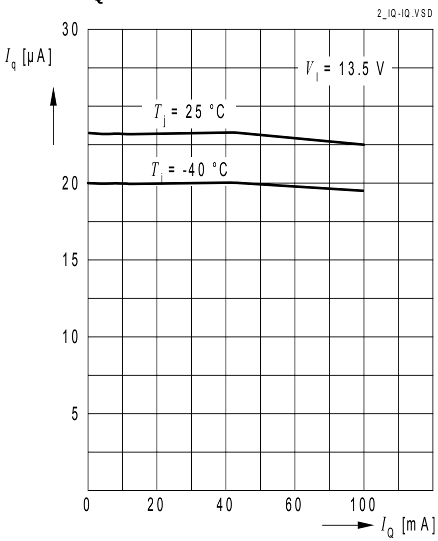
Current Consumption I_q versus Junction Temperature T_j



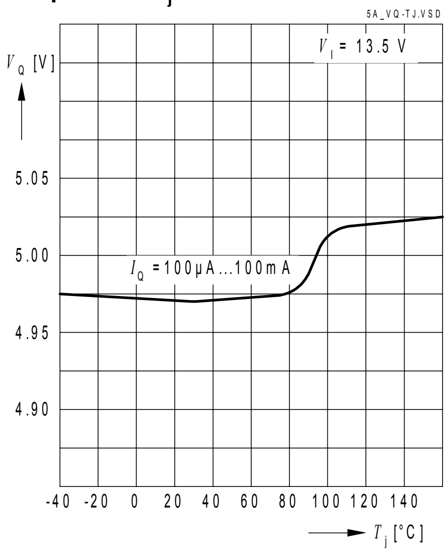
Current Consumption I_q versus Input Voltage V_I



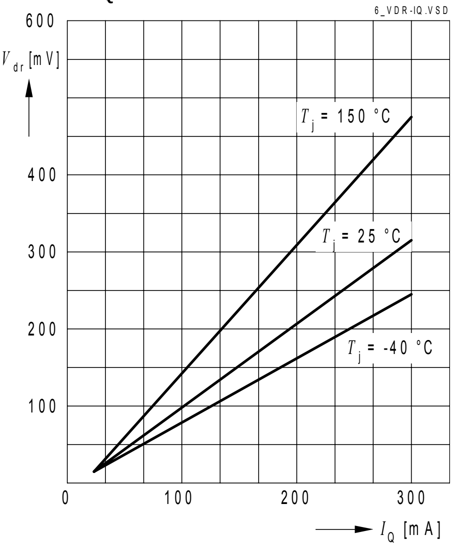
Current Consumption I_q versus Output Current I_Q



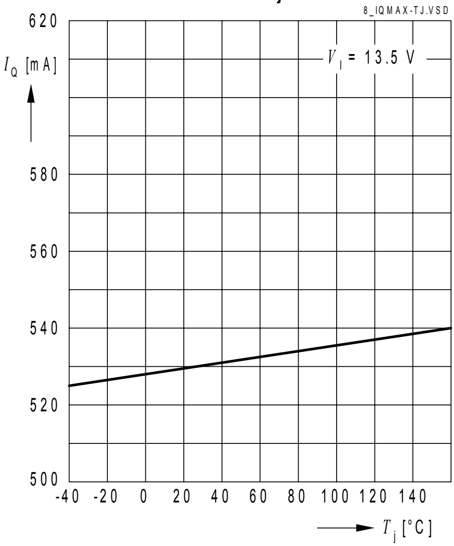
Output Voltage V_Q versus Junction Temperature T_j



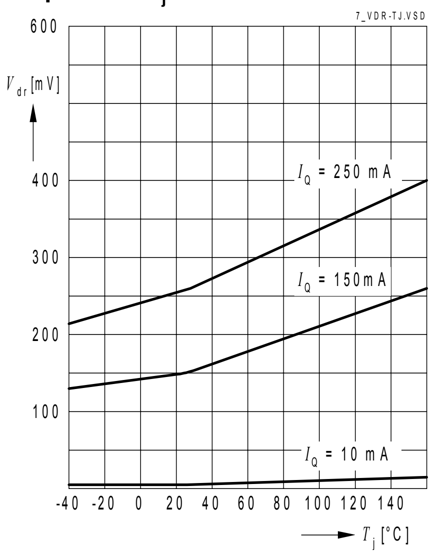
Dropout Voltage V_{dr} versus Output Current I_Q



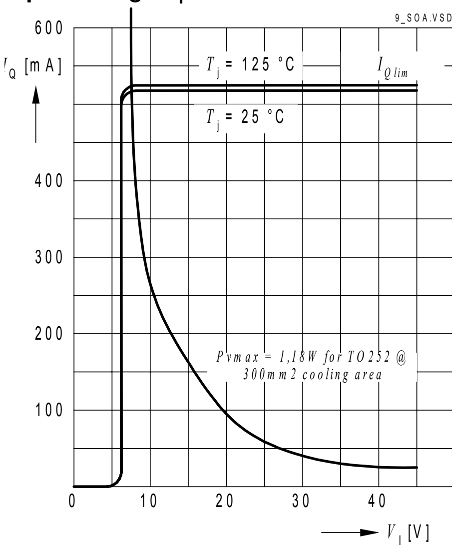
Maximum Output Current I_Q versus Junction Temperature T_j



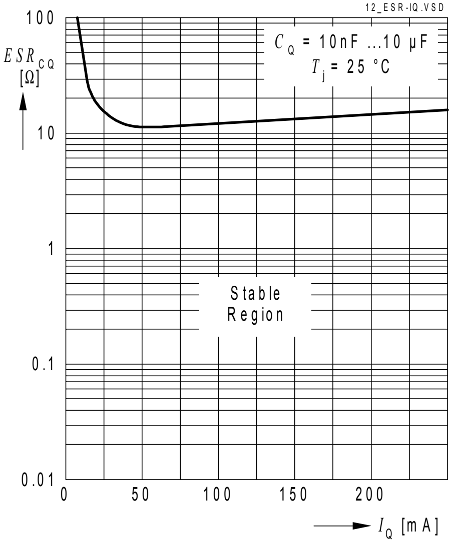
Dropout Voltage V_{dr} versus Junction Temperature T_j



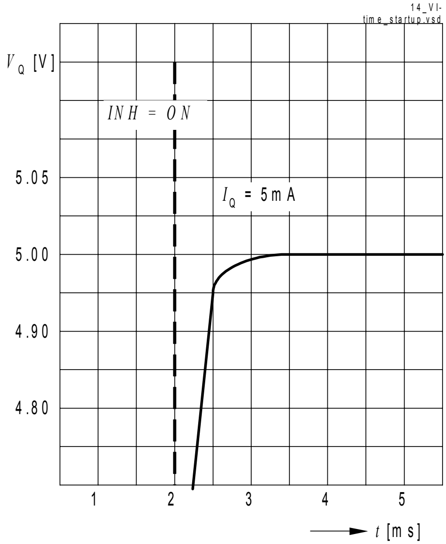
Maximum Output Current I_Q versus Input Voltage V_I



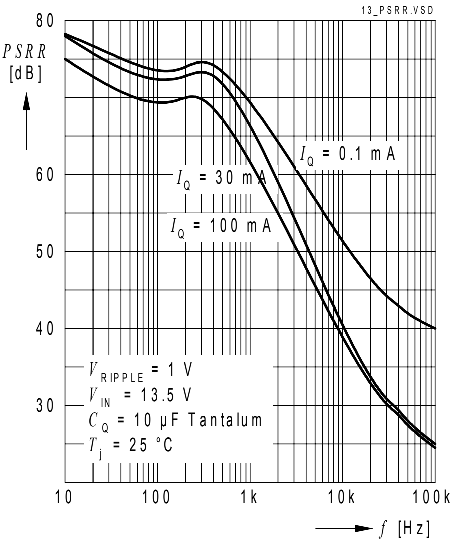
Region of Stability



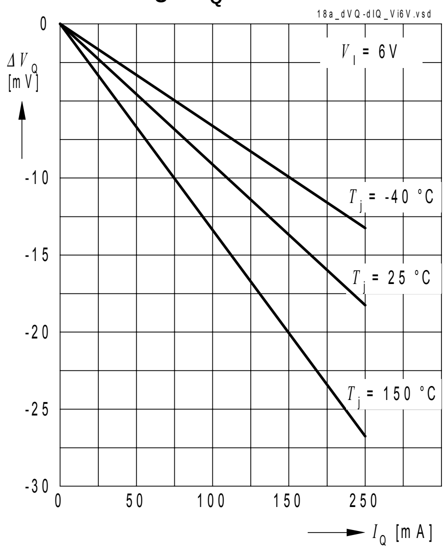
Output Voltage V_Q Start-up behaviour



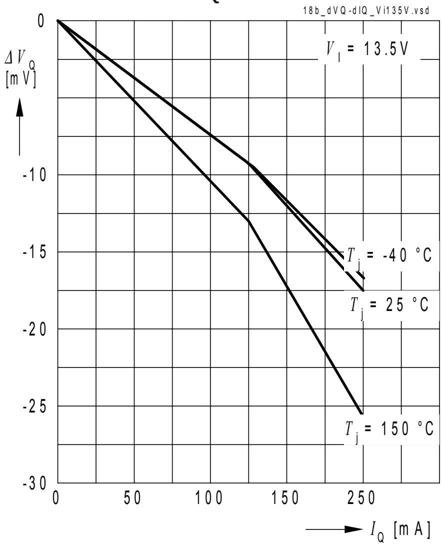
Power Supply Ripple Rejection PSRR versus Frequency f



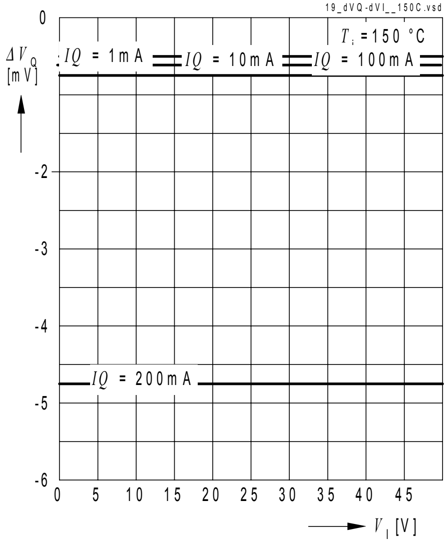
Load Regulation dV_Q versus Output Current Change dI_Q



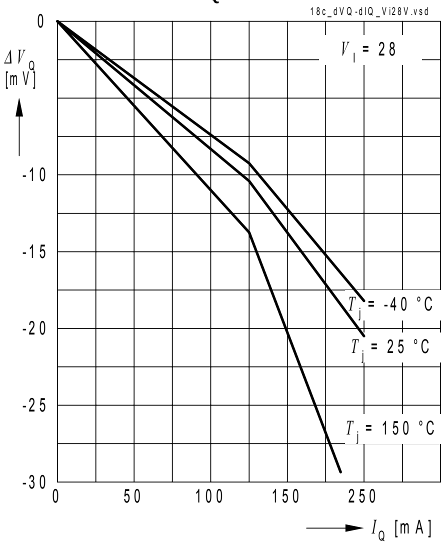
Load Regulation dV_Q versus Output Current Change dI_Q



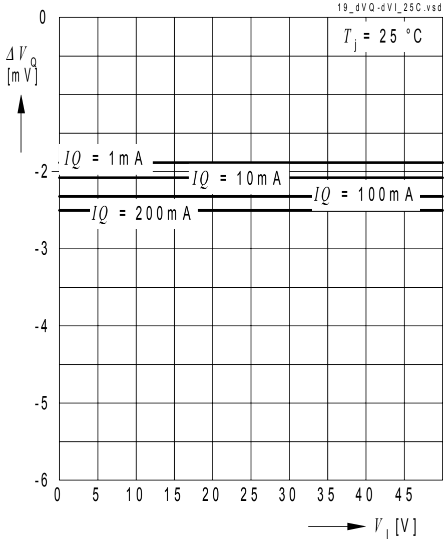
Line Regulation dV_Q versus Input Voltage ChangedV_I



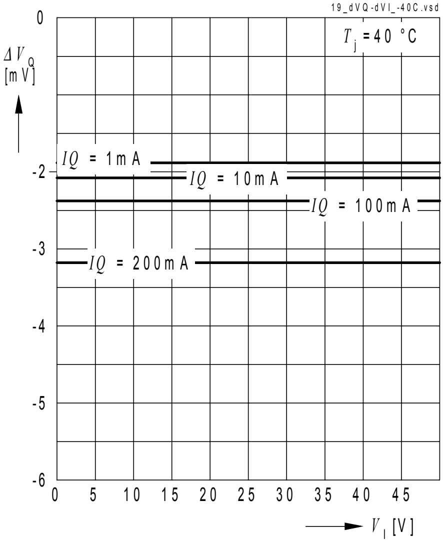
Load Regulation dV_Q versus Output Current Change dI_Q



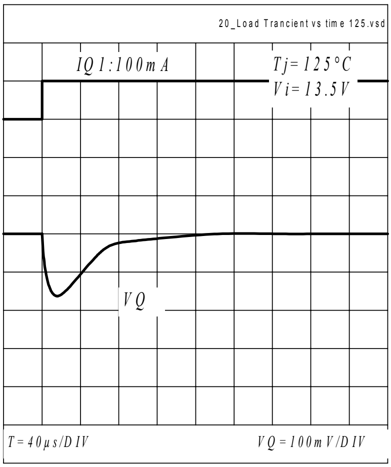
Line Regulation dV_Q versus Input Voltage ChangedV_I



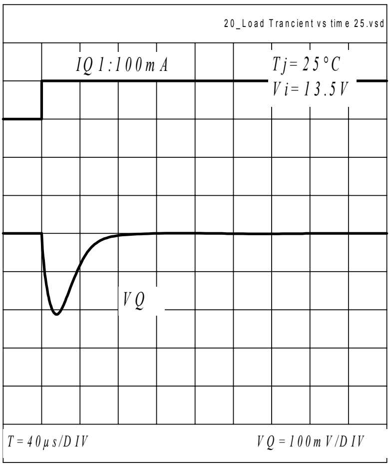
Line Regulation dV_Q versus Input Voltage Change dV_I



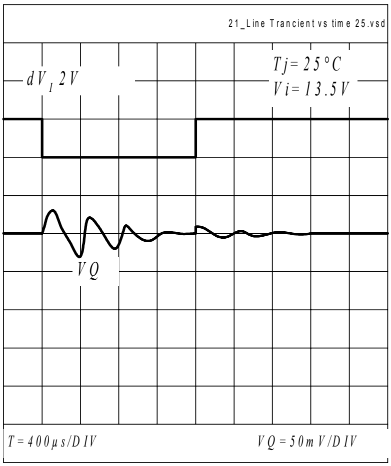
Load Transient Response Peak Voltage dV_Q



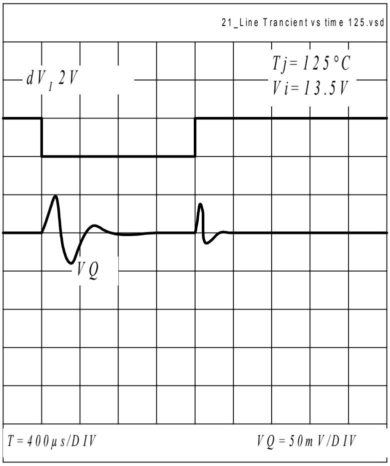
Load Transient Response Peak Voltage dV_Q



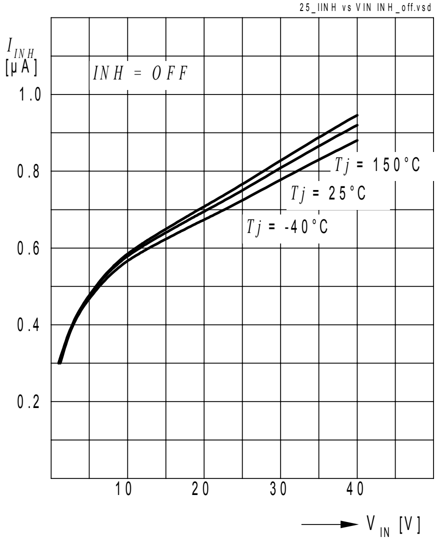
Line Transient Response Peak Voltage dV_Q



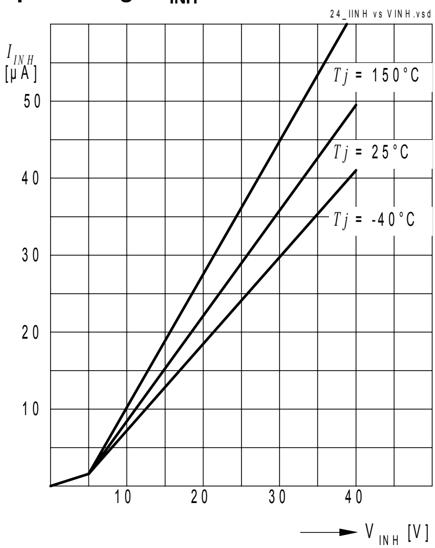
Line Transient Response Peak Voltage dV_Q



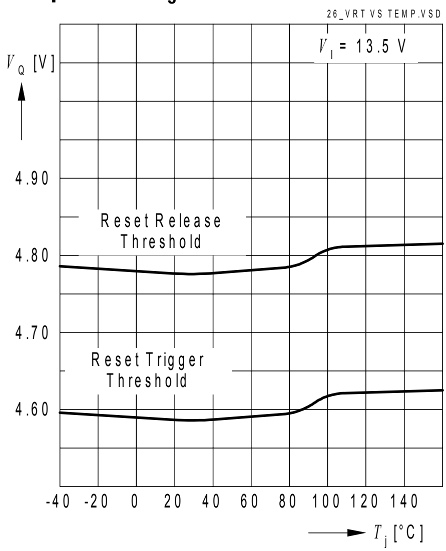
Inhibit Input Current I_{INH} versus Input Voltage V_I, INH=Off



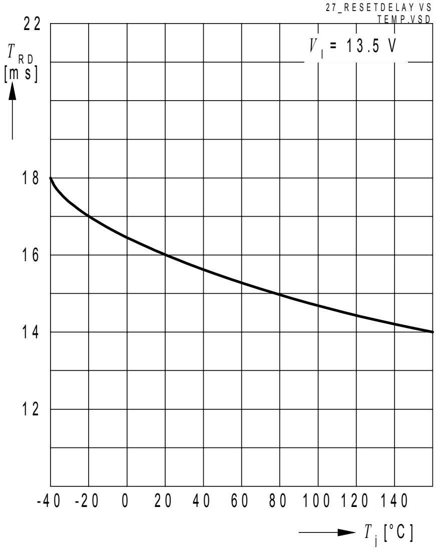
Inhibit Input Current I_{INH} versus Inhibit Input Voltage V_{INH}



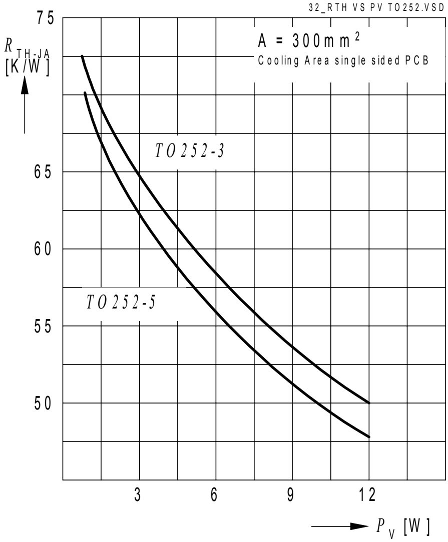
Reset Threshold V_{RT} versus Junction Temperature T_J



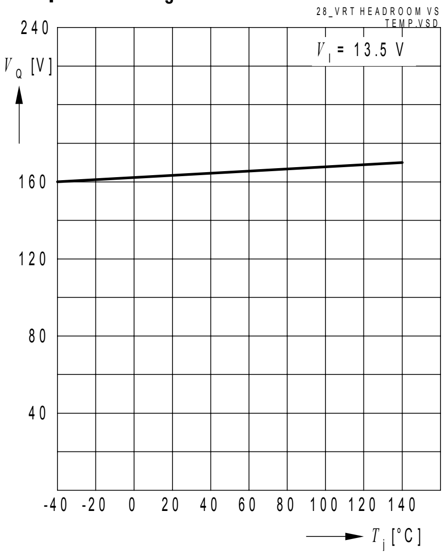
Reset Delay T_{RD} Time versus Junction Temperature T_J



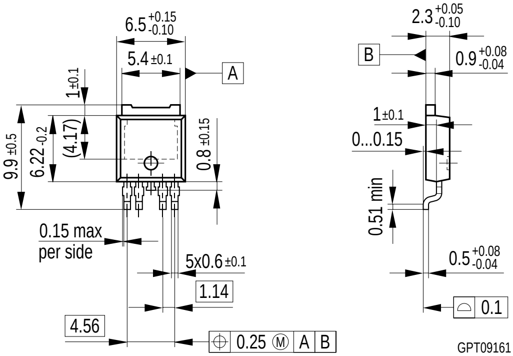
Thermal Resistance Junction-Ambient R_{THJA} versus Power Dissipation P_V



Reset Headroom versus Junction Temperature T_J



Package Outlines



All metal surfaces tin plated, except area of cut.

Figure 4 **P-TO252-5-1** (Plastic Transistor Single Outline)

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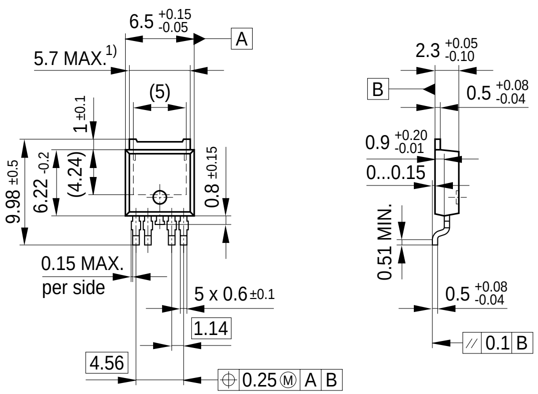
Dimensions in mm



1) Includes mold flashes on each side.
All metal surfaces tin plated, except area of cut.

GPT09527

Figure 5 **P-TO252-5-11** (Plastic Transistor Single Outline)

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Dimensions in mm

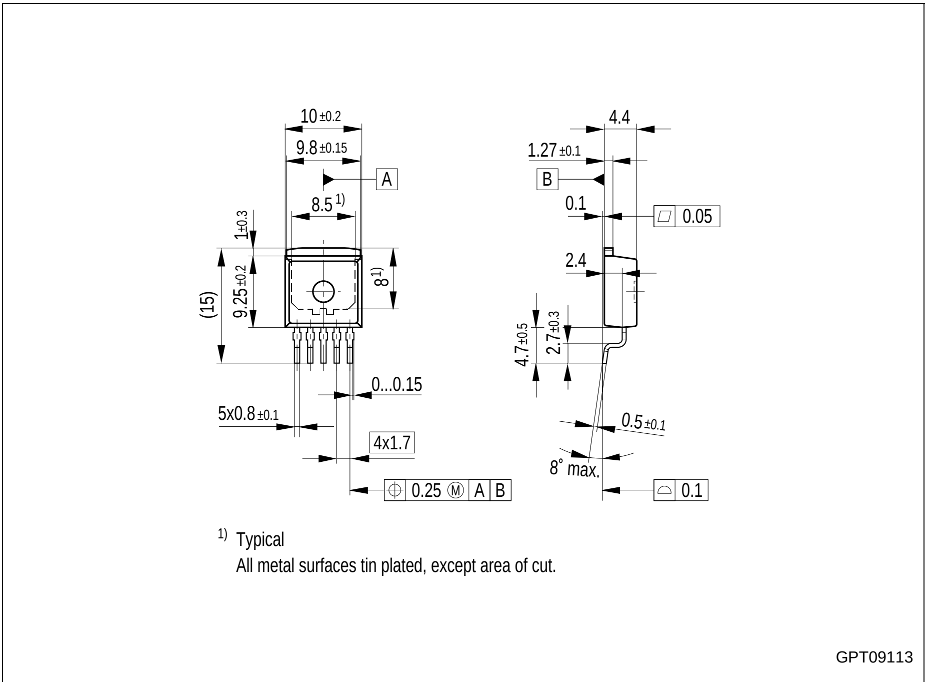

Figure 6 **P-TO263-5-1** (Plastic Transistor Single Outline)

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Dimensions in mm

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TLE 7272
5-V Low Drop Voltage Regulator
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Previous Version:	0.41
	minor text modifications
	release final Version
Previous Version:	1.0a
	minor text modifications