# SFX-200G Synchronous Clock Generators



PLL

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# **Applications**

- SONET / SDH / ATM
- DWDM / FDM
- FEC (Forward Error Correction)

#### **Features**

- Available as a 5.0V or 3.3V High Precision PLL
- Two User Selectable PECL Input References Frequencies
- Two user Selectable PECL Output Frequencies
- Jitter Generation OC-192 Compliant
- 1.2" x 1.0" x 0.285", Surface Mount
- RoHS Compliant



Bulletin	SG152
Page	1 of 8
Revision	00
Date	2 MAY 07
Issued By	ENG

### **General Description**

The SFX-200G is a high precision frequency translator that translates one of two inputs, greater than 1MHz, to one of two selectable output frequencies between 77.76 MHz and 777.6 MHz. The SFX-200G supports all major FEC rates such as 15/14, 255/237 etc.

SFX-200G is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment. The SFX-200G provides a jitter filtered, wander following output signal synchronized to

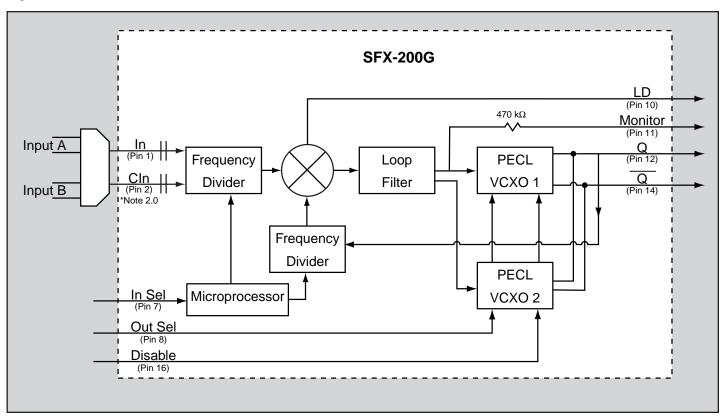
a superior Stratum or peer input reference signal.

The SFX-200G includes a lock detect alarm output. The PLL control voltage is brought out through a 470 k $\Omega$  resistor and can be used to determine when the pull range limits are reached. The LVPECL outputs may be put into the tri-state high impedance condition for external testing purposes by asserting a high signal to the Enable/Disable pin.

The SFX-200G package typical dimensions are 1.2" x 1.0"  $\times$  0.285". Parts are assembled using high temperature solder to withstand surface mount reflow process.

### **Functional Block Diagram**

Figure 1



## **Absolute Maximum Rating**

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage (OptionC) Power Supply Voltage (OptionD)	-0.3 -0.3		5.5 3.8	Volts Volts	
V <sub>I</sub>	Input Voltage	-0.2		Vcc	Volts	
Ts	Storage Temperature (OptionF) Storage Temperature (OptionC)	-55 -40		125 85	°C °C	



Data Sheet #: **SG152** Page **2** of **8** Rev: **00** Date: **5/2/07** 

# **Specifications**

Table 2

Symbol	ymbol Parameter		Nominal	Maximum	Units	Notes
f <sub>IN</sub>	Input Frequencies (Comp PECL)	1		777.6	MHz	3.0
	Input Frequencies (HCMOS )	1		100	MHz	2.0
f <sub>out</sub>	Output Frequencies (Comp PECL)	77.76		777.6	MHz	
Vcc	Supply Voltage ( $C = 5.0 V_{DC}$ ) ( $D = 3.3 V_{DC}$ )	4.75 3.15	5.0 3.3	5.25 3.45	Volts Volts	
I <sub>cc</sub>	Supply Current		80		mA	
V <sub>OH</sub>	High Level Output Voltage	2.275			V	
V <sub>OL</sub>	Low Level Output Voltage			1.68	V	
$T_R/T_F$	Rise/Fall Time - 622MHz 155 MHz		250 600	400 1500	ps ps	
SYM	Output Symmetry	45		55	%	
${\sf J}_{\sf GEN}$	Jitter Generation RMS (12 kHz - 20 MHz)		0.5	1	ps	
J <sub>TRAN</sub>	Jitter Transfer			0.1	dB	1.0
APR	Input Frequency Tracking	±50			ppm	
T <sub>OP</sub>	Operating Temperature F = C =	-40 0		85 70	°C °C	

NOTES: 1.0: GR-253-CORE, Sec. 5.6.2.1.2

- 2.0: For reference inputs <100MHz,  $\overline{\text{CIN}}$  (Pin 2) is not used and is not terminated internally. For Complementary Inputs ≥100 MHz, Both IN (Pin 1) and  $\overline{\text{CIN}}$  (Pin 2) are required.
- 3.0: Both reference inputs frequencies must be either <100 MHz or  $\geq$ 100 MHz. Reference A <100 MHz and Reference B  $\geq$ 100 MHz is not supported.

### **Pin Description**

#### Table 3

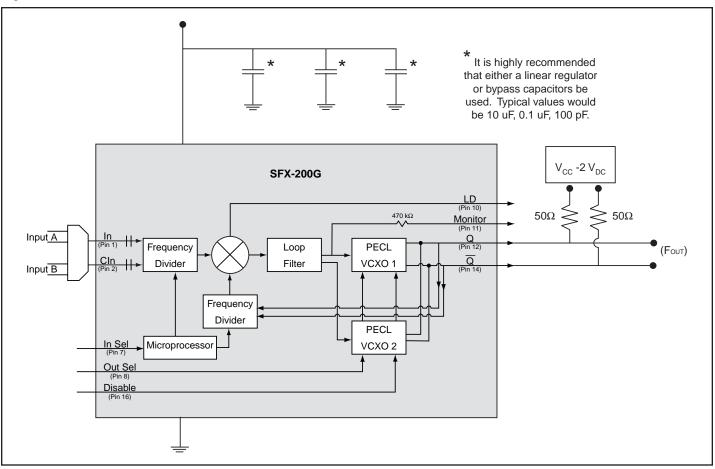
Pin#	Connection	Description			
1	In	Input Frequency, Signal is AC coupled			
2	Cln	Complementary Input Frequency, Signal is AC coupled			
3		Missing			
4		Missing			
5		Missing			
6		Missing			
7	In Sel	Input Frequency Select - Logic "0" = Input Freq. A, Logic "1" = Input Freq. B			
8	Out Sel	Output Frequency Select - Logic "0" = Output Freq. #1, Logic "1" = Output Freq. #2			
9	Vcc	Supply Voltage			
10	LD (Output)	Lock Detect Logic "1" indicates that the unit is locked to the input reference Logic "0" indicates that the reference is lost or out of lock range			
11	Monitor (Output)	Control voltage level for the PECL oscillator and is brought out through a $470k\Omega$ resistor			
12	Q	PECL Output			
13	GND	Ground			
14	Q	PECL Complemetary Output			
15	GND	Ground			
16	Disable (Input)	Logic "0" (or no connect) = PECL Outputs are Enabled Logic "1" = PECL Outputs are put into Tri-State High Impedence			



Data Sheet #: SG152 Page 3 of 8 Rev: 00 Date: 5/2/07

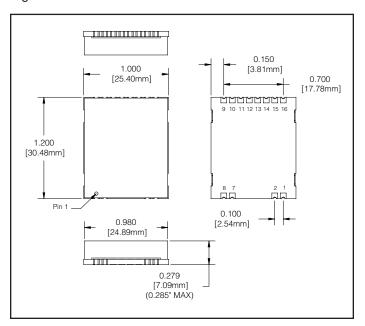
# **Output Load and Power Supply Filtering Recommendations**

Figure 2



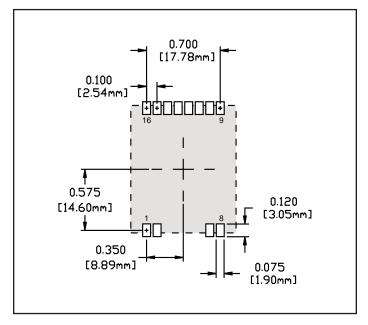
## **Package Dimensions**

Figure 3



## **Recommended Footprint Dimensions**

Figure 4

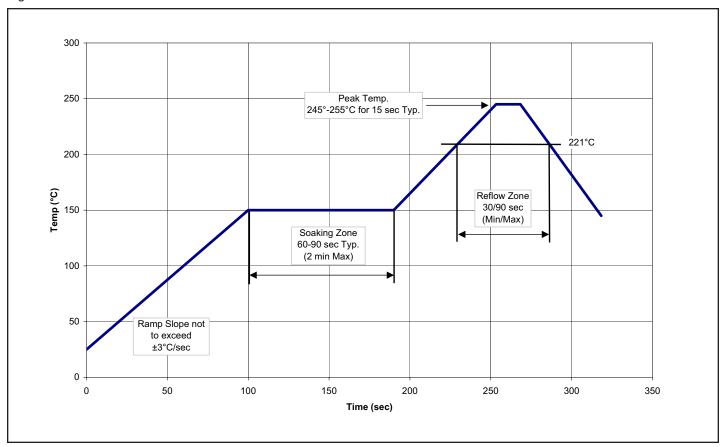




Data Sheet #: SG152 Page 4 of 8 Rev: 00 Date: 5/2/07

### **Solder Profile**

Figure 5



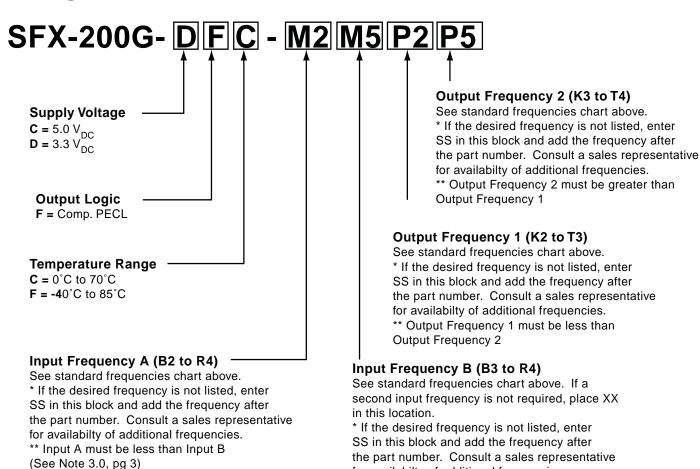


Data Sheet #: **SG152** Page **5** of **8** Rev: **00** Date: **5/2/07** 

### **Standard Frequencies**

1.0240 MHz	B2	22.2171 MHz	E5	82.9440 MHz	K6	625.0000 MHz	P3
1.5440 MHz	B3	26.0000 MHz	F3	112.0000 MHz	L2	627.3596 MHz	P7
2.0480 MHz	B4	27.0000 MHz	F4	114.0000 MHz	L3	644.5312 MHz	P4
4.0960 MHz	B5	29.4912 MHz	F5	125.0000 MHz	L4	666.5143 MHz	P5
6.4800 MHz	C2	32.7680 MHz	H3	139.2640 MHz	L5	669.1281 MHz	R2
8.1920 MHz	C3	37.0560 MHz	H4	155.5200 MHz	M2	669.3266 MHz	R3
10.0000 MHz	C4	38.8800 MHz	H5	156.2500 MHz	МЗ	672.1627 MHz	R5
12.8000 MHz	D2	44.4343 MHz	J2	161.1328 MHz	M4	690.5692 MHz	R4
13.0000 MHz	D3	44.7360 MHz	J3	166.6286 MHz	M5	710.9486 MHz	T2
15.0000 MHz	D4	51.8400 MHz	J4	167.3316 MHz	N2	719.7344 MHz	Т3
16.3840 MHz	D5	61.4400 MHz	J5	168.0407 MHz	N3	777.6000 MHz	T4
19.4400 MHz	D6	65.5360 MHz	J6	311.0400 MHz	P1	No 2nd Input Freq.	XX
20.0000 MHz	E2	77.7600 MHz	K2	622.0800 MHz	P2	Input Freq. not listed	SS
20.1416 MHz	E3	78.1250 MHz	K3	624.7048 MHz	P6	Output Freq. not listed	SS
20.4800 MHz	E4	78.6432 MHz	K5				

### **Ordering Information**





Data Sheet #: **SG152** Page 6 of 8 Rev: **00** Date: **5/2/07** 

for availabilty of additional frequencies.

\*\* Input B must be greater than Input A

(See Note 3.0, pg 3)



Data Sheet #: **SG152** Page **7** of **8** Rev: **00** Date: **5/2/07** 



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Revision	Revision Date	Note
00	5/2/07	Final Release