Dual, 30V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output, Operational Amplifier

ADA4096S

1.0 Scope

1.1. This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

1.2. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aeroinfo

1.3. This data specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at http://www.analog.com/ADA4096

2.0 Part Number

2.1. The complete part number(s) of this specification follows:

Specific Part Number	Description
ADA4096R703F	Dual, 30V, Micropower, Overvoltage Protection, Rail-to-Rail Input/Output, Operational Amplifier. Radiation tested to 100Krads (Si)

3.0 Case Outline

3.1. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline Letter	Descriptive Designator	Terminals	Package style
X	CDFP3-F10	10 lead	Bottom Brazed Flat pack

Package: X			
Pin Number	Terminal Symbol	Pin Type	Pin Description
1	OUT A	Analog output	Operational amplifier output, Amp-A
2	-IN A	Analog input	Operational amplifier negative input, Amp-A
3	NC/GND	N/A	No connection or ground this terminal
4	+IN A	Analog input	Operational amplifier positive input, Amp-A
5	-Vs	power	Negative power supply
6	+IN B	Analog input	Operational amplifier positive input, Amp-B
7	-IN B	Analog input	Operational amplifier negative input, Amp-B
8	NC/GND	N/A	No connection or ground this terminal
9	OUT B	Analog output	Operational amplifier output, Amp-B
10	+Vs	power	Positive power supply

Figure 1 – Terminal Connections

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

4.0 Specifications

4.1. Absolute Maximum Ratings 1/

Supply voltage ($+V_{SY}$ to $-V_{SY}$) ..... 36 V
Input voltage (V_{IN})
Operating ..... $-V_{SY}$ to $+V_{SY}$
Overvoltage Condition 2/..... $-V_{SY}$ - 32V to $+V_{SY}$ + 32V
Differential Input Voltage 3/ ..... $\pm V_{SY}$
Input Current ..... ± 5 mA
Output short circuit duration to GND..... Indefinite
Storage temperature range ..... -65°C to +150°C
Junction temperature maximum (T_J) ..... +150°C
Lead temperature (soldering, 60 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 17 °C/W 4/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 27 °C/W 4/

4.2. Recommended Operating Conditions 5/

Supply voltage ($\pm V_{SY}$) ..... ±1.8 V to ±15.0 V
Ambient operating temperature range (T_A)..... -55°C to +125°C

4.3. Nominal Operating Performance Characteristics (TA = 25°C, V_{CM} = 0V unless otherwise noted)

Input Capacitance
Differential (C_{DM}) V_{SY} = ±15 V ..... 2.5 pF
Common Mode (C_{CM}) V_{SY} = ±15 V..... 7.0 pF
Settling Time (t_S) to 0.1%, 10V step, V_{SY} = ±15 V..... 23.4 µS
Closed-Loop Impedance (Z_{OUT} f = 100 kHz, A_V = 1)
V_{SY} = ±1.5 V ..... 102 Ω
V_{SY} = ±5 V ..... 71 Ω
V_{SY} = ±15 V ..... 40 Ω
Unity-Gain Crossover (V_{IN} = 5 mV_{p-p}, R_L = 10 kΩ, A_V = 1)
V_{SY} = ±1.5 V ..... 465 kHz
V_{SY} = ±5 V ..... 550 kHz
V_{SY} = ±15 V ..... 800 kHz
Phase Margin
V_{SY} = ±1.5 V ..... 51 Degrees
V_{SY} = ±5 V ..... 52 Degrees
V_{SY} = ±15 V ..... 60 Degrees
-3 dB Closed-Loop Bandwidth (V_{IN} = 5 mV_{p-p}, A_V = 1)
V_{SY} = ±1.5 V ..... 672 kHz
V_{SY} = ±5 V ..... 783 kHz
V_{SY} = ±15 V ..... 1029 kHz

NOISE PERFORMANCE (V_{SY} = ±1.5V, V_{SY} = ±5 V, V_{SY} = ±15 V)

Voltage Noise (e_n p-p 0.1 Hz to 10 Hz) ..... 0.7 Vp-p

Voltage Noise Density (e_n f=1kHz) ..... 27 nV/√Hz

Current Noise Density (i_n f=1kHz) ..... 0.2 pA/√Hz

Channel Separation (V_{SY} = ±15 V) ..... 100 dB

4.4. Radiation Features

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)….100 k rads(Si)

1/ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2/ Performance not guaranteed during overvoltage conditions.

3/ Limit the input current to +/-5mA.

4/ Measurement taken under absolute worst case condition and represents data taken with thermal camera for highest power density location. See MIL-STD-1835 for average θ_{JC} number.

5/ Minimum supply voltages of $\pm V_{SY}$=±1.5 V can be used for Ambient operating temperature range limited to (T_A) -40°C to +125°C while minimum supply voltages of $\pm V_{SY}$=±1.65 V must be used for Ambient operating temperature range (T_A) -55°C to +125°C to meet Table I specifications.

TABLE IA – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-1.8V)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		1	-300	300	µV
			2,3	-500	500	µV
		M,D,P,L,R	1	-300	300	µV
Offset Voltage Matching	V_{OSA}- V_{OSB}		1	-300	300	µV
			2,3	-500	500	µV
		M,D,P,L,R	1	-300	300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	3/ 4/	2,3	-3	2	µV/°C
Input Bias Current	I_B		1	-25	0	nA
			2	-30	5	nA
			3	-35	0	nA
		M,D,P,L,R	1	-25	0	nA
Input Bias Current	I_B	V_{CM} = +V_{SY}	1	0	25	nA
			2	-10	35	nA
			3	0	45	nA
		M,D,P,L,R	1	0	25	nA
Input Bias Current	I_B	V_{CM} = -V_{SY}	1	-45	-15	nA
			2	-50	5	nA
			3	-65	-10	nA
		M,D,P,L,R	1	-45	-15	nA
Input Offset Current	I_{OS}		1,2	-1.5	1.5	nA
			3	-3	3	nA
		M,D,P,L,R	1	-1.5	1.5	nA
Input Voltage Range	IVR		1,2,3	-V_{SY}	+V_{SY}	V
		M,D,P,L,R	1	-V_{SY}	+V_{SY}	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -V_{SY} to +V_{SY}	1	61		dB
			2,3	58		dB
		M,D,P,L,R	1	61		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = -V_{SY}+0.1V to +V_{SY} -0.1V	1	91		dB
			2,3	84		dB
		M,D,P,L,R	1	91		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = -V_{SY}+0.2V to +V_{SY} -0.2V	1	86		dB
			2,3	77		dB
		M,D,P,L,R	1	86		dB

TABLE IA – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-1.8V) – Cont.

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	1	$+V_{SY}$ - 0.02		V
			2,3	$+V_{SY}$ - 0.05		V
		M,D,P,L,R	1	$+V_{SY}$ - 0.02		V
		R_L = 2 kΩ to GND	1	$+V_{SY}$ - 0.05		V
			2,3	$+V_{SY}$ - 0.1		V
		M,D,P,L,R	1	$+V_{SY}$ - 0.05		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND	1		$-V_{SY}$ + 0.02	V
			2,3		$-V_{SY}$ + 0.05	V
		M,D,P,L,R	1		$-V_{SY}$ + 0.02	V
		R_L = 2 kΩ to GND	1		$-V_{SY}$ + 0.04	V
			2,3		$-V_{SY}$ + 0.1	V
		M,D,P,L,R	1		$-V_{SY}$ + 0.04	V
Short-Circuit Limit	I_{SC+}	Source	1,2,3	-11	-1	mA
		M,D,P,L,R	1	-11	-1	mA
	I_{SC-}	Sink	1,2,3	2	13	mA
		M,D,P,L,R	1	2	13	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.3V to 36V	1,2	100		dB
			3	90		dB
		M,D,P,L,R	1	100		dB
Total Supply Current (Both Amplifiers)	I_{SY}	V_O = 0 V	1		100	µA
			2		140	µA
			3		130	µA
		M,D,P,L,R	1		100	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF 2/ 3/ 5/	4	0.15		V/us
			5	0.25		V/us
			6	0.09		V/us
Gain Bandwidth Product	GBP	V_{IN} = 5 mV_{p-p}, R_L = 10 kΩ, A_V = -100 2/ 3/	4,5,6	350		kHz

TABLE IA NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, T_A min = -55ºC and V_{CM} = 0V unless otherwise noted.

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ Calculated from 25ºC to -55ºC, 25ºC to 125ºC and -55ºC to 125ºC

5/ Measured from 10% to 90% and 90% to 10% of rail to rail output swing.

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-5V)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		1	-300	300	µV
			2,3	-500	500	µV
		M,D,P,L,R	1	-300	300	µV
Offset Voltage Matching	V_{OSA}- V_{OSB}		1	-300	300	µV
			2,3	-500	500	µV
		M,D,P,L,R	1	-300	300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	3/ 4/	2,3	-3	2	µV/°C
Input Bias Current	I_B		1	-25	0	nA
			2	-25	10	nA
			3	-35	0	nA
		M,D,P,L,R	1	-25	0	nA
Input Bias Current	I_B	V_{CM} = +V_{SY} -2.5V	1	-20	5	nA
			2	-30	15	nA
			3	-35	10	nA
		M,D,P,L,R	1	-20	5	nA
Input Bias Current	I_B	V_{CM} = -V_{SY} +2.5V	1	-30	0	nA
			2	-35	10	nA
			3	-40	5	nA
		M,D,P,L,R	1	-25	0	nA
Input Bias Current	I_B	V_{CM} = +V_{SY}	1	0	25	nA
			2	-10	35	nA
			3	0	45	nA
		M,D,P,L,R	1	10	35	nA
Input Bias Current	I_B	V_{CM} = -V_{SY}	1	-45	-15	nA
			2	-50	5	nA
			3	-70	-15	nA
		M,D,P,L,R	1	-40	-15	nA
Input Offset Current	I_{OS}		1	-2	2	nA
			2,3	-3	3	
		M,D,P,L,R	1	-2	2	nA
Input Voltage Range	IVR		1,2,3	-V_{SY}	+V_{SY}	V
		M,D,P,L,R	1	-V_{SY}	+V_{SY}	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -V_{SY} to +V_{SY}	1	72		dB
			2,3	68		dB
		M,D,P,L,R	1	72		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = -V_{SY}+2V to +V_{SY} -2V	1	91		dB
			2,3	85		dB
		M,D,P,L,R	1	91		dB

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-5V) – Cont.

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS – cont.						
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = -V_{SY}+0.2V to +V_{SY} -0.2V	1	102		dB
			2,3	99		dB
		M,D,P,L,R	1	102		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = -V_{SY}+0.3V to +V_{SY} -0.3V	1	93		dB
		V_O = -V_{SY}+0.3V to +V_{SY} -0.3V	2	88		dB
		V_O = -V_{SY}+0.4V to +V_{SY} -0.4V	3	88		dB
		M,D,P,L,R	1	93		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	1	+V_{SY} - 0.04		V
			2,3	+V_{SY} - 0.05		V
		M,D,P,L,R	1	+V_{SY} - 0.04		V
		R_L = 2 kΩ to GND	1	+V_{SY} - 0.2		V
			2,3	+V_{SY} - 0.3		V
		M,D,P,L,R	1	+V_{SY} - 0.2		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND	1		-V_{SY} + 0.03	V
			2,3		-V_{SY} + 0.05	V
		M,D,P,L,R	1		-V_{SY} + 0.03	V
		R_L = 2 kΩ to GND	1		-V_{SY} + 0.2	V
			2,3		-V_{SY} + 0.25	V
		M,D,P,L,R	1		-V_{SY} + 0.2	V
Short-Circuit Limit	I_{SC+}	Source	1,2	-18	-6	mA
			3	-14	-2	
		M,D,P,L,R	1	-18	-6	mA
	I_{SC-}	Sink	1,2,3	3	16	mA
		M,D,P,L,R	1	3	16	mA
POWER SUPPLY						
Total Supply Current (Both Amplifiers)	I_{SY}	V_O = 0 V	1		110	µA
			2,3		150	µA
		M,D,P,L,R	1		110	µA

TABLE IB – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-5V) – Cont.

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF 2/ 3/ 5/	4	0.2		V/us
			5	0.3		V/us
			6	0.12		V/us
Gain Bandwidth Product	GBP	V_{IN} = 5 mV_{p-p}, R_L = 10 kΩ, A_V = -100 2/ 3/	4,5,6	450		kHz

TABLE IB NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, T_A min = -55ºC and V_{CM} = 0V unless otherwise noted.

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ Calculated from 25ºC to -55ºC, 25ºC to 125ºC and -55ºC to 125ºC

5/ Measured from 10% to 90% and 90% to 10% of rail to rail output swing.

TABLE IC – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-15V)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		1	-300	300	µV
			2,3	-500	500	µV
		M,D,P,L,R	1	-300	300	µV
Offset Voltage Matching	V_{OSA}- V_{OSB}		1	-300	300	µV
			2,3	-500	500	µV
		M,D,P,L,R	1	-300	300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	3/ 4/	2,3	-3	2	µV/°C
Input Bias Current	I_B		1	-20	5	nA
			2	-25	10	nA
			3	-25	10	nA
		M,D,P,L,R	1	-20	5	nA
Input Bias Current	I_B	V_{CM} = +V_{SY} -2.5V	1	-10	15	nA
			2	-20	25	nA
			3	-20	25	nA
		M,D,P,L,R	1	-10	15	nA
Input Bias Current	I_B	V_{CM} = -V_{SY} +2.5V	1	-35	-5	nA
			2	-40	5	nA
			3	-50	-5	nA
		M,D,P,L,R	1	-35	-5	nA
Input Bias Current	I_B	V_{CM} = +V_{SY}	1	10	35	nA
			2	-5	40	nA
			3	10	55	nA
		M,D,P,L,R	1	10	35	nA
Input Bias Current	I_B	V_{CM} = -V_{SY}	1	-55	-25	nA
			2	-55	0	nA
			3	-80	-25	nA
		M,D,P,L,R	1	-55	-25	nA
Input Offset Current	I_{OS}		1,2	-1.5	1.5	nA
			3	-3	3	nA
		M,D,P,L,R	1	-1.5	1.5	nA
Input Voltage Range	IVR		1,2,3	-V_{SY}	+V_{SY}	V
		M,D,P,L,R	1	-V_{SY}	+V_{SY}	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = -V_{SY} to +V_{SY}	1	81		dB
			2,3	75		dB
		M,D,P,L,R	1	81		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = -V_{SY}+2V to +V_{SY} -2V	1	95		dB
			2,3	89		dB
		M,D,P,L,R	1	95		dB

TABLE IC – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-15V) – Cont.

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
INPUT CHARACTERISTICS – cont.						
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = -V_{SY}+0.3V to +V_{SY} -0.3V	1	109		dB
			2,3	105		dB
		M,D,P,L,R	1	109		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = -V_{SY}+4V to +V_{SY} -4V	1	99		dB
		V_O = -V_{SY}+4V to +V_{SY} -4V	2	90		dB
		V_O = -V_{SY}+5V to +V_{SY} -5V	3	90		dB
		M,D,P,L,R	1	99		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to GND	1	+V_{SY} - 0.08		V
			2,3	+V_{SY} - 0.25		V
		M,D,P,L,R	1	+V_{SY} - 0.08		V
		R_L = 2 kΩ to GND	1,2	+V_{SY} - 1		V
			3	+V_{SY} - 6		V
		M,D,P,L,R	1	+V_{SY} - 1		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to GND	1		-V_{SY} + 0.08	V
			2,3		-V_{SY} + 0.25	V
		M,D,P,L,R	1		-V_{SY} + 0.08	V
		R_L = 2 kΩ to GND	1		-V_{SY} + 0.75	V
			2		-V_{SY} + 1.5	V
			3		-V_{SY} + 3	V
		M,D,P,L,R	1		-V_{SY} + 0.75	V
Short-Circuit Limit	I_{SC+}	Source	1	-28	-17	mA
			2	-34	-20	mA
			3	-28	-6	mA
		M,D,P,L,R	1	-28	-17	mA
	I_{SC-}	Sink	1,2,3	8	18	mA
		M,D,P,L,R	1	8	18	mA
POWER SUPPLY						
Total Supply Current (Both Amplifiers)	I_{SY}	V_O = 0 V, V_{SY} = +/-15V & V_{SY} = +/-16.5V	1		150	µA
			2,3		200	µA
		M,D,P,L,R	1		150	µA

TABLE IC – ELECTRICAL PERFORMANCE CHARACTERISTICS (V_{SY} = +/-15V) – Cont.

Parameter See notes at end of table	Symbol	Conditions 1/ Unless otherwise specified	Sub-Group	Limit Min	Limit Max	Units
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF 2/ 3/ 5/	4	0.3		V/us
			5	0.4		V/us
			6	0.2		V/us
Gain Bandwidth Product	GBP	V_{IN} = 5 mV_{p-p}, R_L = 10 kΩ, A_V = -100 2/ 3/	4,5,6	600		kHz

TABLE IC NOTES:

1/ T_A nom = 25ºC, T_A max = 125ºC, T_A min = -55ºC and V_{CM} = 0V unless otherwise noted.

2/ Parameter is part of device initial characterization which is only repeated after design and process changes or with subsequent wafer lots.

3/ Parameter is not tested post irradiation

4/ Calculated from 25ºC to -55ºC, 25ºC to 125ºC and -55ºC to 125ºC

5/ Measured from 10% to 90% and 90% to 10% of rail to rail output swing.

TABLE IIA – ELECTRICAL TEST REQUIREMENTS:

Table IIA	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1,2,3 1/ 2/
Group A Test Requirements	1,2,3
Group C end-point electrical parameters	1,2,3 2/
Group D end-point electrical parameters	1,2,3
Group E end-point electrical parameters	1 3/

Table IIA Notes:
1/ PDA applies to Table I subgroup 1 and Table IIB delta parameters.
2/ See Table IIB for delta parameters
3/ Parameters noted in Table IA, IB are not tested post irradiation.

TABLE IIB – LIFE TEST/BURN-IN DELTA LIMITS (V_{SY} = +/-1.8V, V_{SY} = +/-5V & V_{SY} = +/-15V)

Table IIB			
Parameter	Symbol	Delta	Units
Offset voltage	V_{OS}	± 75	µV
Input Bias Current V_{CM} = 0V	I_B	± 2	nA
Supply Current	I_{SY}	± 5	µA

5.0 Burn-In Life Test, and Radiation

5.1. Burn-In Test Circuit, Life Test Circuit

5.1.1. The test conditions and circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 test condition B and alternate test condition D of MIL-STD-883.

5.1.2. HTRB is not applicable for this drawing.

5.2. Radiation Exposure Circuit

5.2.1. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A.

6.0 MIL-PRF-38535 QMLV Exceptions

6.1. Wafer Fabrication

Wafer fabrication occurs at MIL-PRF-38535 QML Class Q certified facility.

6.2. Wafer Lot Acceptance (WLA)

WLA per MIL-STD-883 TM 5007 is not available for this product.

7.0 Application Notes

7.1. General Description

The ADA4096S operational amplifier features micropower operation and rail-to-rail input and output ranges. The extremely low power requirements and guaranteed operation from 3V to 30V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 27 nV/√Hz voltage noise density, recommends them for low power applications. Capacitive loads to 200 pF are handled without oscillation.

The ADA4096S has overvoltage protection inputs and diodes that allow the voltage input to extend 32V above and below the supply rails, making this device ideal for robust industrial applications.

The ADA4096S features a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up; this is called overvoltage protection, or OVP.

7.2. Electrical Characteristics

For reference figures 3 through 44 are typical performance characteristics at T_A = 25°C unless otherwise stated taken from Rev 0 of the ADA4096-2 commercial datasheet.

VSY = +/- 1.5V CHARACTERISTICS

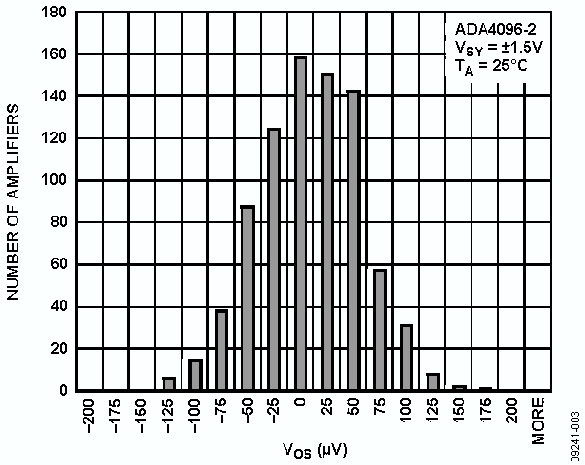

Figure 3. Input Offset Voltage Distribution

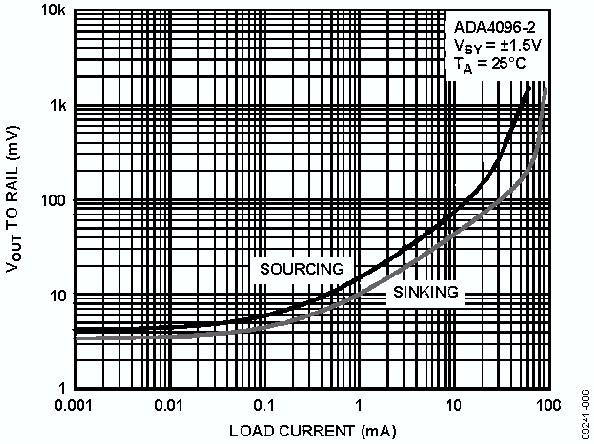

Figure 6. Dropout Voltage vs. Load Current

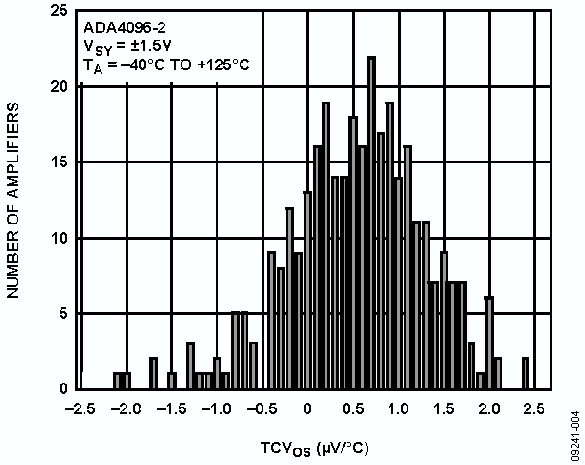

Figure 4. Offset Voltage Drift Distribution

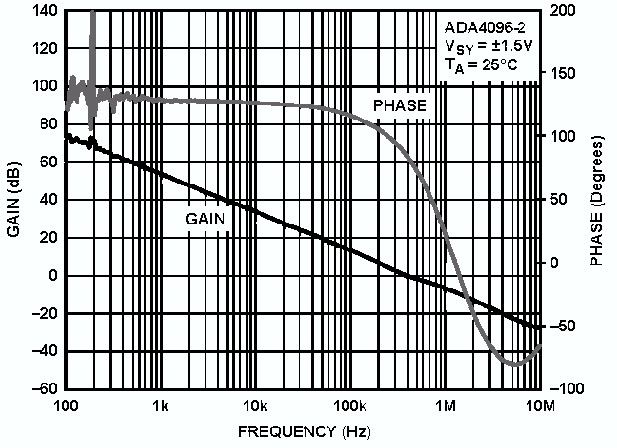

Figure 7. Open-Loop Gain and Phase vs. Frequency

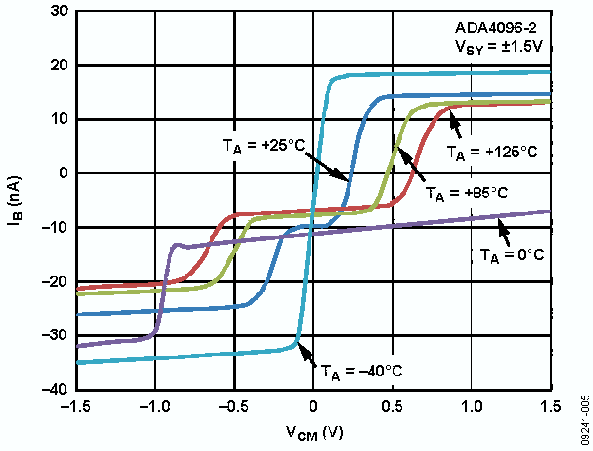

Figure 5. Input Bias Current vs. V_{CM} and Temperature

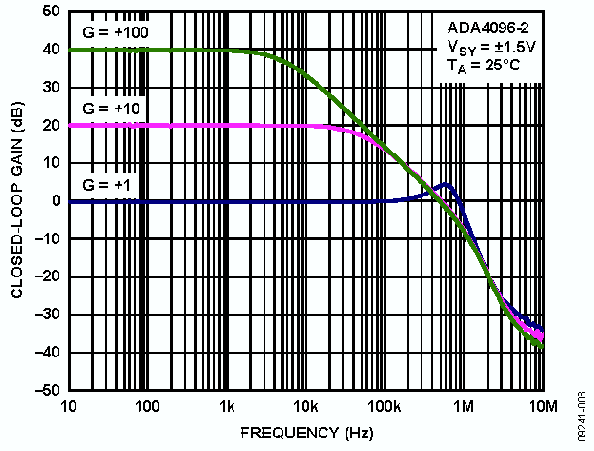

Figure 8. Closed-Loop Gain vs. Frequency

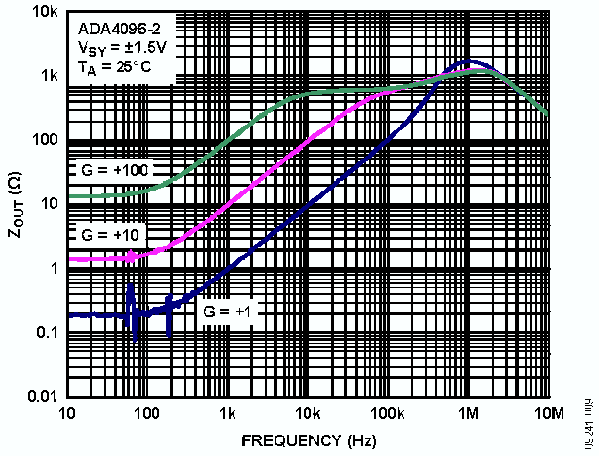

Figure 9. Output Impedance vs. Frequency

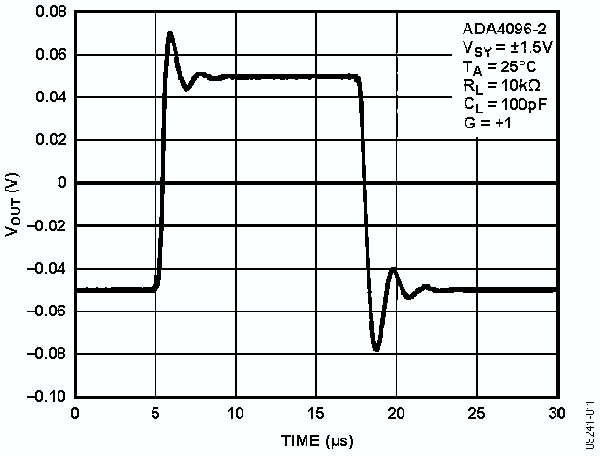

Figure 12. Small Signal Transient Response

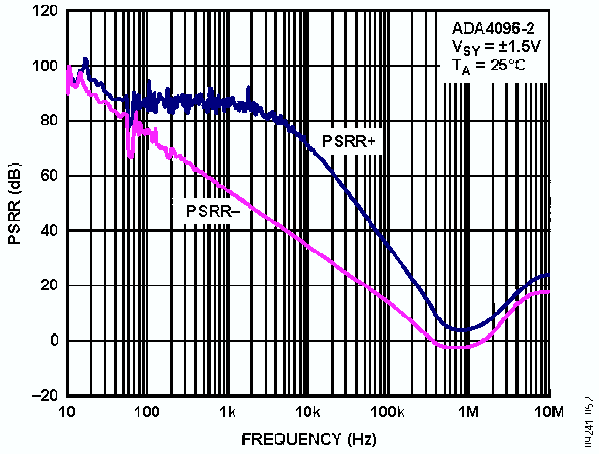

Figure 10. PSRR vs. Frequency

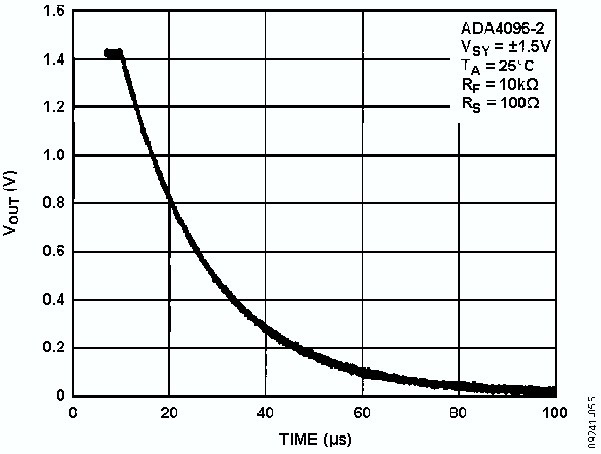

Figure 13. Positive Overload Recovery

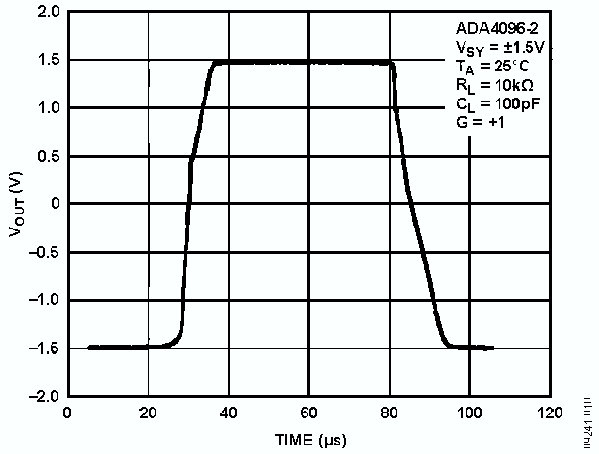

Figure 11. Large Signal Transient Response

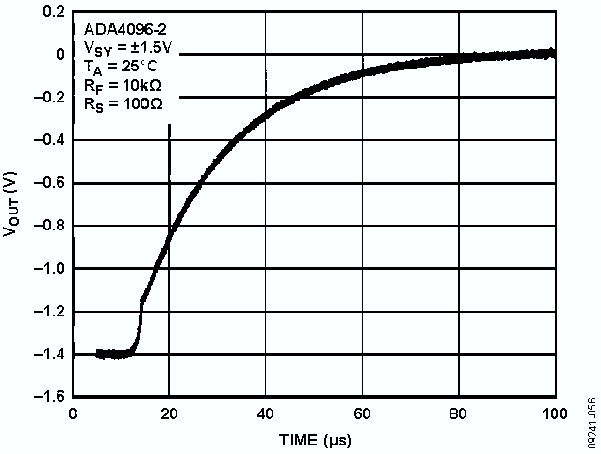

Figure 14. Negative Overload Recovery

VSY = +/- 5V CHARACTERISTICS

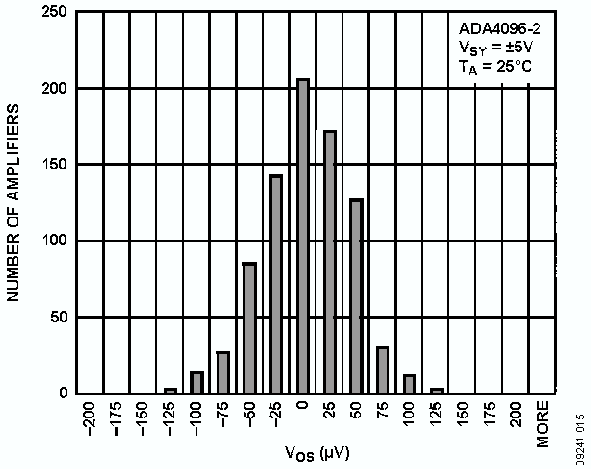

Figure 15. Input Offset Voltage Distribution

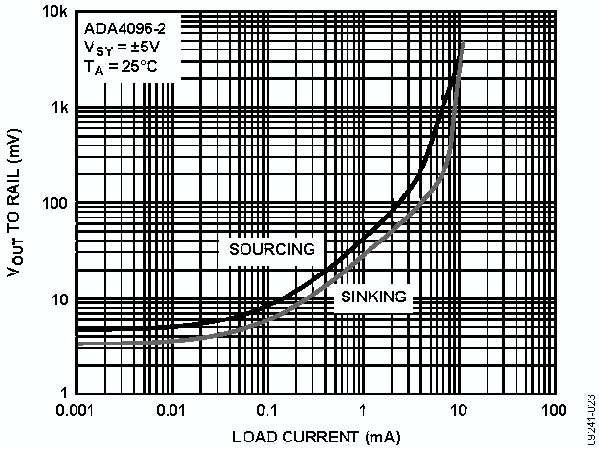

Figure 18. Dropout Voltage vs. Load Current

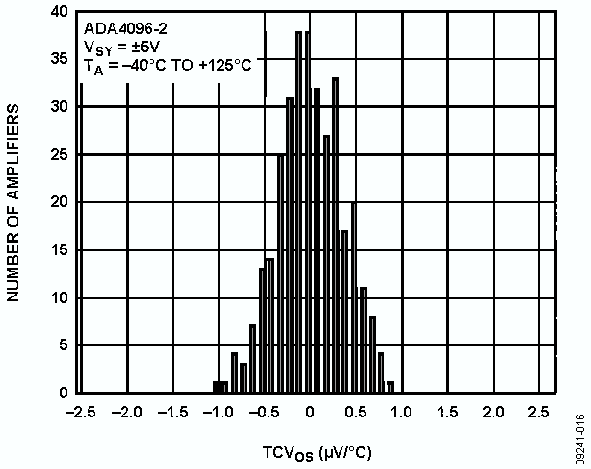

Figure 16. Offset Voltage Drift Distribution

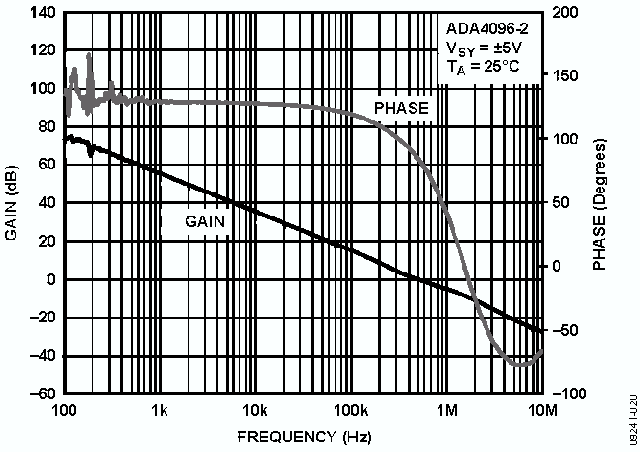

Figure 19. Open Loop Gain and Phase vs. Frequency

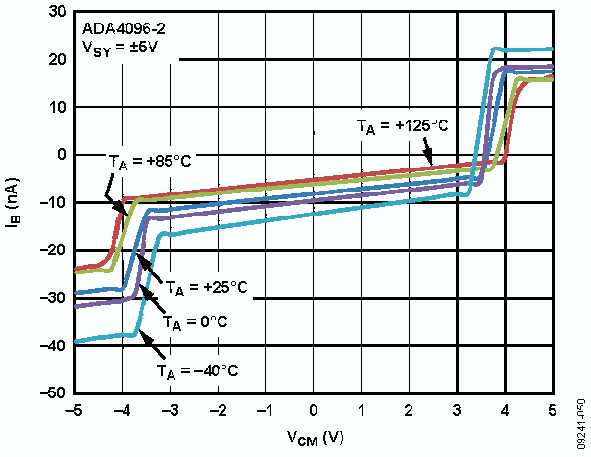

Figure 17. Input Bias Current vs. V_{CM} and Temperature

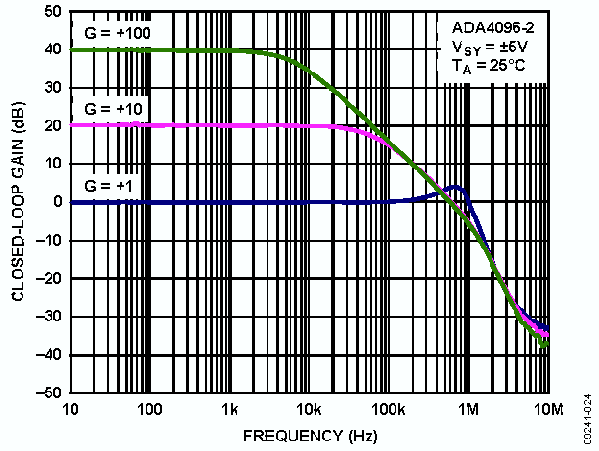

Figure 20. Closed-Loop Gain vs. Frequency

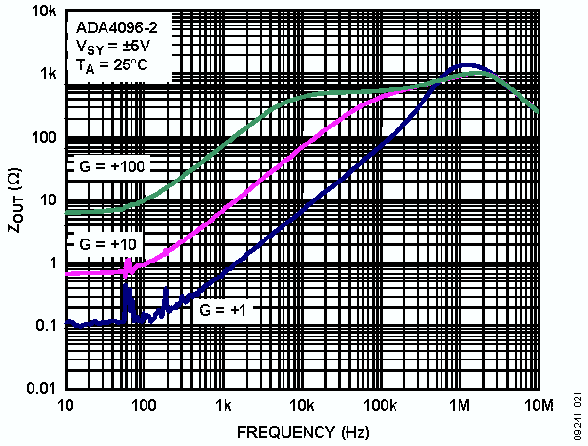

Figure 21. Output Impedance vs. Frequency

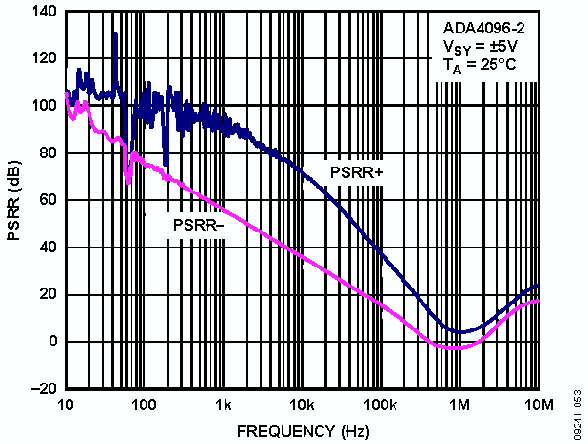

Figure 22. PSRR vs. Frequency

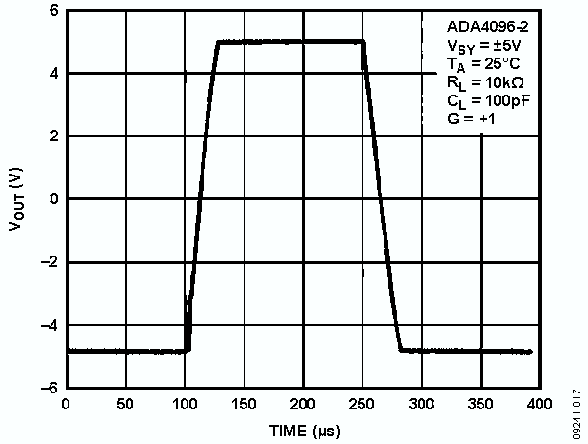

Figure 23. Large Signal Transient Response

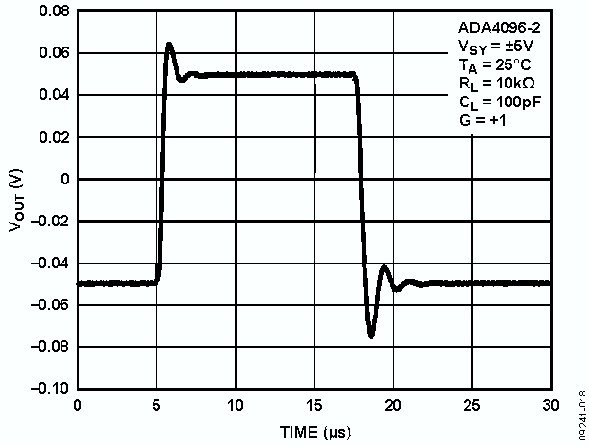

Figure 24. Small Signal Transient Response

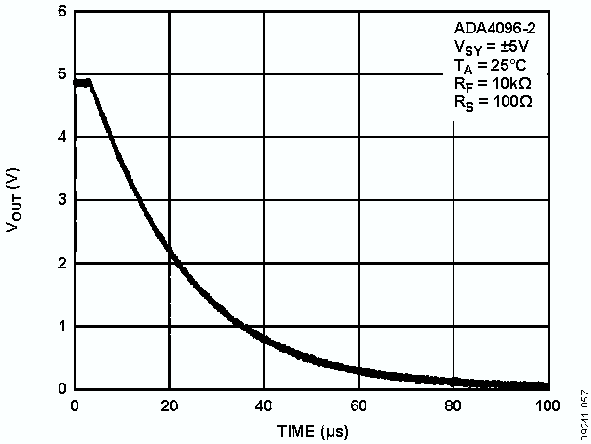

Figure 25. Positive Overload Recovery

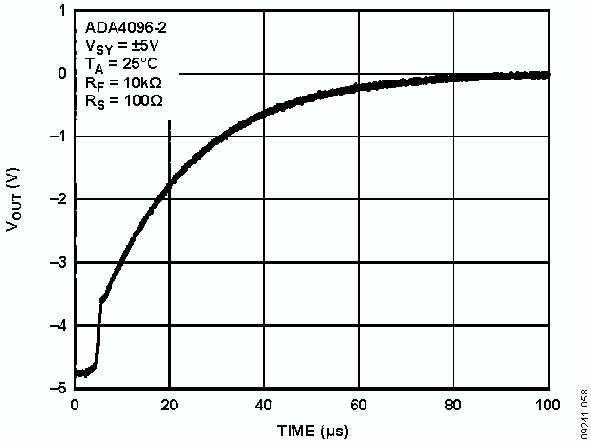

Figure 26. Negative Overload Recovery

VSY = +/- 15V CHARACTERISTICS

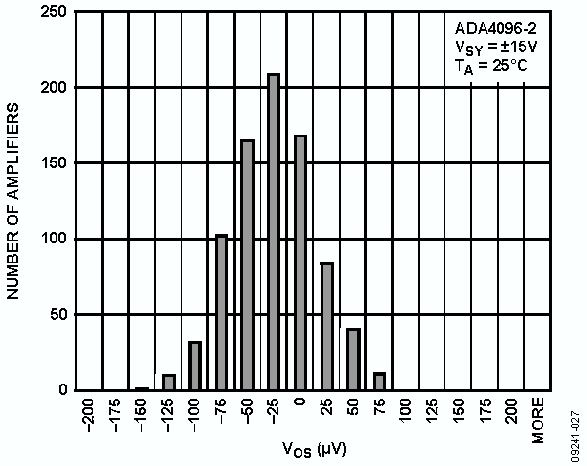

Figure 27. Input Offset Voltage Distribution

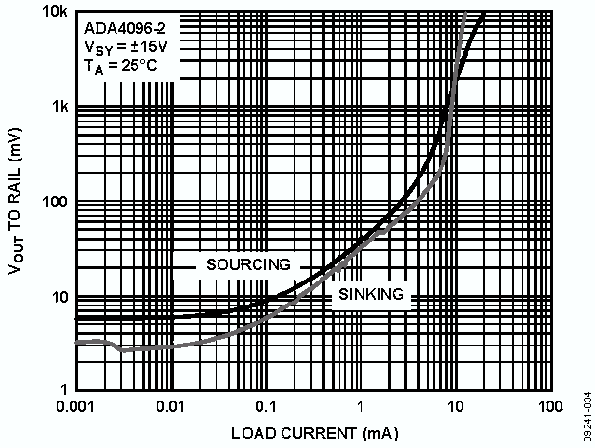

Figure 30. Dropout Voltage vs. Load Current

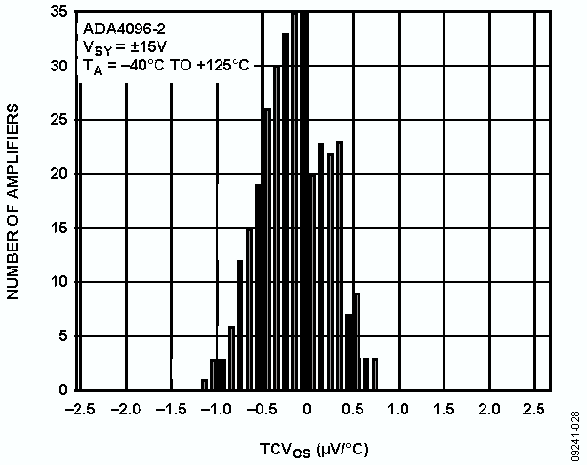

Figure 28. Offset Voltage Drift Distribution

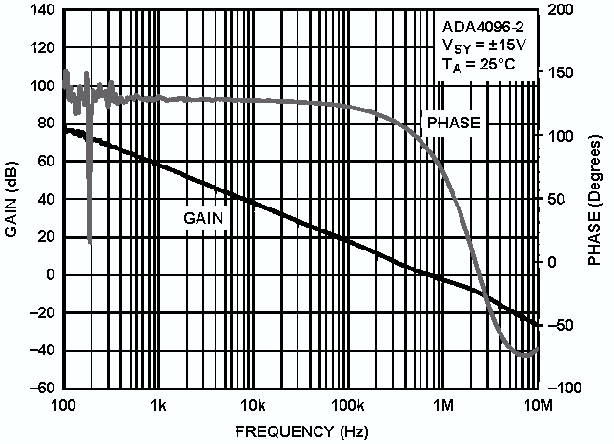

Figure 31. Open-Loop Gain and Phase vs. Frequency

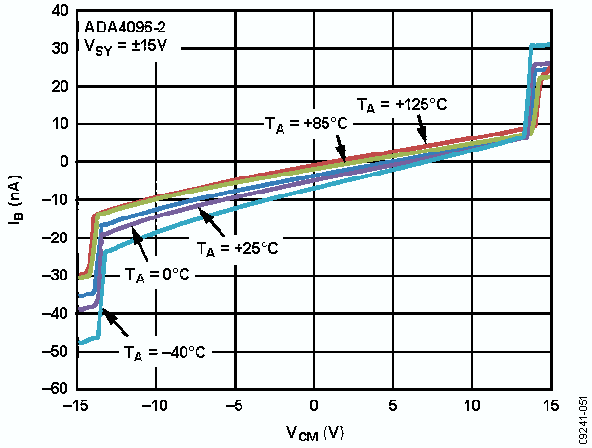

Figure 29. Input Bias Current vs. V_{CM} and Temperature

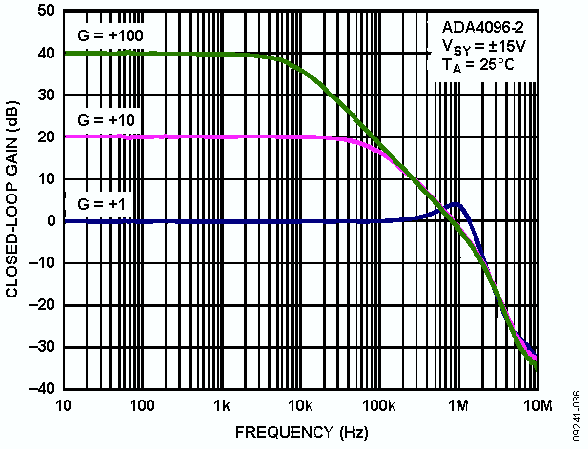

Figure 32. Closed-Loop Gain vs. Frequency

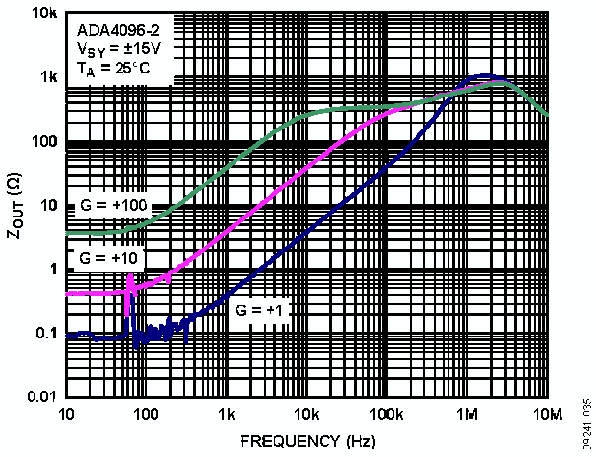

Figure 33. Output impedance vs. Frequency

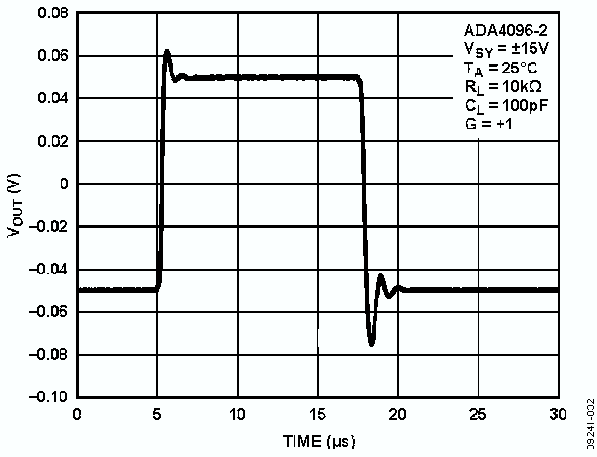

Figure 36. Small Signal Transient Response

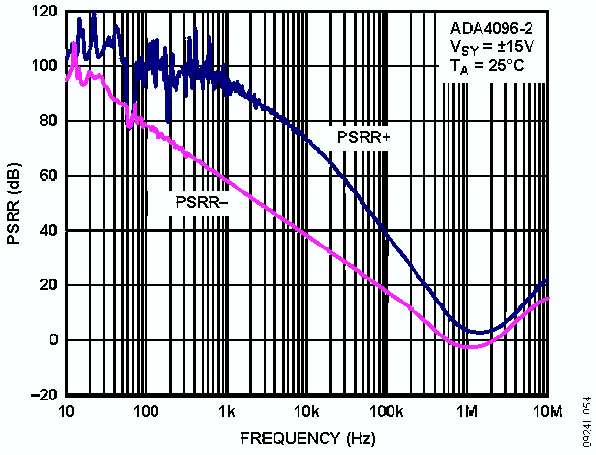

Figure 34. PSRR vs. Frequency

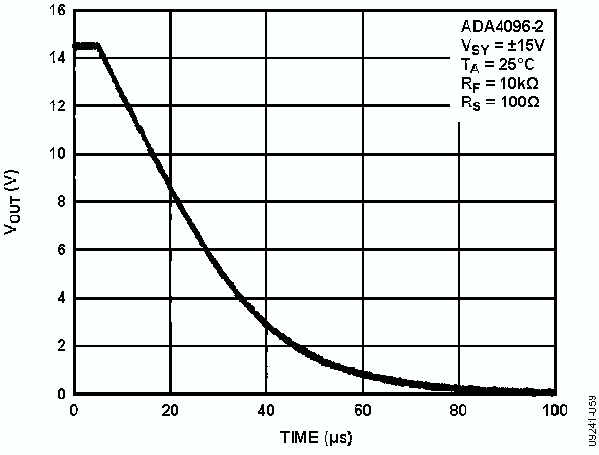

Figure 37. Positive Overload Recovery

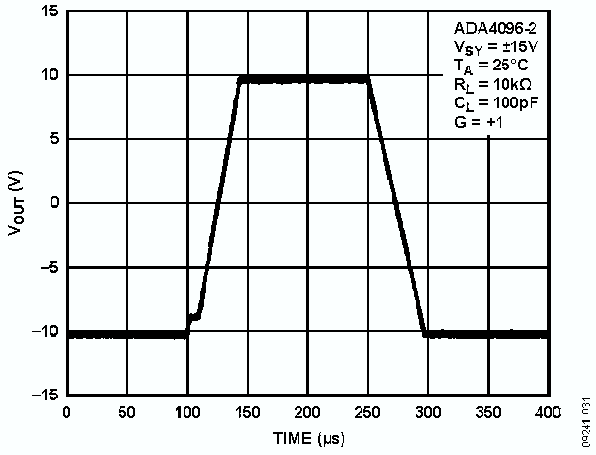

Figure 35. Large Signal Transient Response

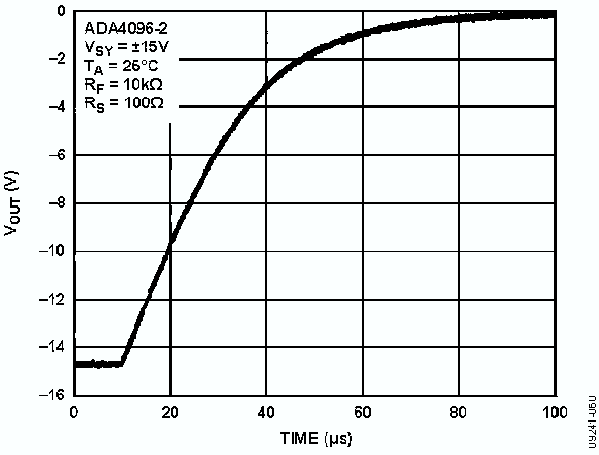

Figure 38. Negative Overload Recovery

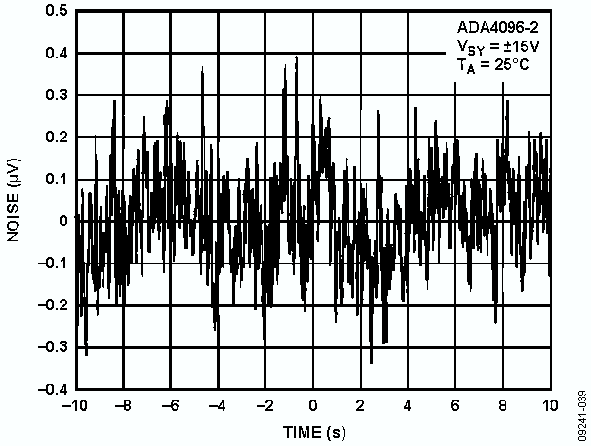

Figure 39. Input Voltage Noise, 0.1 Hz to 10 Hz Bandwidth

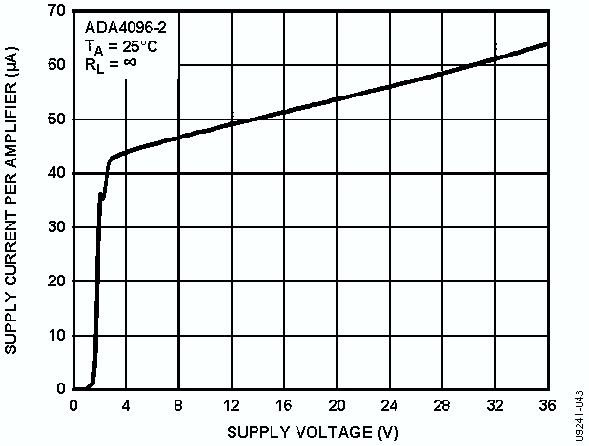

Figure 42. Supply Current vs. Supply Voltage

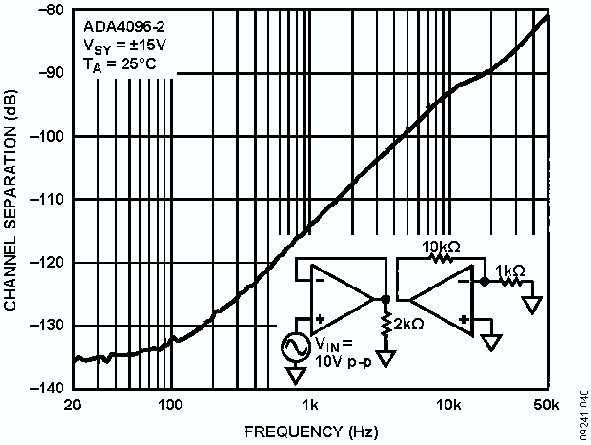

Figure 40. Channel Separation vs. Frequency

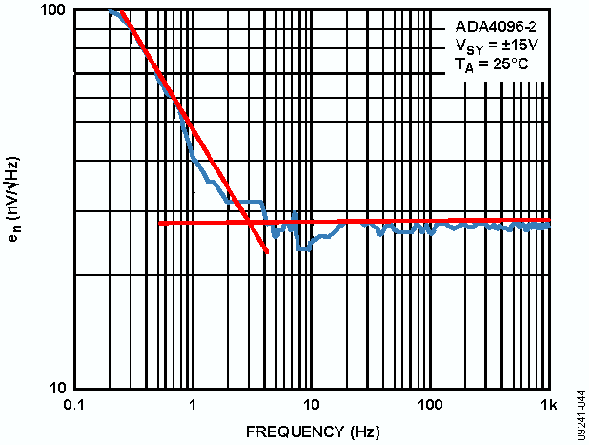

Figure 43. Voltage Noise Density

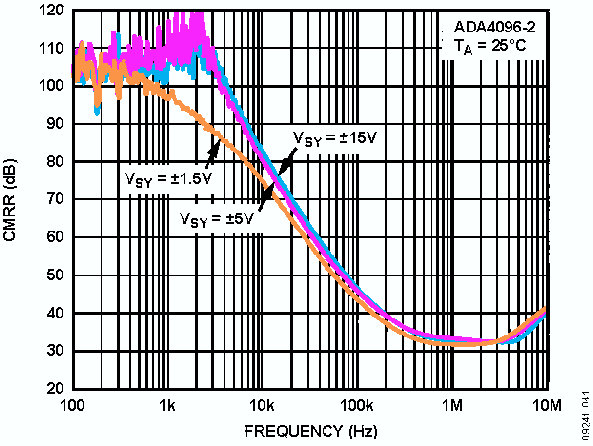

Figure 41. CMRR vs. Frequency

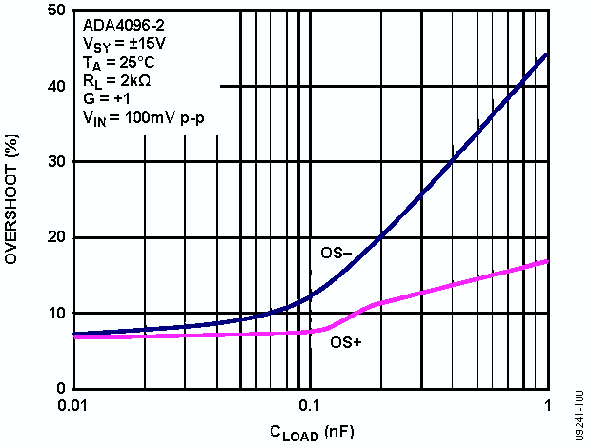

Figure 44. Overshoot vs. Load Capacitance

7.3. INPUT STAGE

Figure 45 shows a simplified schematic of the ADA4096S. The input stage comprises two differential pairs (Q1 to Q4 and Q5 to Q8) operating in parallel. When the input common-mode voltage approaches V_{CC} -1.5V, Q1 to Q4 shut down as I1 reaches its minimum voltage compliance. Conversely, when the input common-mode voltage approaches V_{EE} + 1.5V, Q5 to Q8 shut down as I2 reaches its minimum voltage compliance. This topology allow for maximum input dynamic range because the amplifier can function with its inputs at 200 mV outside the rails (at room temperature).

As with any rail-to-rail input amplifier, V_{OS} mismatch between the two input pairs determines the CMRR of the amplifier. If the input common-mode voltage range is kept within 1.5V of each rail, transitions between the input pairs are avoided, thus improving the CMRR by approximately 10 dB (see Table IB and IC).

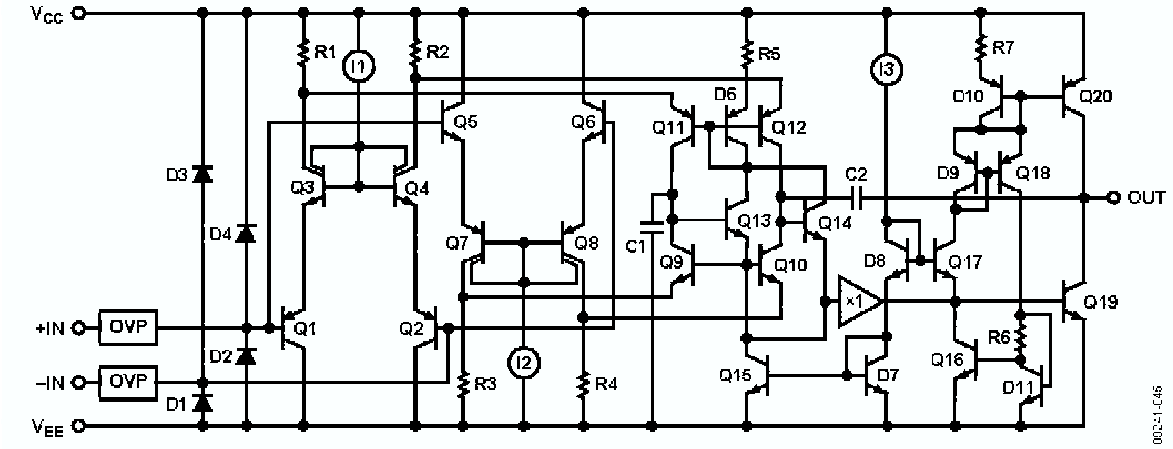

Figure 45. Simplified Schematic

7.4. PHASE INVERSION

Some single-supply amplifiers exhibit phase inversion when the input signal extends beyond the common-mode voltage range of the amplifier. When the input devices become saturated, the inverting and non-inverting inputs exchange functions, causing the output to move in the opposing direction.

Although phase inversion persists for only as long as the inputs are saturated, it can be detrimental to applications where the amplifier is part of a closed-loop system. **The ADA4096S is free from phase inversion over the entire common-mode voltage range, as well as the overvoltage protected range stated in the Absolute Maximum Ratings.** Figure 46 shows the ADA4096S in a unity-gain configuration with the input signal at +/-40V and the amplifier supplies at +/-10V.

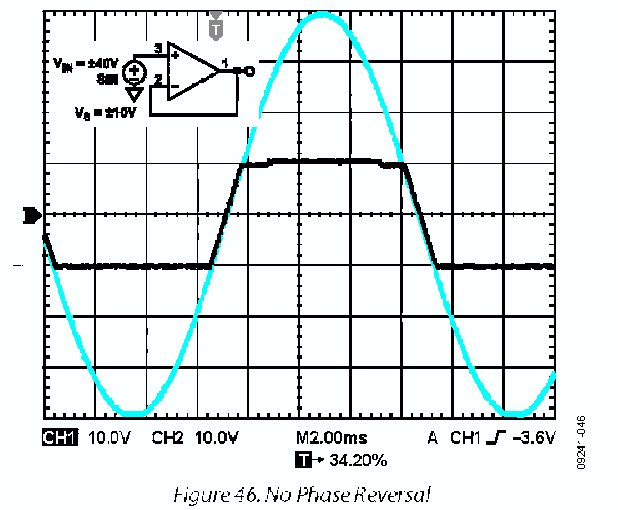

Figure 46. No Phase Reversal

7.5. INPUT OVERLOAD PROTECTION

The ADA4096S inputs are protected from input voltage excursions up to 32V outside each rail. This feature is of particular importance in applications with power supply sequencing issues that could cause the signal source to be active before these supplies to the amplifier. Figure 47 shows the input current limiting capability of the ADA4096S compared to using a 5 kΩ series resistor (red curves).

Figure 47 was generated with the ADA4096S in a buffer configuration with the supplies connected to GND (or +/-15V) and the positive input swept until it exceeds the supplies by 32V. In general, input current is limited to 1 mA during positive overvoltage conditions and 200 µA during negative under voltage conditions. For example, at an overvoltage of 20V, the ADA4096S input current is limited to 1 mA, providing a current limit equivalent to a series 20 kΩ resistor. Figure 47 also shows that the current limiting circuitry is active whether the amplifier is powered or not.

Note that Figure 47 represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table I.

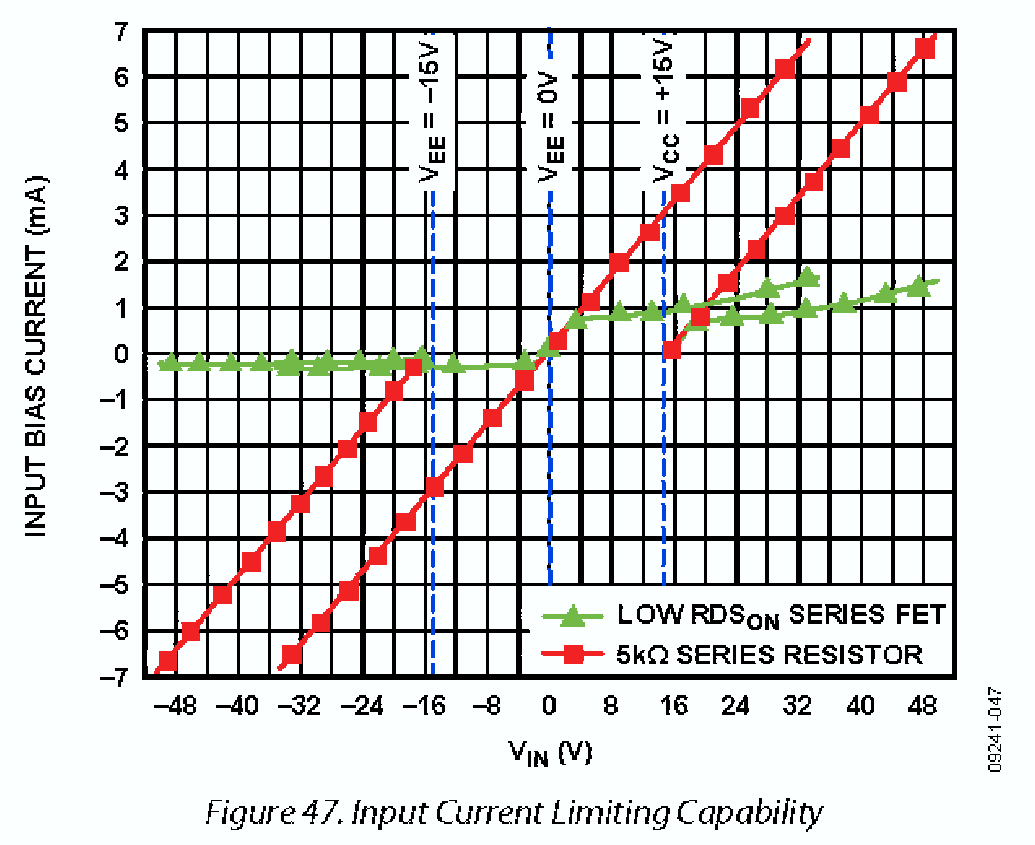

Figure 47. Input Current Limiting Capability

7.6. COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be pressed into service as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop, but it cannot, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 48).

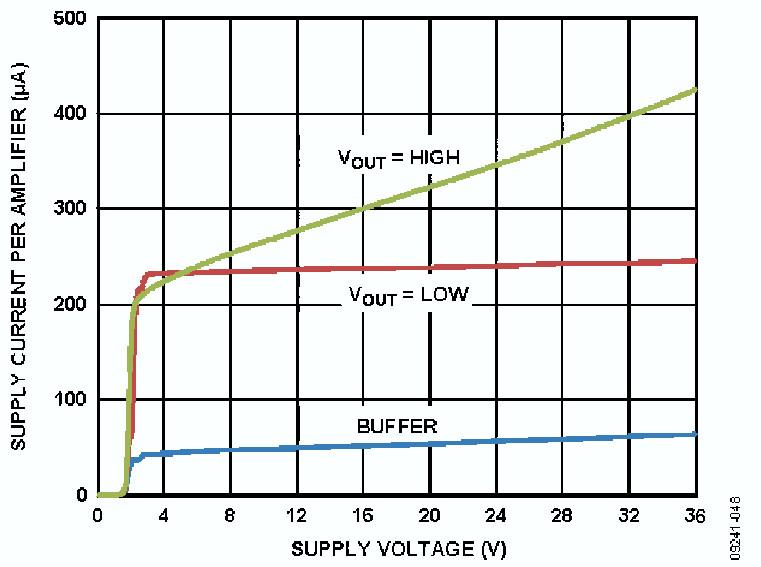

Figure 48. Comparator Supply Current

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4096R703F	−55°C to +125°C	10 Lead Bottom Brazed Flat Pack	CDFP3-F10

Revision History		
Rev	Description of Change	Date
A	Initial Release	July 9, 2013
B	Update NC/GND pin name and characterization note to latest standards.	Aug 2, 2013

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