

## 17-24GHz Down Converter

### GaAs Monolithic Microwave IC in SMD leadless package

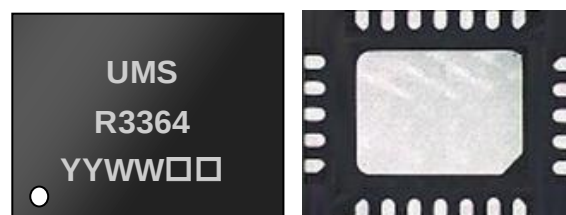
#### Description

The CHR3364-QEG is a multifunction monolithic receiver, which integrates a balanced cold FET mixer, a LO chain with buffers associated to a time two multiplier, and a RF low noise amplifier including gain control.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

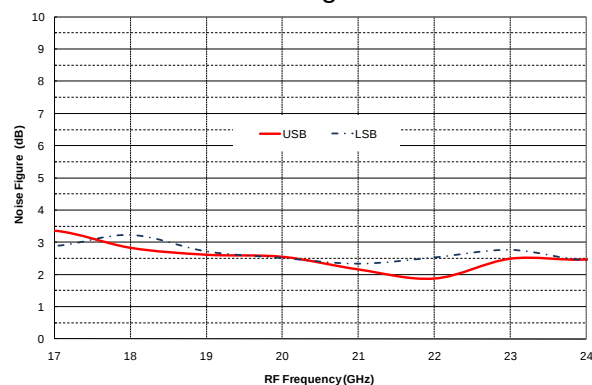
It is supplied in RoHS compliant SMD package.



#### Main Features

- Broadband performances: 17-24GHz
- 11dB Conversion gain
- 17dBc Image Rejection
- 1dBm Input IP3
- 2.7dB Noise Figure for IF>0.1GHz
- 0dBm LO input Power
- DC bias: Vd=4V @ Id=320mA
- 24L-QFN4x5
- MSL1

Noise figure



#### Main Electrical Characteristics

Tamb.= +25°C

| Symbol          | Parameter          | Min  | Typ  | Max  | Unit |
|-----------------|--------------------|------|------|------|------|
| F <sub>RF</sub> | RF frequency range | 17.0 |      | 24.0 | GHz  |
| F <sub>LO</sub> | LO frequency range | 6.5  |      | 14.0 | GHz  |
| F <sub>IF</sub> | IF frequency range | DC   |      | 3.5  | GHz  |
| C <sub>G</sub>  | Conversion gain    |      | 11.0 |      | dB   |

## Electrical Characteristics

T<sub>amb.</sub> = +25°C, V<sub>D</sub> = V<sub>DL</sub> = 4.0V

| Symbol          | Parameter                             | Min | Typ  | Max | Unit |
|-----------------|---------------------------------------|-----|------|-----|------|
| F <sub>RF</sub> | RF frequency range                    | 17  |      | 24  | GHz  |
| F <sub>LO</sub> | LO frequency range                    | 6.5 |      | 14  | GHz  |
| F <sub>IF</sub> | IF frequency range                    | DC  |      | 3.5 | GHz  |
| C <sub>G</sub>  | Conversion Gain                       |     | 11   |     | dB   |
| NF              | Noise Figure for IF>0.1GHz            |     | 2.7  |     | dB   |
| Im_rej          | Image rejection <sup>(1)</sup>        |     | 17   |     | dBc  |
| P <sub>LO</sub> | LO Input power                        |     | 0    |     | dBm  |
| IIP3            | Input IP3                             |     | 1    |     | dBm  |
| 2LO/RF          | 2LO leakage at RF port                |     | -40  |     | dBc  |
| VD, VDL         | DC drain voltage                      |     | 4.0  |     | V    |
| ID              | Drain current on VD pin for LO buffer |     | 245  |     | mA   |
| IDL             | Drain current on VDL pin for LNA      |     | 75   |     | mA   |
| VGL             | LNA DC gate voltage <sup>(2)</sup>    |     | -0.5 |     | V    |
| VGM             | Mixer DC gate voltage                 |     | -0.7 |     | V    |

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

<sup>(1)</sup> An external combiner 90° is required on I / Q.

<sup>(2)</sup> Typical VGL value for IDL = 75mA

See in paragraph "biasing option" other possibility to optimise differently the performances

## Absolute Maximum Ratings <sup>(1)</sup>

T<sub>amb.</sub> = +25°C

| Symbol           | Parameter                                            | Values      | Unit |
|------------------|------------------------------------------------------|-------------|------|
| VD, VDL          | Drain bias voltage                                   | 5           | V    |
| ID+IDL           | Drain bias current                                   | 430         | mA   |
| VGL              | LNA Gate bias voltage                                | -2 to +0.4  | V    |
| VGM              | Mixer Gate bias voltage                              | -2 to +0.4  | V    |
| P <sub>RF</sub>  | Maximum peak RF input power overdrive <sup>(2)</sup> | +10         | dBm  |
| P <sub>LO</sub>  | Maximum peak LO input power overdrive <sup>(2)</sup> | +10         | dBm  |
| T <sub>j</sub>   | Junction temperature                                 | 175         | °C   |
| T <sub>a</sub>   | Operating temperature range                          | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage temperature range                            | -55 to +150 | °C   |

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

<sup>(2)</sup> Duration < 1s.

## Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve P<sub>diss. Max.</sub>) in order to guarantee the nominal device life time (MTTF).

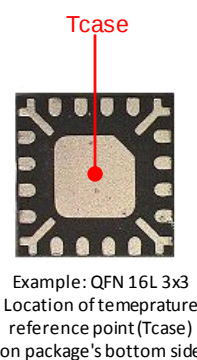
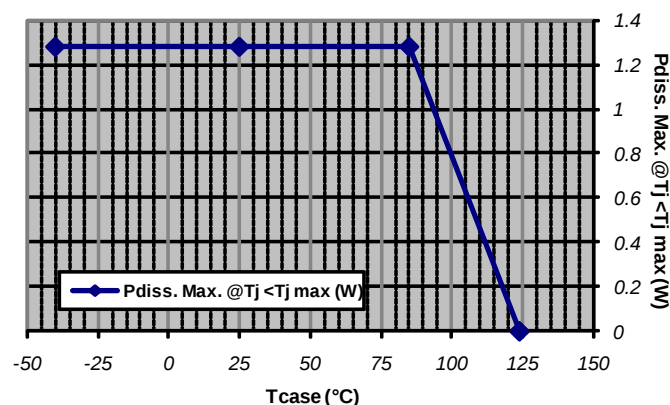
### DEVICE THERMAL SPECIFICATION : CHR3364-QEG

|                                                                                    |   |          |
|------------------------------------------------------------------------------------|---|----------|
| Recommended max. junction temperature (T <sub>j</sub> max)                         | : | 124 °C   |
| Junction temperature absolute maximum rating                                       | : | 175 °C   |
| Max. continuous dissipated power (P <sub>diss. Max.</sub> )                        | : | 1.3 W    |
| => P <sub>diss. Max.</sub> derating above T <sub>case</sub> <sup>(1)</sup> = 85 °C | : | 33 mW/°C |
| Junction-Case thermal resistance (R <sub>th J-C</sub> ) <sup>(2)</sup>             | : | <30 °C/W |
| Minimum T <sub>case</sub> operating temperature <sup>(3)</sup>                     | : | -40 °C   |
| Maximum T <sub>case</sub> operating temperature <sup>(3)</sup>                     | : | 85 °C    |
| Minimum storage temperature                                                        | : | -55 °C   |
| Maximum storage temperature                                                        | : | 150 °C   |

(1) Derating at junction temperature constant = T<sub>j</sub> max.

(2) R<sub>th J-C</sub> is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.

(3) T<sub>case</sub>=Package back side temperature measured under the die-attach-pad (see the drawing below).

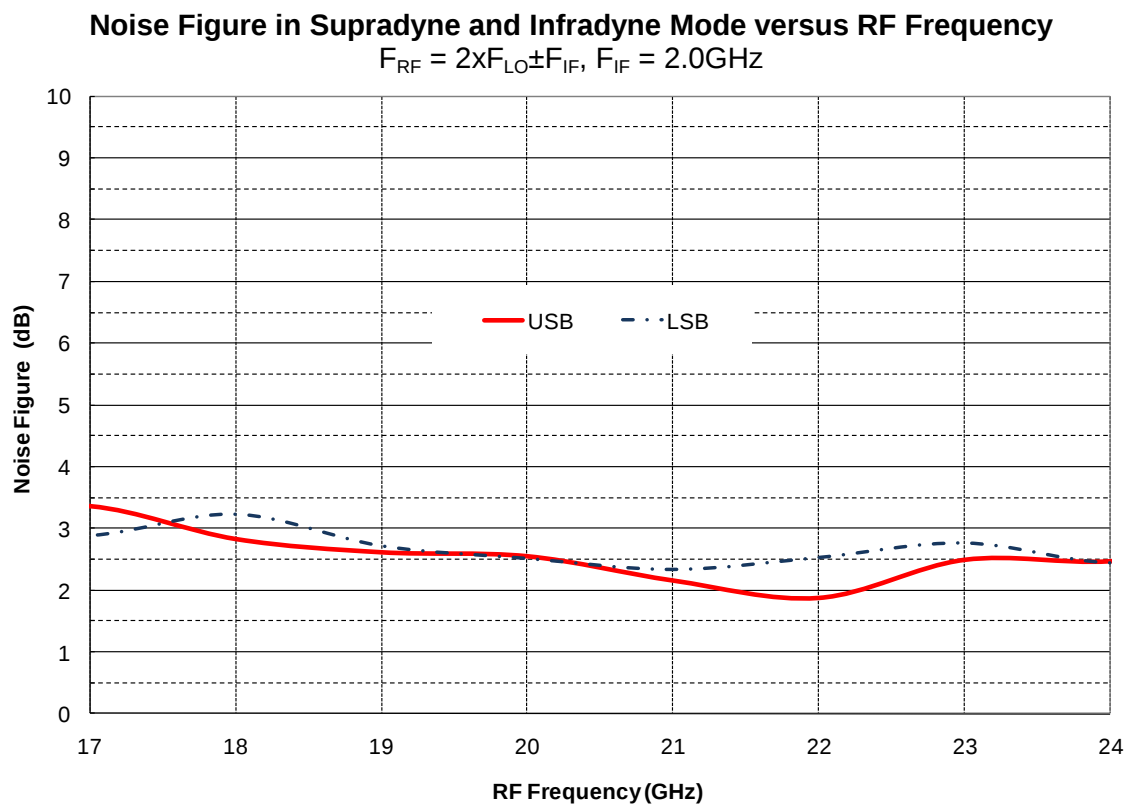


6.0

### Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P<sub>LO</sub> = 0dBm

The values shown on the following pages are representative of on-board measurements where results are given on package access planes.

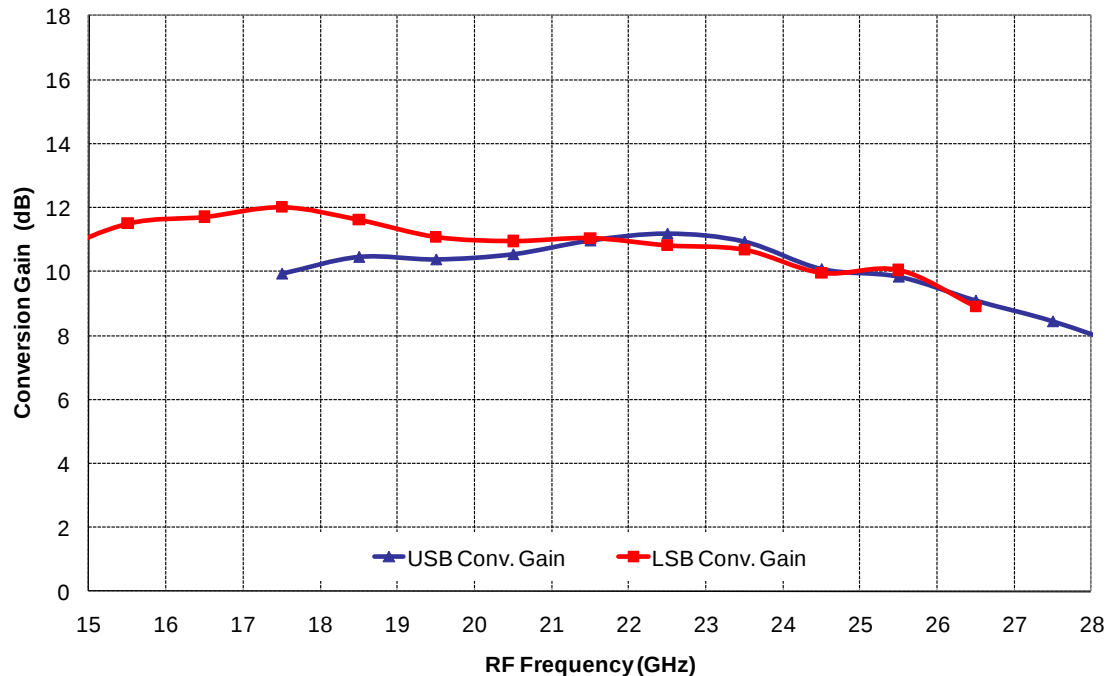


## Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P<sub>LO</sub> = 0dBm

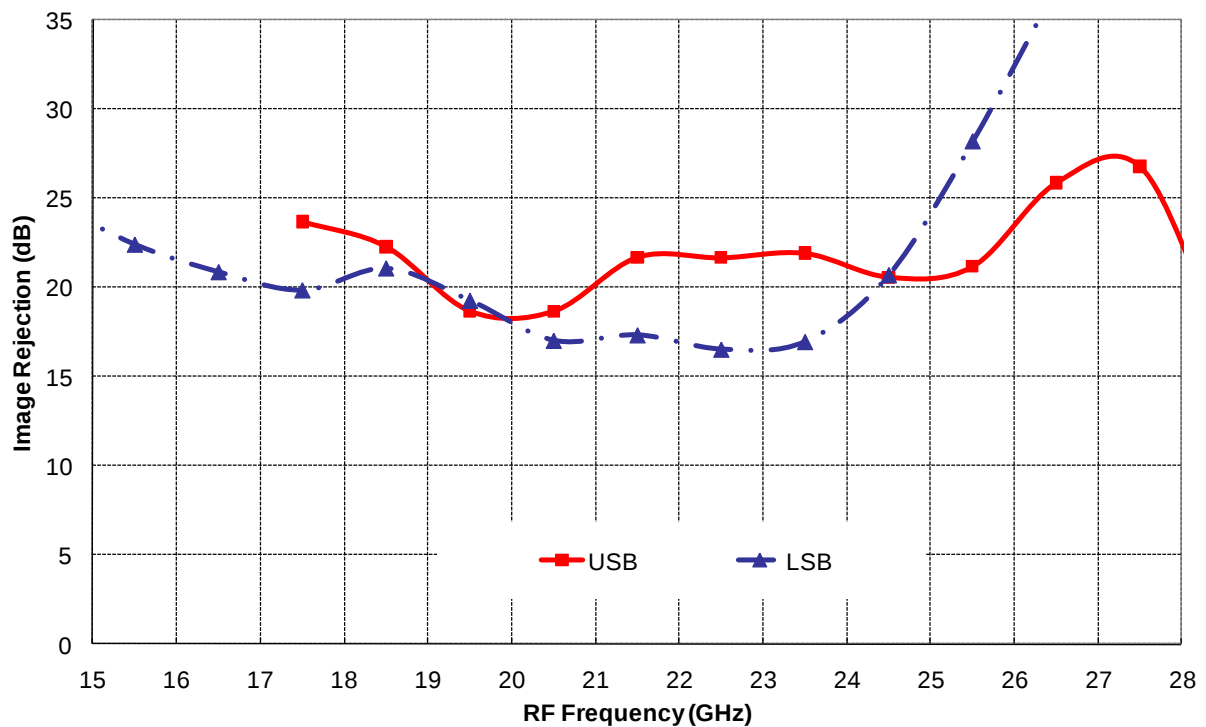
### Conversion Gain in Supradynne and Infradyne Mode versus RF Frequency

$$F_{RF} = 2xF_{LO} \pm F_{IF}, F_{IF} = 3.5\text{GHz}$$



### Image Rejection versus RF Frequency

$$F_{RF} = 2xF_{LO} \pm F_{IF}, F_{IF} = 3.5\text{GHz}$$

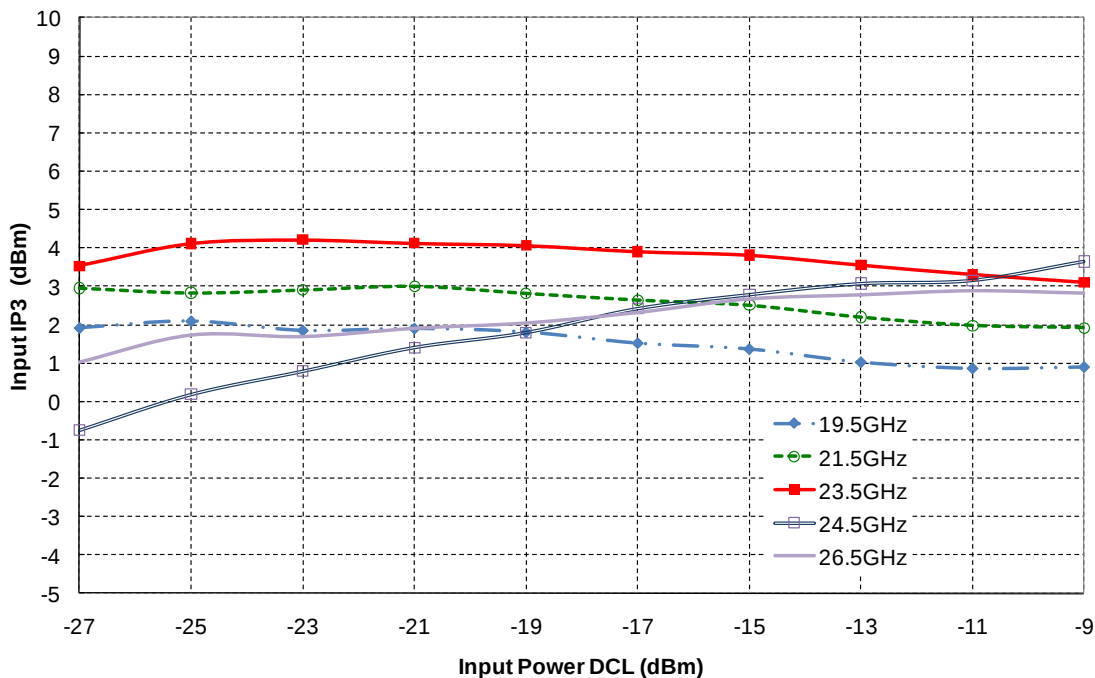


### Typical Board Measurements

Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P<sub>LO</sub> = 0dBm

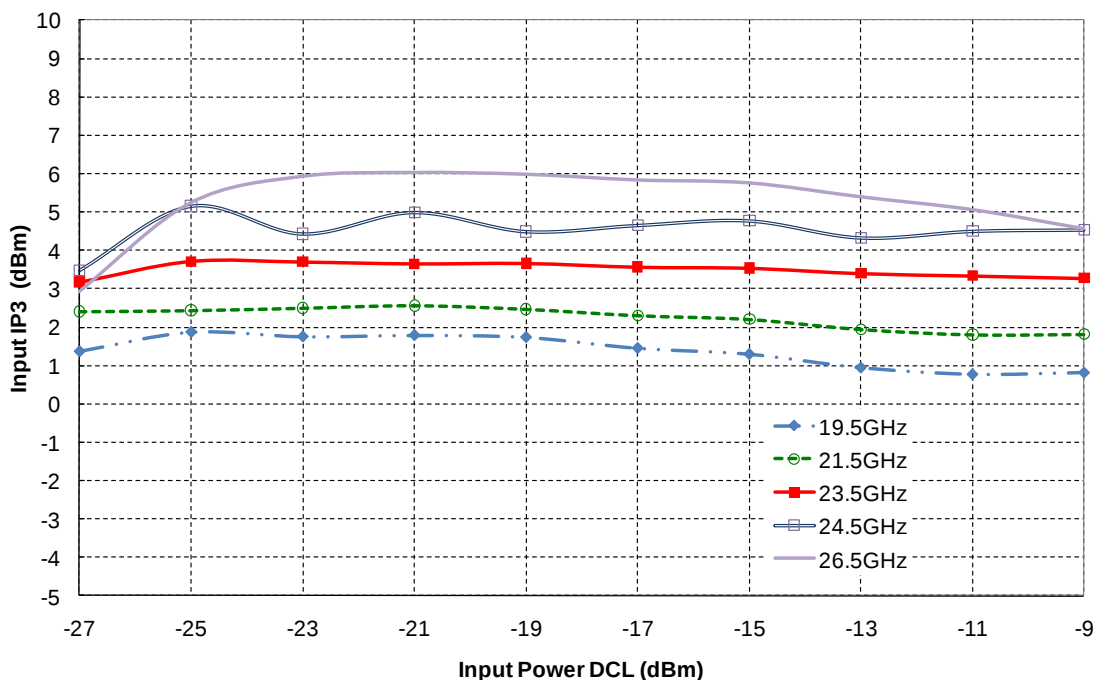
#### Input IP3 in Supradyn Mode versus RF Frequency

$$F_{RF} = 2 \times F_{LO} + F_{IF}, F_{IF} = 3.5\text{GHz}$$



#### Input IP3 in Infradyne Mode versus RF Frequency

$$F_{RF} = 2 \times F_{LO} - F_{IF}, F_{IF} = 3.5\text{GHz}$$

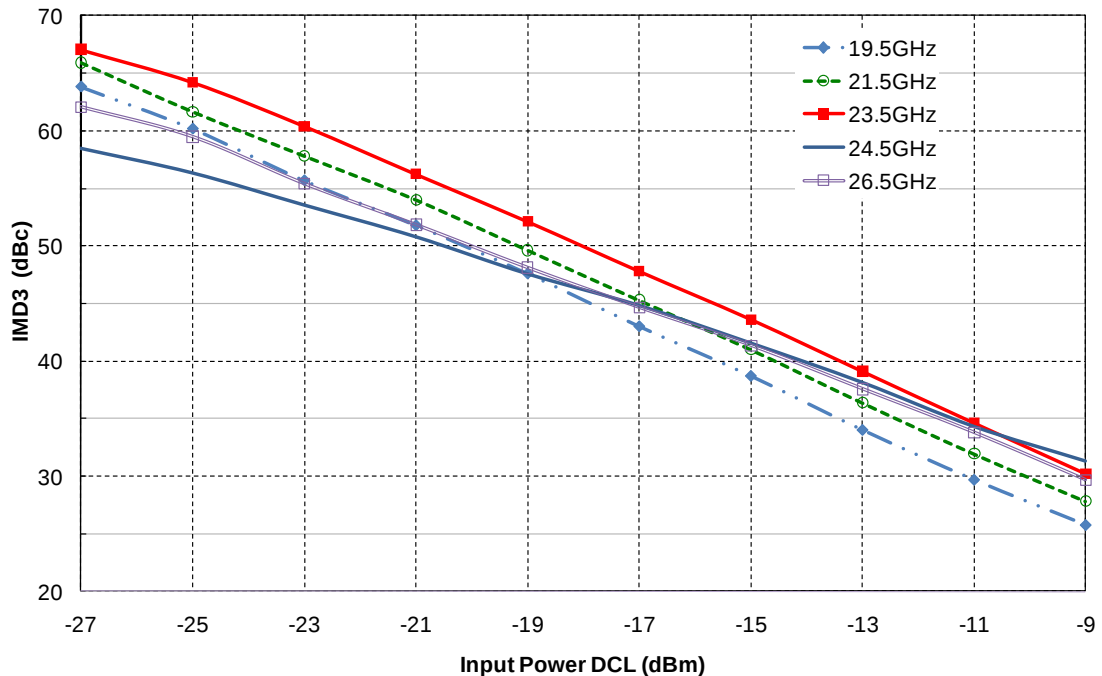


## Typical Board Measurements

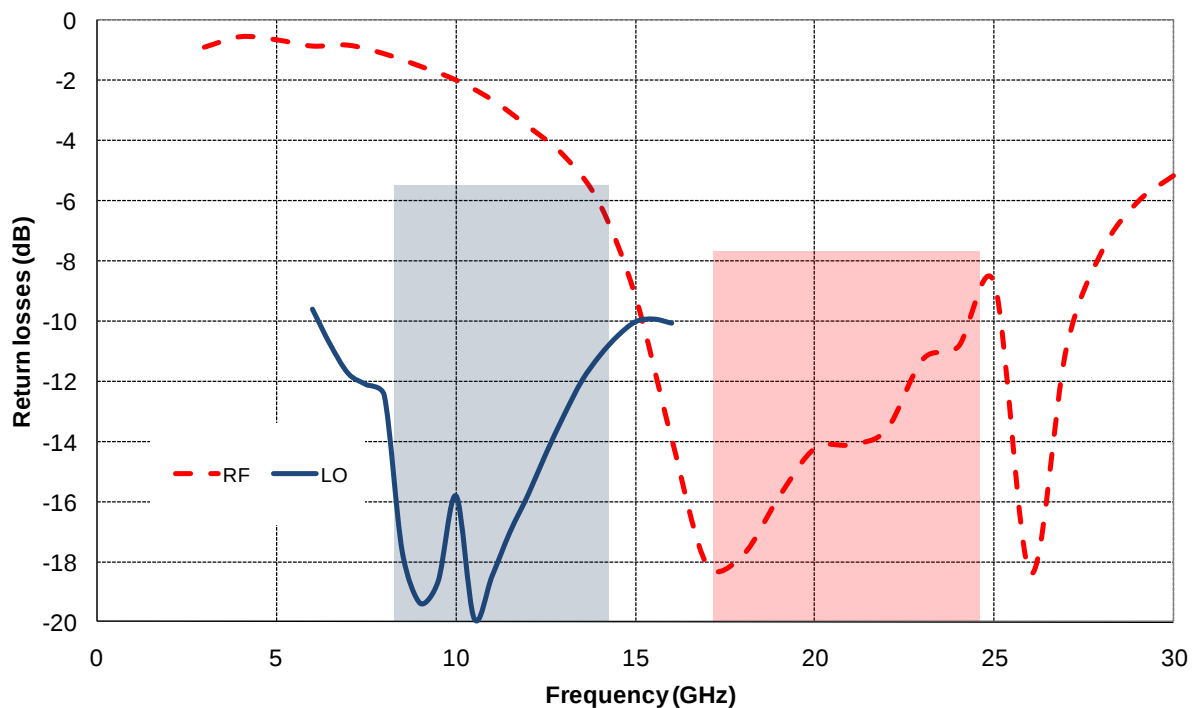
Tamb = +25°C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P<sub>LO</sub> = 0dBm

### IMD3 in Supradyn Mode versus RF Frequency

$$F_{RF} = 2 \times F_{LO} + F_{IF}, F_{IF} = 3.5\text{GHz}$$



### LO & RF return loss versus frequency

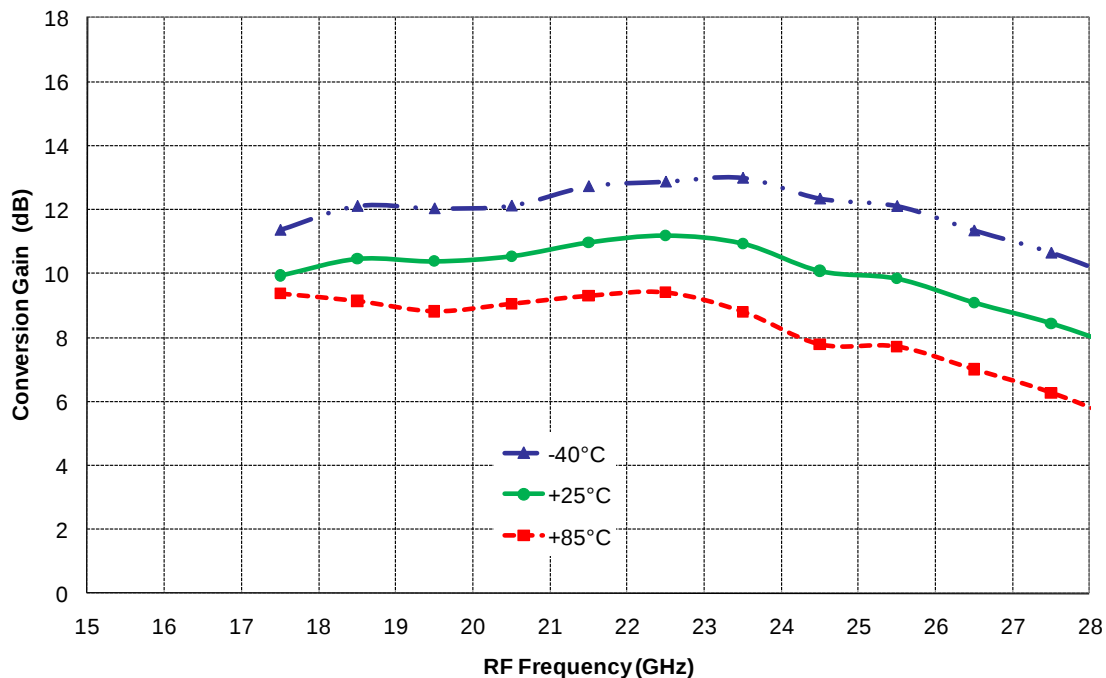


### Temperature Board Measurements

T = [-40, +25, +85] °C, VD = VDL = 4.0V, VGL = -0.5V, VGM = -0.7V, P<sub>LO</sub> = 0dBm

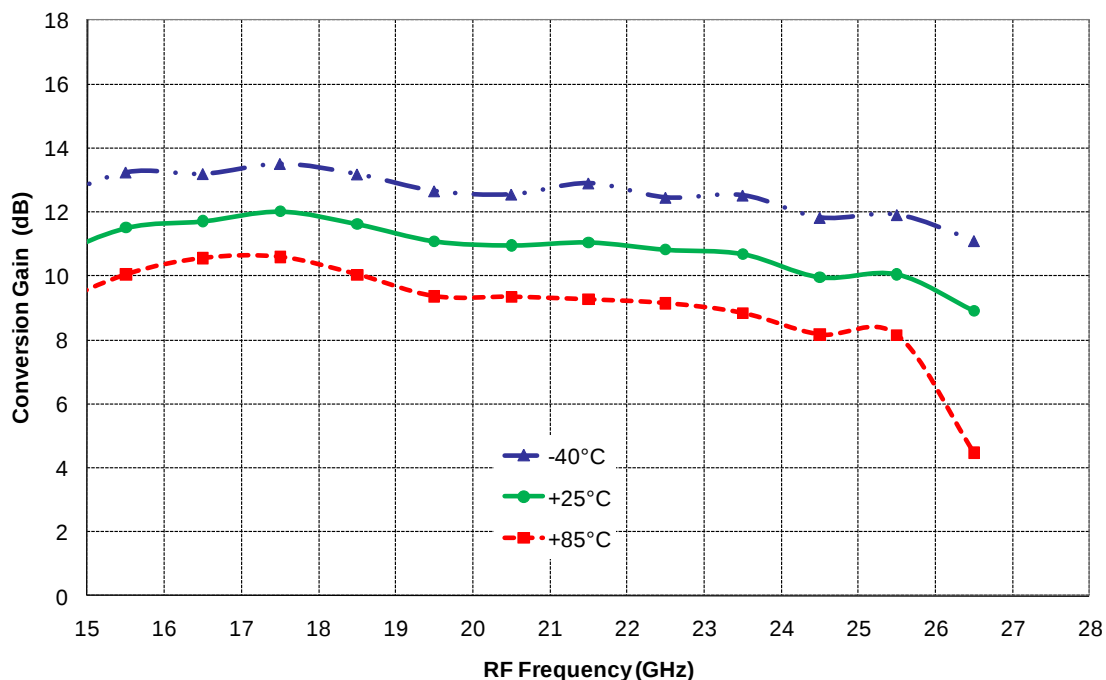
#### Conversion Gain in Supradyn Mode versus RF Frequency

$$F_{RF} = 2 \times F_{LO} + F_{IF}, F_{IF} = 3.5\text{GHz}$$



#### Conversion Gain in Infradyne Mode versus RF Frequency

$$F_{RF} = 2 \times F_{LO} - F_{IF}, F_{IF} = 3.5\text{GHz}$$

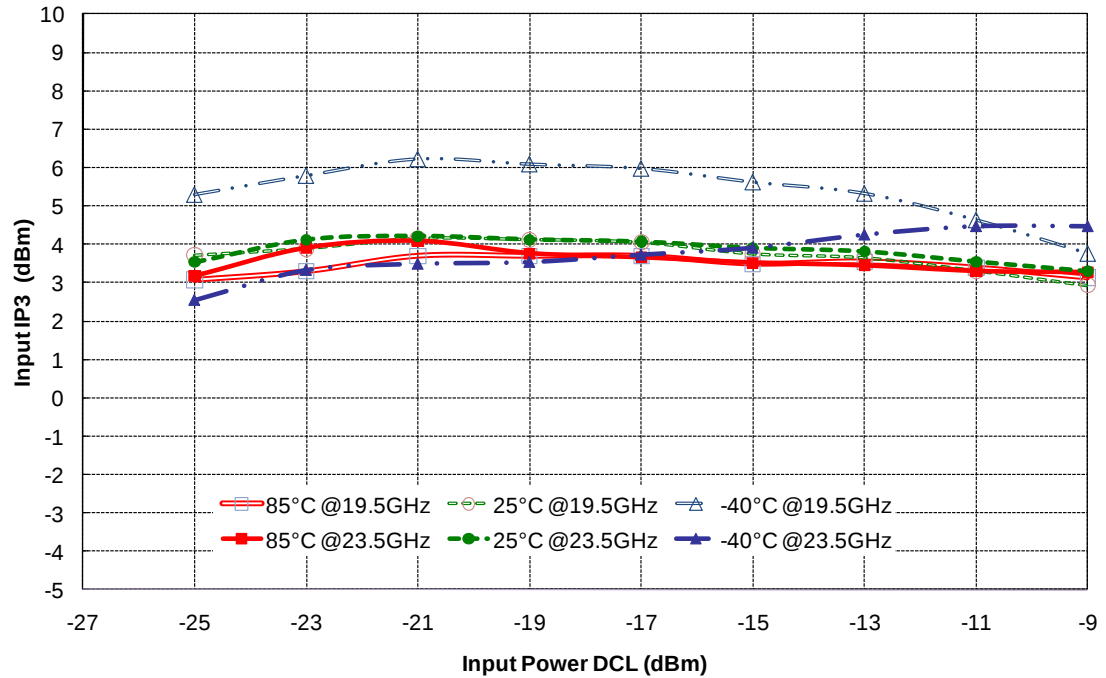


## Temperature Board Measurements

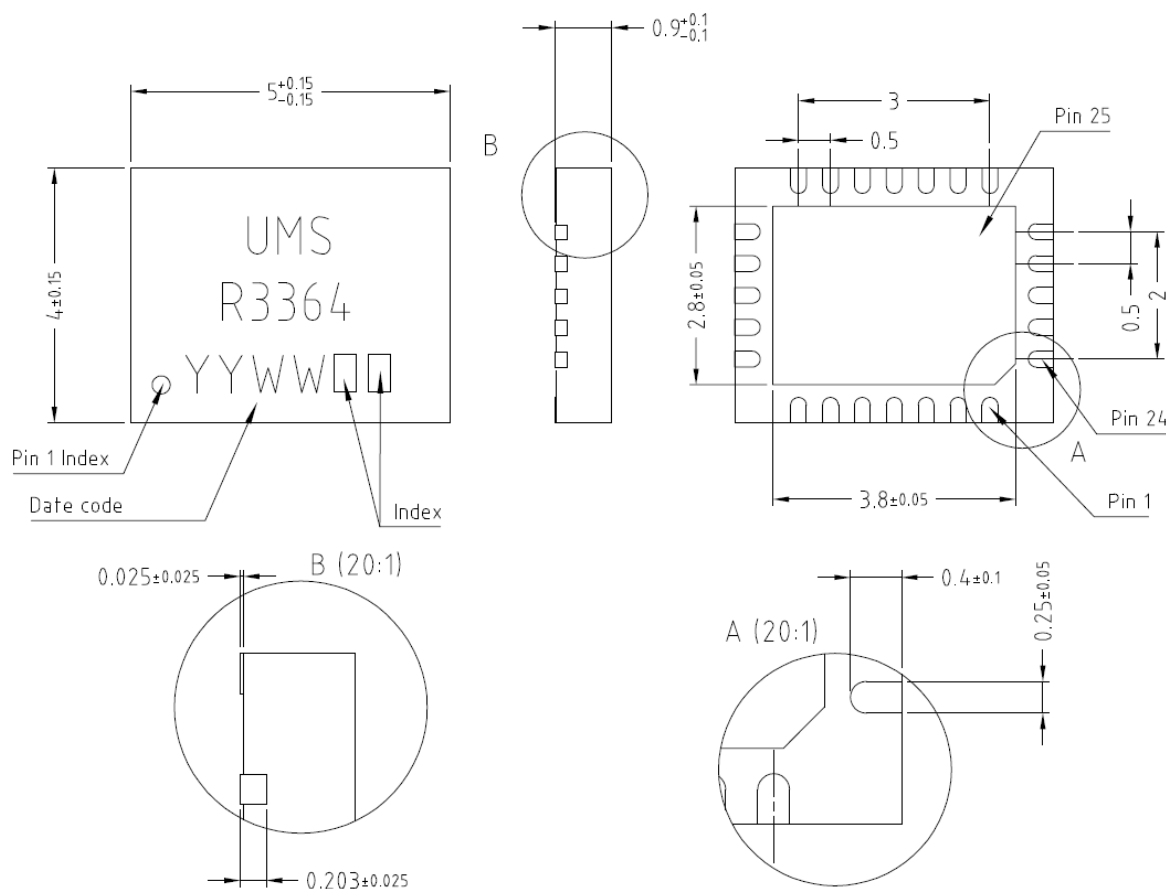
T = [-40, +25, +85] °C, V<sub>D</sub> = V<sub>DL</sub> = 4.0V, V<sub>GL</sub> = -0.5V, V<sub>GM</sub> = -0.7V, P<sub>LO</sub> = 0dBm

### Input IP3 in Supradyn Mode versus RF Frequency

$$F_{RF} = 2 \times F_{LO} + F_{IF}, F_{IF} = 3.5\text{GHz}$$



## Package outline <sup>(1)</sup>



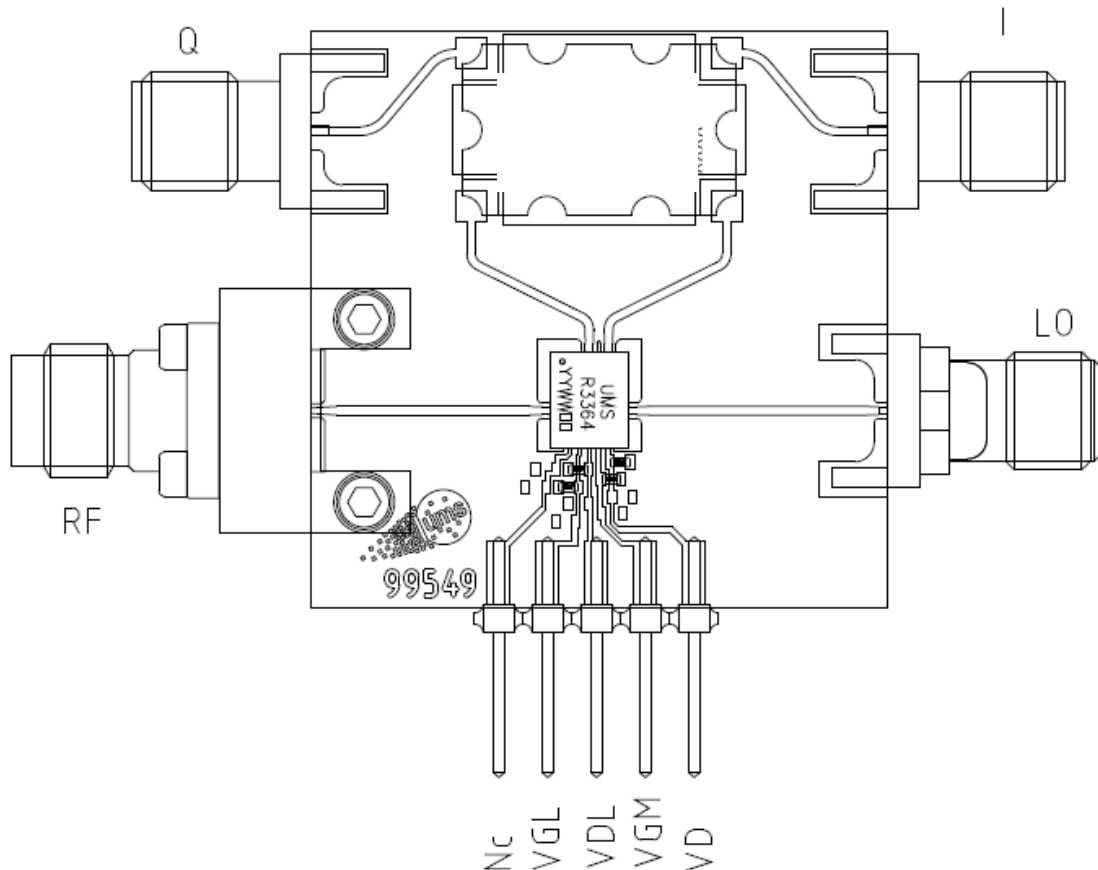
|                     |              |    |                    |     |                    |     |                    |
|---------------------|--------------|----|--------------------|-----|--------------------|-----|--------------------|
| Matt tin, Lead Free | (Green)      | 1- | Nc                 | 9-  | VGL                | 17- | Nc                 |
| Units :             | mm           | 2- | Nc                 | 10- | VDL                | 18- | Nc                 |
| From the standard : | JEDEC MO-220 | 3- | Nc                 | 11- | VGM                | 19- | Nc                 |
|                     | (VGGD)       | 4- | Gnd <sup>(2)</sup> | 12- | VD                 | 20- | IF_I out           |
| 25-                 | GND          | 5- | RF in              | 13- | Nc                 | 21- | Gnd <sup>(2)</sup> |
|                     |              | 6- | Gnd <sup>(2)</sup> | 14- | Gnd <sup>(2)</sup> | 22- | IF_Q out           |
|                     |              | 7- | Nc                 | 15- | LO in              | 23- | Nc                 |
|                     |              | 8- | Nc                 | 16- | Gnd <sup>(2)</sup> | 24- | Nc                 |

<sup>(1)</sup> The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

<sup>(2)</sup> It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

**Evaluation mother board**

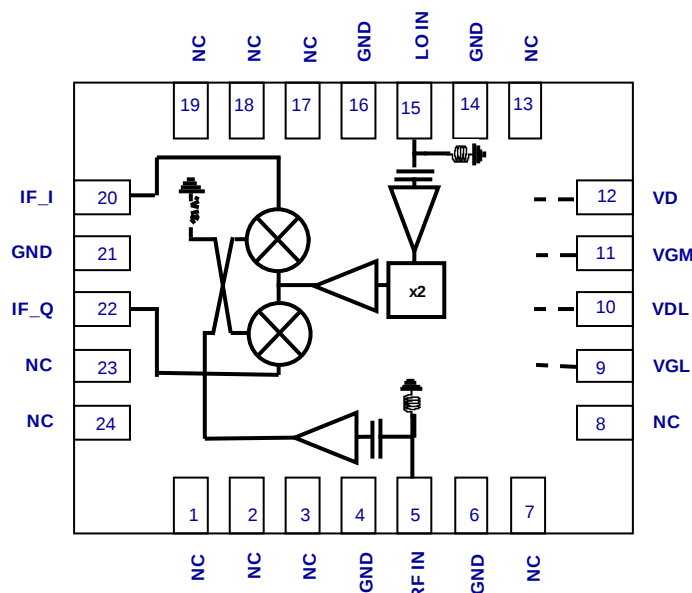
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF  $\pm 10\%$  are recommended for all DC accesses.
- See application note AN0017 for details.



Hybrid coupler 90° 2-4GHz

## Notes

Due to ESD protection circuits on RF and LO input, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses.



ESD protections are also implemented on gate accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

## Biasing Options

In order to improve the conversion gain or the input IP3, the biasing could be tuned.

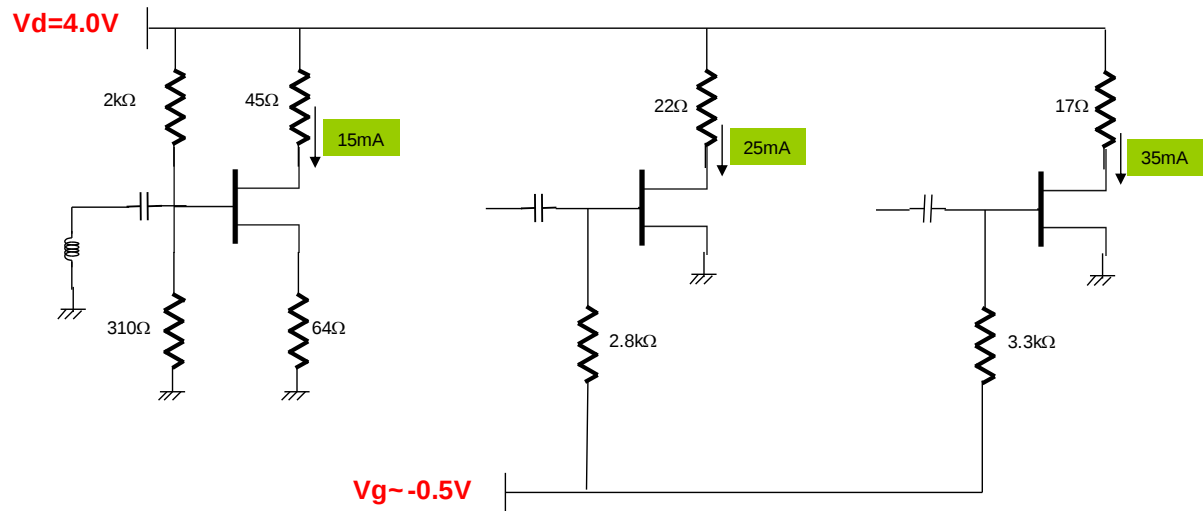
VGL voltage allows controlling IDL current.

Table below gives the typical value for main characteristics

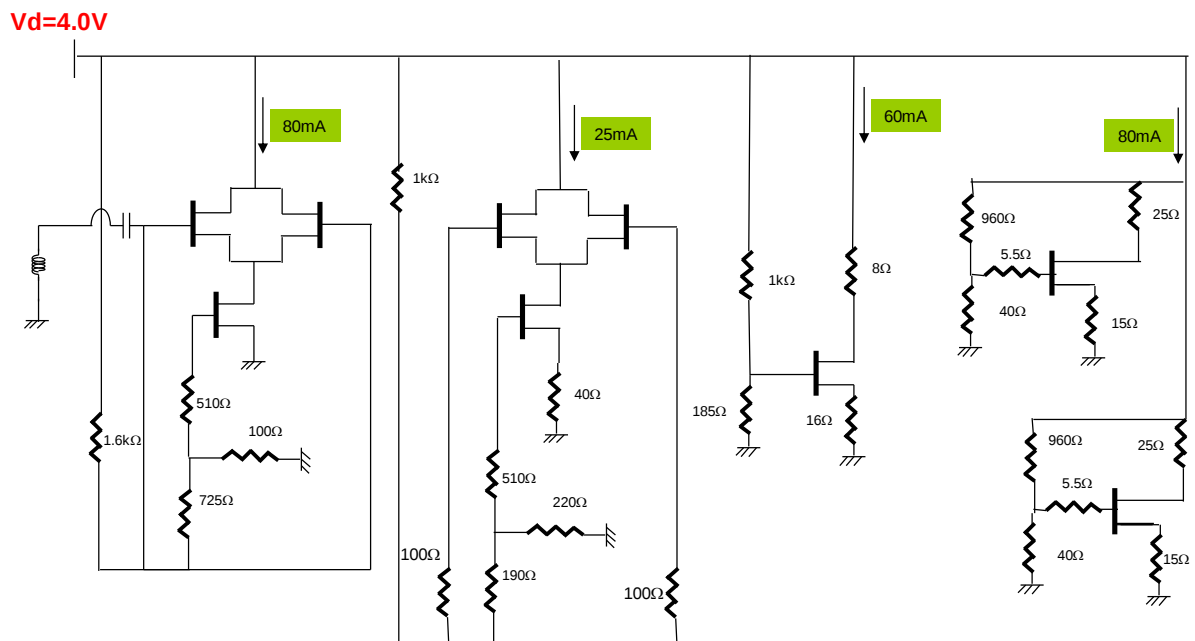
|                                 | VD=VDL= 4.0V<br>IDL= 75mA | VD=VDL= 4.5V<br>IDL= 110mA |
|---------------------------------|---------------------------|----------------------------|
| Conversion Gain (dB)            | 11                        | 12.5                       |
| Noise Figure (dB)               | 2.7                       | 2.6                        |
| Input IP3 (dBm)                 | +1                        | +3                         |
| VGL (V)                         | -0.5                      | -0.4                       |
| ID (mA)                         | 245                       | 250                        |
| ID +IDL (mA)                    | 320                       | 360                        |
| Total DC power consumption (mW) | 1280                      | 1620                       |

## DC Schematic

## LNA: 4V, 75mA



## LO Buffer: 4V, 245mA



## Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 4x5 RoHS compliant package:

CHR3364-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

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