

Entry level PMIC for applications requiring up to 8.5 A

General description

DA9062 is a power management integrated circuit (PMIC) optimised for supplying systems with single- and dual-core processors, I/O, DDR memory, and peripherals. It targets mobile device, medical equipment, entry level IVI system, and FPGA based applications.

DA9062 features four buck converters providing a total current of 8.5 A. High efficiency is achieved over a wide load range by using automatic Pulse Frequency Modulation (PFM) mode. All power switches are integrated, therefore, external Schottky diodes are not required. Furthermore, low-profile inductors can be used with DA9062. Two of the buck converters can be used in a dual-phase configuration, and one can be used as a DDR VTT supply. The four LDO regulators with programmable output voltage provide up to 300 mA.

Dynamic voltage control (DVC) allows dynamic control of DA9062 supply voltages according to the operating point of the system. It is controlled by writing directly to the registers using the I²C compatible 2-wire interface or the GPIOs.

DA9062 features a programmable power sequencer that handles start-up and shutdown sequences. Power mode transitions can be triggered with software control, GPIOs, or with the on-key. Several types of on-key presses can be detected to trigger different power mode transitions.

The real-time clock (RTC) with an external 32 kHz crystal oscillator provides time keeping and alarm functions. Additionally, the integrated watchdog timer monitors the system.

Five GPIOs are able to perform system functions, including: keypad supervision, application wakeup, and timing-controlled external regulators/power switches or other ICs.

DA9062 is also available as an automotive AEC-Q100 Grade 3 version.

Key features

- Input voltage 2.8 to 5.5 V
- Four buck converters with dynamic voltage control:
 - Buck1: 0.3 to 1.57 V, 2.5 A
 - Buck2: 0.3 to 1.57 V, 2.5 A (can be used in dual-phase configuration with Buck1)
 - Buck3: 0.8 to 3.34 V, 2 A
 - Buck4: 0.53 to 1.8 V, 1.5 A (can be used as DDR VTT supply)
 - 3 MHz switching frequency (enables low profile inductors)
- Four LDO regulators:
 - LDO1: 0.9 to 3.6 V, 100 mA
 - LDO2, LDO3, LDO4: 0.9 to 3.6 V, 300 mA
- Programmable power mode sequencer
- System supply and junction temperature monitoring
- Watchdog timer
- Five GPIOs
- Coin cell/super-capacitor charger
- Ultra-low power real-time clock with alarm
- 32 kHz oscillator with external crystal
- -40 to +85 °C temperature range
- 40-pin QFN 6x6 mm package, 0.5 mm pitch (exposed paddle)
- Automotive AEC-Q100 Grade 3 variant available

Applications

- Supply for single core application processors
- Power supply for entry-level FPGAs
- E-book readers and entry-level car infotainment

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Block diagram

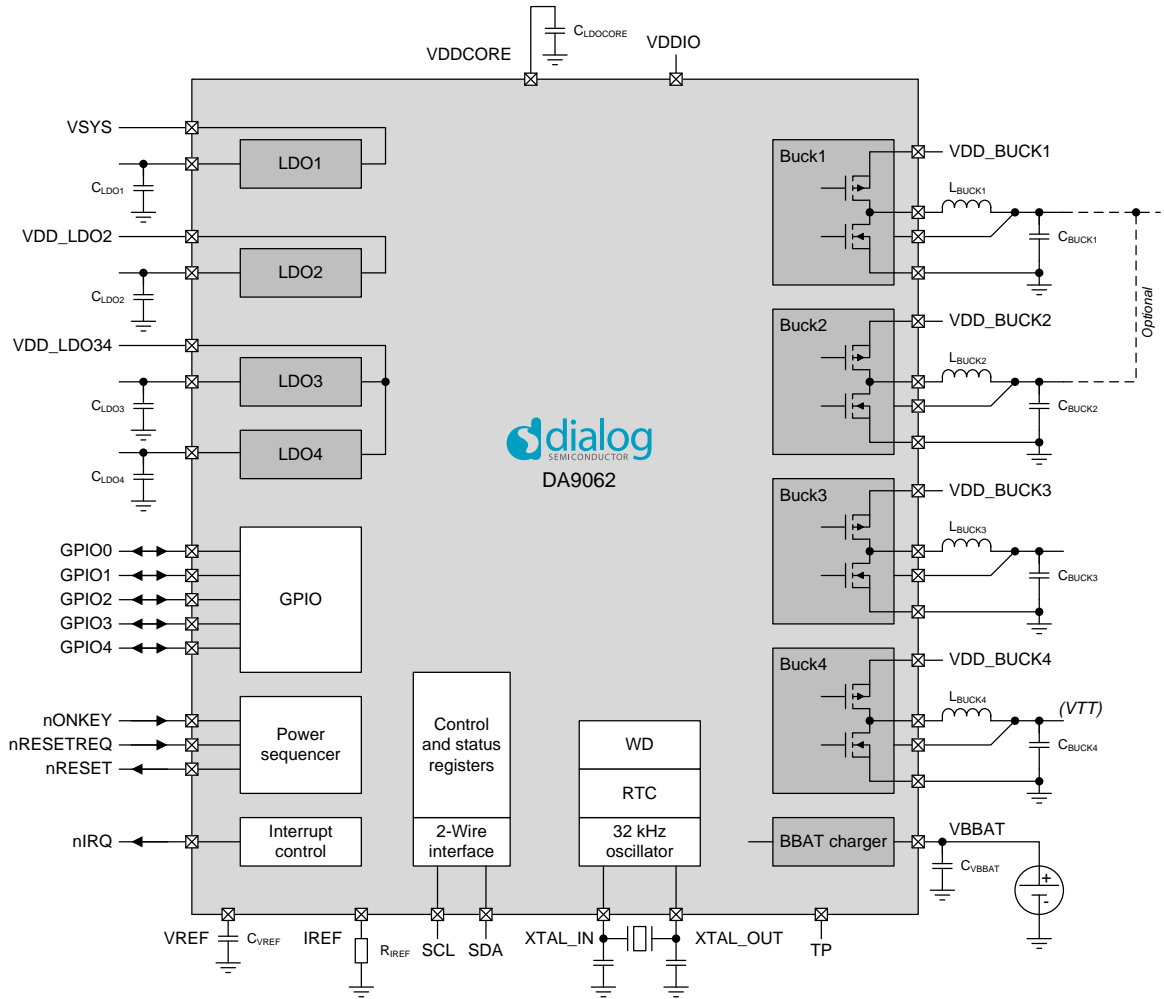


Figure 1: DA9062 block diagram

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1 Package information

1.1 Pin list

Table 1: DA9062 pin description

Pin	Name	Type Table 2	Description
Paddle	GND	GND	Power grounds of the bucks, digital ground
1	VLDO1	AO	LDO1 output voltage
2	VLDO2	AO	LDO2 output voltage
3	VDD_LDO2	PS	LDO2 supply
4	IREF	AO	Reference current
5	VREF	AIO	Reference voltage
6	XTAL_IN	AI	Crystal connection
7	VSS_ANA	GND	Analog ground
8	XTAL_OUT	AO	Crystal connection
9	VLDO3	AO	LDO3 output voltage
10	VDD_LDO34	PS	LDO3 and LDO4 supply
11	VLDO4	AO	LDO4 output voltage
12	VBBAT	AO	Backup battery connection
13	SDA	DIO	Data signal of the 2-wire interface
14	SCL	DI	Clock signal of the 2-wire interface
15	nONKEY	DI	Input for power-on key
16	nRESETREQ	DI	Reset request input
17	VLX_BUCK4	AO	Switching node of Buck4
18	VDD_BUCK4	PS	Buck4 supply
19	VDD_BUCK3	PS	Buck3 supply
20	VLX_BUCK3	AO	Switching node of Buck3
21	GPIO0	DIO	General purpose I/O, VDDQ reference, WDKICK
22	GPIO1	DIO	General purpose I/O, VTTR
23	VDDIO	PS	IO supply
24	VBUCK4	AI	Voltage feedback of Buck4
25	VBUCK3	AI	Voltage feedback of Buck3
26	VBUCK1	AI	Voltage feedback of Buck1
27	VBUCK2	AI	Voltage feedback of Buck2
28	GPIO2	DIO	General purpose I/O, PWR_EN
29	GPIO3	DIO	General purpose I/O
30	GPIO4	DIO	General purpose I/O, SYS_EN
31	VLX_BUCK1	AO	Switching node of Buck1
32	VDD_BUCK1	PS	Buck1 supply
33	VDD_BUCK2	PS	Buck2 supply

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Pin	Name	Type Table 2	Description
34	VLX_BUCK2_A	AO	Switching node of Buck2
35	VLX_BUCK2_B	AO	Switching node of Buck2
36	TP	DIO	Test pin
37	nIRQ	DO	Interrupt signal to host processor
38	nRESET	DO	Reset output
39	VDDCORE	AO	Internal supply
40	VSYS	PS	System supply, LDO1 supply

Table 2: Pin type definitions

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
PS	Power Supply	GND	Ground connection

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1.2 Package outline drawing

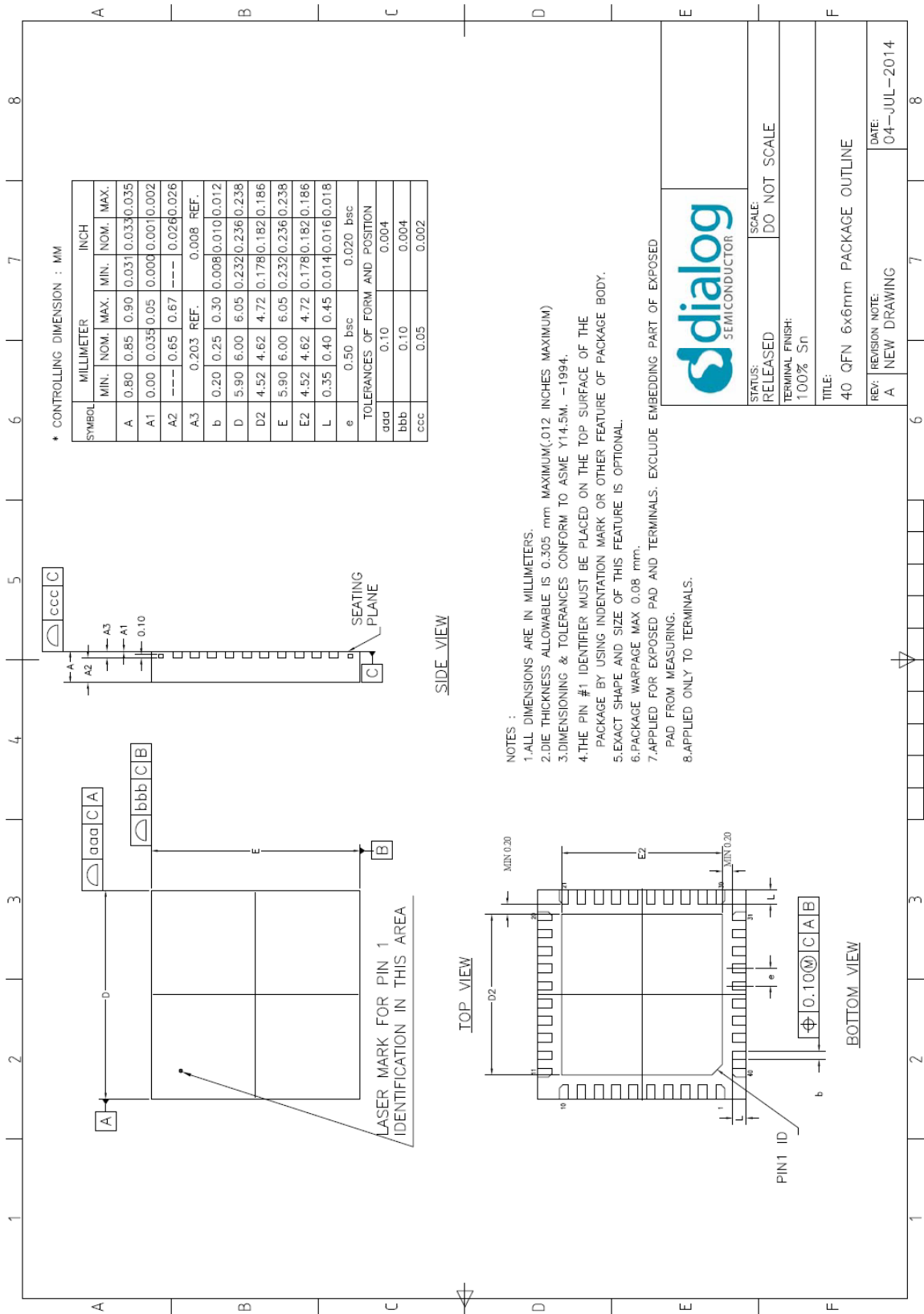


Figure 2: DA9062 package outline drawing

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2 Absolute maximum ratings

Table 3 lists the absolute maximum ratings of the device. Exceeding these ratings may cause permanent damage to the device. Device functionality is only guaranteed under the conditions listed in Sections 3 and 4. Operating the device in conditions exceeding those listed in Sections 3 and 4, but compliant with the absolute maximum ratings listed in Table 3, for extended periods of time may affect device reliability.

Table 3: Absolute maximum ratings

Parameter	Symbol	Note	Min	Typ	Max	Unit
Storage temperature			-65		+150	°C
Operating junction temperature	T_J		-40		+150 Note 1	°C
Supply voltage	V_{SYS}		-0.3		5.5	V
	All other pins		-0.3		$V_{SYS} + 0.3$ Note 2	V
ESD protection HBM			2000			V
ESD protection CDM		Corner pins	750			V
		All other pins	500			

Note 1 See Sections Note 1 and 7.10 for more detail.

Note 2 Voltage must not exceed 5.5 V.

3 Recommended operating conditions

Table 4: Recommended operating conditions

Parameter	Symbol	Note	Min	Typ	Max	Unit
Ambient operating temperature	T_A		-40		+85	°C
Supply voltage	V_{SYS}		0		5.5	V
Supply voltage IO	V_{DDIO}	IO supply voltage Note 1	1.2		3.6	V
Maximum power dissipation Note 2		Derating factor above $T_A = 70\text{ °C}$: 56 mW/°C		3000		mW

Note 1 V_{DDIO} must not exceed V_{SYS} .

Note 2 Obtained from package thermal simulation, board dimension 76 x 114 x 1.6 mm (JEDEC), 6-layer board, 35 μm thick copper top/bottom layers, 17 μm thick copper inside layers, natural convection (still air).

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4 Electrical characteristics

4.1 Digital I/O

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 5: Digital I/O electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input high voltage (GPIO-GPI4, nRESETREQ)	V_{IH}	VDDCORE mode	1.0		V_{SYS}	V
		VDDIO mode	$0.7 * V_{DDIO}$		V_{SYS}	
Input low voltage (GPIO-GPI4, nRESETREQ)	V_{IL}	VDDCORE mode	-0.3		0.4	V
		VDDIO mode	-0.3		$0.3 * V_{DDIO}$	
Input high voltage (nONKEY)	V_{IH}	RTC mode	1.0		V_{SYS}	V
		VDDCORE mode	1.0		V_{SYS}	
		VDDIO mode	$0.7 * V_{DDIO}$			
Input low voltage (nONKEY)	V_{IL}	RTC mode	-0.3		0.4	V
		VDDCORE mode	-0.3		0.4	
		VDDIO mode	-0.3		$0.3 * V_{DDIO}$	
Input high voltage (SCL, SDA)	V_{IH}	VDDCORE mode	1.0			V
		VDDIO mode	$0.7 * V_{DDIO}$			
Input low voltage (SCL, SDA)	V_{IL}	VDDCORE mode			0.4	V
		VDDIO mode			$0.3 * V_{DDIO}$	
Output high voltage (GPO0-GPO4, nRESET, nIRQ)	V_{OH}	$I_{LOAD} = 1$ mA Push-pull mode	$0.7 * V_{DDIO}$			V
Output low voltage (GPO0-GPO4, nRESET, nIRQ)	V_{OL}	$I_{LOAD} = 1$ mA			0.3	V
Output low voltage (SDA)	V_{OL}	$I_{LOAD} = 20$ mA			0.4	V
		$I_{LOAD} = 3$ mA			0.24	
Source current capability (GPO0-GPO4)	I_{OH}	$V_{OUT} = 0.7 * V_{DDIO}$ $V_{DDIO} \geq 1.8$ V		-1		mA
Sink current capability (GPO0-GPO4)	I_{OL}	$V_{OUT} = 0.3$ V		1		mA
Input capacitance (SCL, SDA)	C_{IN}				10	pF
Pull-down resistance (GPIO-GPI4)	R_{PD}		50	100	250	k Ω
Pull-up resistance (GPO0-GPO4)	R_{PU}	$V_{DDIO} = 1.5$ V	60	180	310	k Ω
		$V_{DDIO} = 1.8$ V	45	120	190	
		$V_{DDIO} = 3.3$ V	20	40	60	

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4.2 Watchdog

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 6: Watchdog electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Minimum watchdog time	t_{WDMIN}	External 32 kHz oscillator			110	ms
		Internal 25 kHz oscillator			200	ms
Maximum watchdog time	t_{WDMAX}	External 32 kHz oscillator	2			s
		Internal 25 kHz oscillator	2.5			s
Minimum assert time of WDKICK	$t_{WDKICKMIN}$			150		µs

4.3 2-wire interface

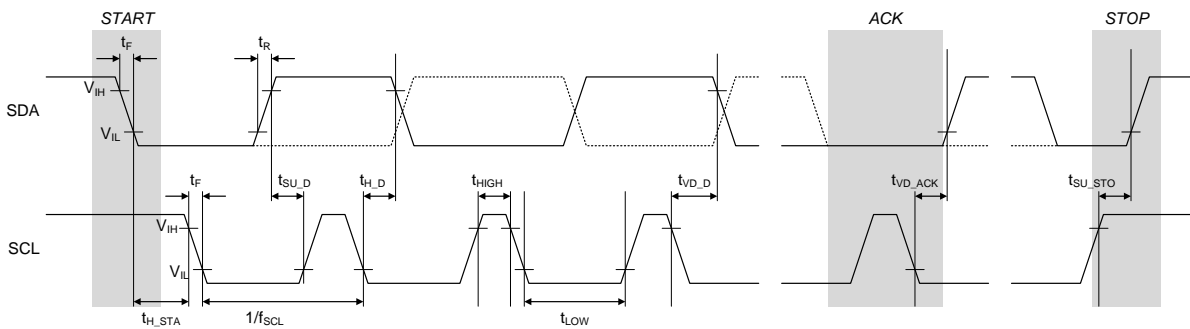


Figure 3: 2-wire interface timing

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

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Table 7: 2-wire interface electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Bus free time STOP to START	t_{BUF}		0.5			μs
Bus line capacitive load	C_B				150	pF
Standard/Fast/Fast+ Mode						
SCL clock frequency	f_{SCL}	Note 1	0		1000	kHz
Start condition set-up time	t_{SU_STA}		0.26			μs
Start condition hold time	t_{H_STA}		0.26			μs
SCL low time	t_{W_CL}		0.5			μs
SCL high time	t_{W_CH}		0.26			μs
2-WIRE SCL and SDA rise time	t_R	(input requirement)			1000	ns
2-WIRE SCL and SDA fall time	t_F	(input requirement)			300	ns
Data set-up time	t_{SU_D}		50			ns
Data hold-time	t_{H_D}		0			ns
Data valid time	t_{VD_D}				0.45	μs
Data valid time acknowledge	t_{VD_ACK}				0.45	μs
Stop condition set-up time	t_{SU_STO}		0.26			μs
High Speed Mode						
SCL clock frequency	f_{SCL}	Requires $V_{DDIO} \geq 1.8 V$ Note 1	0		3400	kHz
Start condition set-up time	t_{SU_STA}		160			ns
Start condition hold time	t_{H_STA}		160			ns
SCL low time	t_{W_CL}		160			ns
SCL high time	t_{W_CH}		60			ns
2-wire SCL and SDA rise time	t_R	(input requirement)			160	ns
2-wire SCL and SDA fall time	t_F	(input requirement)			160	ns
Data set-up time	t_{SU_D}		10			ns
Data hold-time	t_{H_D}		0			ns
Stop condition set-up time	t_{SU_STO}		160			ns

Note 1 Minimum clock frequency is 10 kHz if 2WIRE_TO is enabled.

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4.4 LDOs

4.4.1 LDO1

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C.

Table 8: LDO1 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	$V_{DD} = V_{SYS}$	2.8		5.5	V
Output voltage	V_{LDO}	Programmable in 50 mV steps	0.9		3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$ including static line/load regulation	-3%		+3%	
Stabilisation capacitor	C_{OUT}	Including voltage and temperature coefficient	-55%	1.0	+35%	μF
Output capacitor ESR	$R_{C_{OUT_ESR}}$	$f > 1$ MHz including wiring parasitics	0		300	m Ω
Output current	I_{OUT}	$V_{DD} \geq 1.8$ V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ $I_{OUT} = I_{MAX}/3$ for $V_{DD} = 1.5$ V		100	150	mV
Static line regulation	V_{S_LINE}	$V_{DD} = 3.0$ to 5.5 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	V_{S_LOAD}	$I_{OUT} = 1$ mA to I_{MAX}		5	20	mV
Line transient response	V_{TR_LINE}	$V_{DD} = 3.0$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10$ μs		5	20	mV
Load transient response	V_{TR_LOAD}	$V_{DD} = 3.6$ V $I_{OUT} = 1$ mA to I_{MAX} $t_r = t_f = 1$ μs		30	50	mV
Power supply rejection ratio	PSRR	$V_{DD} = 3.6$ V $V_{DD} - V_{LDO} \geq 0.6$ V $I_{OUT} = I_{MAX}/2$ $f = f_{VDDLDO}$ $f = 10$ Hz to 10 kHz	40	60		dB
Output noise	N	$V_{DD} = 3.6$ V, $V_{LDO} = 2.8$ V $I_{OUT} = 5$ mA to I_{MAX} $f = 10$ Hz to 100 kHz		70		μV rms
Quiescent current in ON mode	I_{Q_ON}			9 + 0.9% I_{OUT}		μA
Quiescent current in SLEEP mode	I_{Q_SLEEP}			1.5 + 1.6% I_{OUT}		μA
Quiescent current in OFF mode	I_{Q_OFF}	$T_A = 25$ °C $V_{LDO} < 0.5$ V			1	μA
Turn-on time	t_{ON}	10 to 90 %			350	μs
		SLEEP mode			450	
Turn-off time	t_{OFF}	90 to 10% Pull-down enabled			1	ms

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Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Pull-down resistance in OFF mode	R_{OFF}	$V_{LDO} = 0.5\text{ V}$ Can be disabled via LDO1_PD_DIS		100		Ω

4.4.2 LDO2, LDO3, LDO4

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85\text{ }^\circ\text{C}$.

Table 9: LDO2, LDO3, LDO4 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8		5.5	V
		Power stage supplied from buck	1.5			
Output voltage	V_{LDO}	Programmable in 50 mV steps	0.9		3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$ including static line/load regulation	-3%		+3%	
Stabilisation capacitor	C_{OUT}	Including voltage and temperature coefficient	-55%	2.2	+35%	μF
Output capacitor ESR	R_{COUT_ESR}	$f > 1\text{ MHz}$ including wiring parasitics	0		300	$\text{m}\Omega$
Output current	I_{OUT}	$V_{DD} \geq 1.8\text{ V}$	300			mA
Short circuit current	I_{SHORT}			600		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ $I_{OUT} = I_{MAX}/3$ for $V_{DD} = 1.5\text{ V}$		100	150	mV
Static line regulation	V_{S_LINE}	$V_{DD} = 3.0$ to 5.5 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	V_{S_LOAD}	$I_{OUT} = 1\text{ mA}$ to I_{MAX}		5	20	mV
Line transient response	V_{TR_LINE}	$V_{DD} = 3.0$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_R = t_F = 10\text{ }\mu\text{s}$		5	20	mV
Load transient response	V_{TR_LOAD}	$V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_R = t_F = 1\text{ }\mu\text{s}$		30	50	mV
Power supply rejection ratio	PSRR	$V_{DD} = 3.6\text{ V}$ $V_{DD} - V_{LDO} \geq 0.6\text{ V}$ $I_{OUT} = I_{MAX}/2$ $f = f_{VDDLDO}$ $f = 10\text{ Hz}$ to 1 kHz $f = 1$ to 10 kHz $f = 10$ to 100 kHz	70 60 40	80 70 50		dB
Output noise	N	$V_{DD} = 3.6\text{ V}$, $V_{LDO} = 2.8\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} $f = 10\text{ Hz}$ to 100 kHz		50		$\mu\text{V rms}$
Quiescent current in ON mode	I_{Q_ON}			9 + 0.34% I_{OUT}		μA
Quiescent current in SLEEP mode	I_{Q_SLEEP}			2 + 0.7% I_{OUT}		μA
Quiescent current in	I_{Q_OFF}	$T_A = 25\text{ }^\circ\text{C}$			1	μA

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Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
OFF mode		$V_{LDO} < 0.5 \text{ V}$				
Turn-on time	T_{ON}	10 to 90 %			200	μs
		SLEEP mode			300	
Turn-off time	T_{OFF}	90 to 10 % Pull-down enabled			1	ms
Pull-down resistance in OFF mode	R_{OFF}	$V_{LDO} = 0.5 \text{ V}$ Can be disabled via $LDO\langle x \rangle_PD_DIS$		100		Ω

4.4.3 LDOCORE

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85 \text{ }^\circ\text{C}$, $V_{SYS} = 2.8$ to 5.5 V .

Table 10: LDOCORE electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Output voltage	V_{DDCORE}	Note 1	2.45	2.5	2.55	V
		RESET mode		2.2		V
Stabilisation capacitor	C_{OUT}	Including voltage and temperature coefficient	-55%	2.2	+35%	μF
Output capacitor ESR	R_{COUT_ESR}	$f > 1 \text{ MHz}$ including wiring parasitics	0		300	$\text{m}\Omega$
Dropout voltage	$V_{DROPOUT}$	Note 2		50	100	mV

Note 1 Setting $V_{DD_FAULT_LOWER} \geq 2.65 \text{ V}$ avoids LDOCORE dropout. See Section 4.9 for more detail.

Note 2 The LDOCORE supply, V_{SYS} , must be maintained above $V_{DDCORE} + V_{DROPOUT}$

NOTE

LDOCORE is only used to supply internal circuits.

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4.5 Buck converters

4.5.1 Buck1, Buck2

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C.

Table 11: Buck1, Buck2 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8		5.5	V
Output capacitor	C_{OUT}	Half-current mode including voltage and temperature coefficient	-50%	2 * 22	+30%	μF
		Full-current mode including voltage and temperature coefficient	-50%	2 * 47	+30%	
Output capacitor ESR	$R_{C_{OUT_ESR}}$	$C_{OUT} = 2 * 22 \mu\text{F}$ $f > 100 \text{ kHz}$ including wiring parasitics		15	50	$\text{m}\Omega$
		$C_{OUT} = 2 * 47 \mu\text{F}$ $f > 100 \text{ kHz}$ including wiring parasitics		7.5	25	
Inductor value	L_{BUCK}	Half-current mode including current and temperature dependence	0.6	1.0	1.3	μH
		Full-current mode including current and temperature dependence	0.5	1.0	1.3	
Inductor resistance	R_{L_DCR}	Half-current mode		80	120	$\text{m}\Omega$
		Full-current mode		60	100	
Output voltage	V_{BUCK}	Programmable in 10 mV steps	0.7		1.57	V
Output voltage accuracy	V_{BUCK_ACC}	$V_{DD} = 4.2 \text{ V}$, $V_{BUCK} = 1.03 \text{ V}$ excluding static line/load regulation and voltage ripple	-1%		+1%	
		Including static line/load regulation and voltage ripple Note 1	-3%		+3%	
Transient load regulation	V_{TR_LOAD}	$V_{DD} = 3.6 \text{ V}$, $V_{BUCK} = 1.15 \text{ V}$ $I_{OUT} = 200$ to 1000 mA $di/dt = 3 \text{ A}/\mu\text{s}$ $L = 1 \mu\text{H}$		30	45	mV
Transient line regulation	V_{TR_LINE}	$V_{DD} = 3.0$ to 3.6 V $I_{OUT} = 500 \text{ mA}$ $t_R = t_F = 10 \mu\text{s}$		0.2	3	mV
Output current	I_{OUT}	Half-current mode $L > 0.6 \mu\text{H}$			900	mA
		Half-current mode $L > 0.9 \mu\text{H}$			1250	
		Full-current mode $L > 0.9 \mu\text{H}$			2500	

Entry level PMIC for applications requiring up to 8.5 A

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Current limit	I_{LIM}	Controlled in BUCK<x>_ILIM in 200 mA steps. In half-current mode each step is 100 mA.	500		2000	mA
Current limit accuracy	I_{LIM_ACC}		-20%		20%	
Quiescent current in OFF mode	I_{Q_OFF}				1	μ A
Quiescent current in PWM mode	I_{Q_ON}	Half-current mode $I_{OUT} = 0$ mA		9		mA
		Full-current mode $I_{OUT} = 0$ mA		11		
Switching frequency	f		2.85	3	3.15	MHz
Switching duty cycle	DC		14%		83%	
Turn-on time	t_{ON}	$V_{BUCK} = 1.15$ V BUCK_SLOWSTART = disabled SLEW_RATE = 10 mV/1 μ s BUCK<x>_ILIM = 1500 mA		0.37	1.2	ms
Output pull-down resistance	R_{PD}	$V_{BUCK} = 0.5$ V disabled via BUCK<x>_PD_DIS		100	200	Ω
PMOS ON resistance	R_{PMOS}	Half-current mode, including pin and routing, $V_{SYS} = 3.6$ V		160		m Ω
		Full-current mode including pin and routing, $V_{SYS} = 3.6$ V		80		
NMOS ON resistance	R_{NMOS}	Half-current mode, including pin and routing, $V_{SYS} = 3.6$ V		60		m Ω
		Full-current mode, including pin and routing, $V_{SYS} = 3.6$ V		30		
PFM mode						
Output voltage	V_{BUCK_PFM}	Programmable in 10 mV steps. Output voltages below 0.7 V force the buck to stay in PFM mode.	0.3		1.57	V
Mode transition current threshold (PFM to PWM) in AUTO mode	I_{AUTO_THR}	$V_{IN} = 3.6$ V, $V_{BUCK} = 1.15$ V $R_{TRACK} \sim 45$ m Ω including bondwire, PCB and inductor ESR		400		mA
Output current	I_{OUT_PFM}	Forced PFM mode			300	mA
Current limit	I_{LIM_PFM}			1000		mA
Quiescent current	I_{Q_PFM}	Forced PFM mode, $I_{OUT} = 0$ mA		27	32	μ A
		AUTO mode, $I_{OUT} = 0$ mA		35	42	
Mode transition time	t_{AUTO}	AUTO mode		6		μ s

Note 1 Minimum tolerance 35 mV.

Entry level PMIC for applications requiring up to 8.5 A

4.5.2 Buck3

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C.

Table 12: Buck3 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	$I_{OUT} \leq 1.5$ A	2.8		5.5	V
		$I_{OUT} > 1.5$ A	3.3		5.5	
Output capacitor	C_{OUT}	$I_{OUT} \leq 1.5$ A including voltage and temperature coefficient	-50%	2 * 22	+30%	μ F
		$I_{OUT} > 1.5$ A including voltage and temperature coefficient	-50%	2 * 47	+30%	
Output capacitor ESR	$R_{C_{OUT_ESR}}$	$C_{OUT} = 2 * 22$ μ F $f > 100$ kHz including wiring parasitics		15	50	m Ω
		$C_{OUT} = 2 * 47$ μ F $f > 100$ kHz including wiring parasitics		7.5	25	
Inductor value	L_{BUCK}	Including current and temperature dependence	0.6	1.0	1.3	μ H
Inductor resistance	R_{L_DCR}			80	120	m Ω
Output voltage	V_{BUCK}	Programmable in 20 mV steps	0.8		3.34	V
Output voltage accuracy	V_{BUCK_ACC}	Including static line and load regulation and voltage ripple Note 1	-3%		+3%	
Transient load regulation	V_{TR_LOAD}	$V_{DD} = 3.6$ V, $V_{BUCK} = 1.8$ V $I_{OUT} = 200$ to 1000 mA $di/dt = 3$ A/ μ s $L = 1$ μ H		30	45	mV
		$V_{DD} = 3.6$ V, $V_{BUCK} = 1.8$ V $I_{OUT} = 200$ to 2000 mA $di/dt = 3$ A/ μ s $L = 1$ μ H		60	90	
		$V_{DD} = 5.0$ V, $V_{BUCK} = 3.34$ V $I_{OUT} = 200$ to 2000 mA $di/dt = 3$ A/ μ s $L = 1$ μ H		60	90	
Transient line regulation	V_{TR_LINE}	$V_{DD} = 3.0$ to 3.6 V $I_{OUT} = 500$ mA $tr = tf = 10$ μ s		0.2	3	mV
Output current	I_{OUT}	$V_{DD} - V_{BUCK} \geq 1.25$ V $L > 0.9$ μ H			2000	mA
		$V_{DD} - V_{BUCK} \geq 1.00$ V $L > 0.9$ μ H			1250	
		$V_{DD} - V_{BUCK} \geq 0.75$ V $L > 0.6$ μ H			900	
Current limit	I_{LIM}	Controlled in BUCK3_ILIM in 100 mA steps	1500		3000	mA
Current limit accuracy	I_{LIM_ACC}		-20%		20%	

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Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Quiescent current in OFF mode	I_{Q_OFF}				1	μA
Quiescent current in PWM mode	I_{Q_ON}	$I_{OUT} = 0 \text{ mA}$		9		mA
Switching frequency	F		2.85	3	3.15	MHz
Switching duty cycle	DC		15%		100%	
Turn-on time	t_{ON}	$V_{BUCK} = 1.8 \text{ V}$ BUCK_SLOWSTART = disabled SLEW_RATE = 20 mV/2 μs BUCK3_ILIM = 2500 mA		0.44	1.5	ms
Output pull-down resistance	R_{PD}	$V_{BUCK} = 0.5 \text{ V}$ disabled via BUCK3_PD_DIS		100	200	Ω
PMOS ON resistance	R_{PMOS}	Including pin and routing $V_{SYS} = 3.6 \text{ V}$		150		m Ω
NMOS ON resistance	R_{NMOS}	Including pin and routing $V_{SYS} = 3.6 \text{ V}$		60		m Ω
PFM mode						
Output voltage	V_{BUCK_PFM}	Programmable in 20 mV steps	0.8		3.34	V
Mode transition current threshold (PFM to PWM) in AUTO mode	I_{AUTO_THR}	$V_{IN} = 3.6 \text{ V}$, $V_{BUCK} = 1.8 \text{ V}$ $R_{TRACK} \sim 45 \text{ m}\Omega$ including bondwire, PCB and inductor ESR		400		mA
Current limit	I_{LIM_PFM}			1000		mA
Output current	I_{OUT_PFM}	Forced PFM mode			300	mA
Quiescent current	I_{Q_PFM}	Forced PFM mode, $I_{OUT} = 0 \text{ mA}$		22	25	μA
		AUTO mode, $I_{OUT} = 0 \text{ mA}$		30	35	
Mode transition time	t_{AUTO}	AUTO mode		6		μs

Note 1 Minimum tolerance 35 mV.

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4.5.3 Buck4

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C.

Table 13: Buck4 electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8		5.5	V
Output capacitor	C_{OUT}	Including voltage and temperature coefficient	-50%	2 * 22	+30%	μ F
Output capacitor ESR	$R_{C_{OUT_ESR}}$	$f > 100$ kHz including wiring parasitics		15	50	m Ω
Inductor value	L_{BUCK}	Including current and temperature dependence	0.6	1.0	1.3	μ H
Inductor resistance	R_{L_DCR}			80	120	m Ω
Output voltage	V_{BUCK}	Programmable in 10 mV steps	0.7		1.8	V
Output voltage accuracy	V_{BUCK_ACC}	Including static line/load regulation and voltage ripple Note 1	-3%		+3%	
Transient load regulation	V_{TR_LOAD}	$V_{DD} = 3.6$ V, $V_{BUCK} = 1.35$ V $I_{OUT} = 200$ to 1000 mA $di/dt = 3$ A/ μ s $L = 1$ μ H		25	40	mV
		$V_{DD} = 3.6$ V, $V_{BUCK} = 1.35$ V $I_{OUT} = 200$ to 1500 mA $di/dt = 3$ A/ μ s $L = 1$ μ H		40	60	
Transient line regulation	V_{TR_LINE}	$V_{DD} = 3.0$ to 3.6 V $I_{OUT} = 500$ mA $t_R = t_F = 10$ μ s		0.2	3	mV
Output current	I_{OUT}	$V_{DD} - V_{BUCK} \geq 1.25$ V $L > 0.9$ μ H			1500	mA
		$V_{DD} - V_{BUCK} \geq 1.00$ V $L > 0.9$ μ H			1250	
		$V_{DD} - V_{BUCK} \geq 1.00$ V $L > 0.6$ μ H			900	
Current limit	I_{LIM}	Controlled in BUCK4_ILIM in 100 mA steps	500		2000	mA
Current limit accuracy	I_{LIM_ACC}		-20%		+20%	
Quiescent current in OFF mode	I_{Q_OFF}				1	μ A
Quiescent current in PWM mode	I_{Q_ON}	$I_{OUT} = 0$ mA		9		mA
Switching frequency	f		2.85	3	3.15	MHz
Switching duty cycle	DC		14%		83%	
Turn-on time	t_{ON}	$V_{BUCK} = 1.35$ V BUCK_SLOWSTART = disabled SLEW_RATE = 10 mV/1 μ s BUCK4_ILIM = 1500 mA		0.39	1.2	ms
Output pull-down resistance	R_{PD}	$V_{BUCK} = 0.5$ V disabled via BUCK4_PD_DIS		100	200	Ω

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Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
PMOS ON resistance	R_{PMOS}	Including pin and routing $V_{SYS} = 3.6\text{ V}$		150		m Ω
NMOS ON resistance	R_{NMOS}	Including pin and routing $V_{SYS} = 3.6\text{ V}$		60		m Ω
PFM mode						
Output voltage	V_{BUCK_PFM}	Programmable in 10 mV steps. Output voltages below 0.7 V force the buck to stay in PFM mode.	0.53		1.8	V
Mode transition current threshold (PFM to PWM) in AUTO mode	I_{AUTO_THR}	$V_{IN} = 3.6\text{ V}$, $V_{BUCK} = 1.35\text{ V}$ $R_{TRACK} \sim 45\text{ m}\Omega$ including bondwire, PCB and inductor ESR		400		mA
Output current	I_{OUT_PFM}				300	mA
Current limit	I_{LIM_PFM}			1000		mA
Quiescent current	I_{Q_PFM}	Forced PFM mode, $I_{OUT} = 0\text{ mA}$		22	25	μA
		AUTO mode, $I_{OUT} = 0\text{ mA}$		30	35	
Mode transition time	t_{AUTO}	AUTO mode		6		μs
VTT mode						
Input voltage	V_{DD}		2.8		5.5	V
Output capacitor	C_{OUT}	Including voltage and temperature coefficient	-50%	2 * 47	+30%	μF
Output capacitor ESR	R_{COUT_ESR}	$f > 100\text{ kHz}$ including wiring parasitics		7.5	25	m Ω
Inductor value	L_{BUCK}			0.25		μH
Inductor resistance	R_{L_DCR}			80	120	m Ω
Output voltage	V_{BUCK}	$V_{BUCK} = V_{DDQ}/2$	0.675		1.3	V
Output voltage accuracy	V_{BUCK_ACC}	Relative to VTTR including static line/load regulation and voltage ripple.	-3%		+4%	
Output current	I_{OUT}	$V_{BUCK} = 0.675\text{ V}$		± 450		mA
		$V_{BUCK} = 0.700\text{ V}$		± 550		
		$V_{BUCK} = 0.750\text{ V}$		± 700		
Transient load regulation	V_{TR_LOAD}	$V_{DD} = 3.6\text{ V}$, $V_{BUCK} = 0.675\text{ V}$ $I_{OUT} = +10\text{ mA}$ to $+1.0\text{ A}$ $I_{OUT} = -450$ to -10 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 0.25\text{ }\mu\text{H}$		25	40	mV
		$V_{DD} = 3.6\text{ V}$, $V_{BUCK} = 0.675\text{ V}$ $I_{OUT} = +1\text{ A}$ to $+10\text{ mA}$ $I_{OUT} = -10$ to -450 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 0.25\text{ }\mu\text{H}$		35	50	
		$V_{DD} = 3.6\text{ V}$, $V_{BUCK} = 0.75\text{ V}$ $I_{OUT} = +10\text{ mA}$ to $+1.0\text{ A}$ $I_{OUT} = -700$ to -10 mA $di/dt = 3\text{ A}/\mu\text{s}$ $L = 0.25\text{ }\mu\text{H}$		25	40	

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Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
		$V_{DD} = 3.6\text{ V}$, $V_{BUCK} = 0.75\text{ V}$ $I_{OUT} = +1\text{ A to }+10\text{ mA}$ $I_{OUT} = -10\text{ to }-700\text{ mA}$ $dl/dt = 3\text{ A}/\mu\text{s}$ $L = 0.25\text{ }\mu\text{H}$		35	50	
Turn-on time	t_{ON}	$V_{BUCK} = 0.75\text{ V}$ BUCK_SLOWSTART = disabled SLEW_RATE = $10\text{ mV}/1\text{ }\mu\text{s}$ BUCK4_ILIM = 1500 mA		0.33	1.2	ms
VTTR buffer						
Feedback voltage	V_{DDQ}		1.35		2.6	V
VTTR output voltage	V_{TTR}	$V_{TTR} = V_{DDQ}/2$	0.675		1.3	V
VTTR voltage accuracy	V_{TTR_ACC}	Relative to V_{DDQ} input voltage	-49%		+51%	
VTTR output capacitor	C_{VTTR}	Including voltage and temperature coefficient	-50%	0.1	+30%	μF
VTTR output current	I_{VTTR}	Sink / source	-10		+10	mA

Note 1 Minimum tolerance 35 mV.

4.6 Backup battery charger

Unless otherwise noted, the following is valid for $T_A = -40\text{ to }+85\text{ }^\circ\text{C}$, $V_{SYS} = 2.8\text{ to }5.5\text{ V}$.

Table 14: Backup battery charger electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Backup battery charging current	I_{SET_BCHG}	$V_{SYS} = 3.6\text{ V}$ $V_{BBAT} = 2.5\text{ V}$	100	Note 1	6000	μA
Charger termination voltage	V_{SET_BCHG}	$V_{SYS} = 3.6\text{ V}$	1.1	Note 2	3.1	V
Backup battery short circuit current	I_{SHORT}	$V_{BBAT} = 0\text{ V}$		6.5		mA
Stabilisation capacitor	C_{OUT}		-55%	470	+35%	nF
Output capacitor ESR	R_{COUT_ESR}	$f > 1\text{ MHz}$			100	$\text{m}\Omega$
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = 5\text{ mA}$		150	200	mV

Note 1 Can be set in 100 μA steps from 100 to 1000 μA and 1 mA steps from 1 to 6 mA via BCHG_ISET in register BBAT_CONT

Note 2 Can be set in 100/200 mV steps via BCHG_VSET in register BBAT_CONT

Entry level PMIC for applications requiring up to 8.5 A

4.7 32 kHz crystal oscillator

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 15: 32 kHz crystal oscillator electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Supply voltage	V_{DDRTC}	Derived from V_{BBAT} or V_{DDCORE}	1.5		2.75	V
Oscillator frequency	f_{OSC}			32.768		kHz
Clock jitter		Cycle to cycle 1000 cycles		20	35	ns
Crystal ESR	R_{XTAL}			50	100	k Ω
Crystal CAP	C_{XTAL}			2		pF
Start-up time	t_{START}	$V_{DDRTC} = 1.5$ to 2.75 V		0.5	2	s
Bypass mode						
Input frequency	f_{IN}		-5%	32	+5%	kHz
Input duty cycle	DC		40%		60%	
XTAL_IN Input high voltage	V_{IH}	RTC_EN = 0	1.8		V_{SYS}	V
		RTC_EN = 1 $V_{BBAT} < V_{SYS}$	1.1			
		RTC_EN = 1 $V_{BBAT} > V_{SYS}$	$0.7 * V_{BBAT}$		V_{BBAT}	
XTAL_OUT Input low voltage	V_{IL}	RTC_EN = 0	-0.3		0.6	V
		RTC_EN = 1 $V_{BBAT} < V_{SYS}$			0.4	
		RTC_EN = 1 $V_{BBAT} > V_{SYS}$			$0.2 * V_{BBAT}$	
Input slew rate	SR	2 pF input capacitance	0.1			V/ns

4.8 Internal oscillator

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 16: Internal oscillator electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Oscillator frequency	f_{OSC}		5.7	6	6.3	MHz

Entry level PMIC for applications requiring up to 8.5 A

4.9 System supply voltage supervision

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 17: System supply voltage supervision electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Under-voltage lockout lower threshold	V_{POR_LOWER}			2.0		V
Under-voltage lockout upper threshold	V_{POR_UPPER}			2.3		V
V_{SYS} undervoltage lower threshold	$V_{DD_FAULT_LOWER}$ Note 1		2.5	2.8	3.25	V
V_{SYS} undervoltage lower threshold accuracy	V_{SYS_LOWER}		-2%		+2%	
V_{SYS} hysteresis	$V_{DD_FAULT_HYS}$ Note 2		100	200	450	mV
V_{SYS} upper threshold	$V_{DD_FAULT_UPPER}$		-2%	$V_{DD_FAULT_LOWER} + V_{DD_FAULT_HYS}$	+2%	
Reference voltage	V_{REF}		-1%	1.2	+1%	V
VREF decoupling capacitor	C_{VREF}			2.2		μF
Reference current resistor	R_{IREF}		-1%	200	+1%	kΩ

Note 1 Can be set in 50 mV steps via $V_{DD_FAULT_ADJ}$ in register $CONFIG_B$, setting $V_{DD_FAULT_LOWER} \geq 2.65$ V avoids LDOCORE dropout, see Section 4.4.3 for more detail

Note 2 Can be set in 50 mV steps via $V_{DD_HYST_ADJ}$ in register $CONFIG_B$

4.10 Junction temperature supervision

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 18: Junction temperature supervision electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
POR temperature threshold	T_{POR}	Note 1	135	150	165	°C
Critical temperature threshold	T_{CRIT}	Note 1	125	140	155	°C
Warning temperature threshold	T_{WARN}	Note 1	110	125	140	°C

Note 1 Thermal thresholds are non-overlapping.

Entry level PMIC for applications requiring up to 8.5 A

4.11 Current consumption

Unless otherwise noted, the following is valid for $T_A = -40$ to $+85$ °C, $V_{SYS} = 2.8$ to 5.5 V.

Table 19: Current consumption electrical characteristics

Operating mode	Symbol	Test conditions	VBBAT (Typ)	VSYS (Typ)	Unit
RTC mode	I _{DDRTC}	V _{SYS} > 2.2 V supplies off (except LDOCORE) RTC enabled V _{BBAT} > V _{SYS}	1.5	1.0	µA
		V _{SYS} > 2.2 V supplies off (except LDOCORE) RTC enabled V _{BBAT} < V _{SYS}	0.5	7	µA
POWERDOWN mode	I _{DDPD}	V _{SYS} > 3.0 V LDOCORE enabled bucks and LDOs disabled		40	µA
ACTIVE mode	I _{DDACT}	All bucks and LDOs enabled		400	µA

5 Typical characteristics

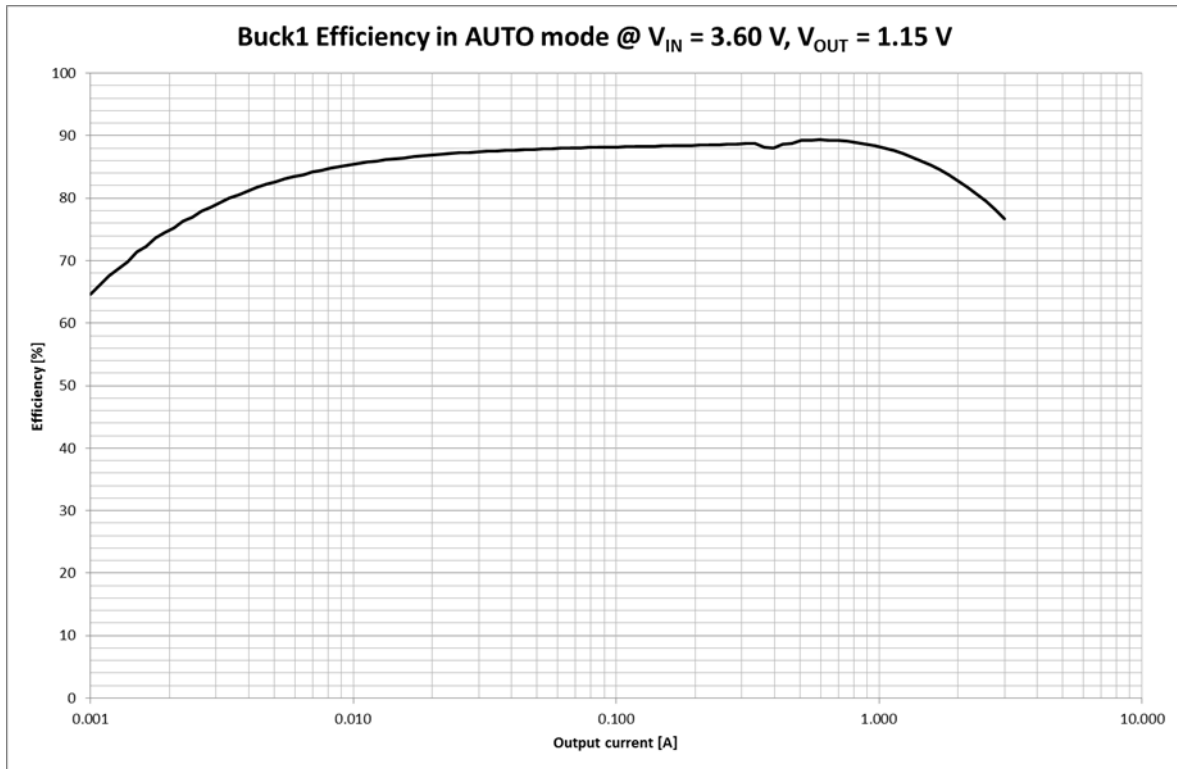


Figure 4: Buck1 efficiency in AUTO mode

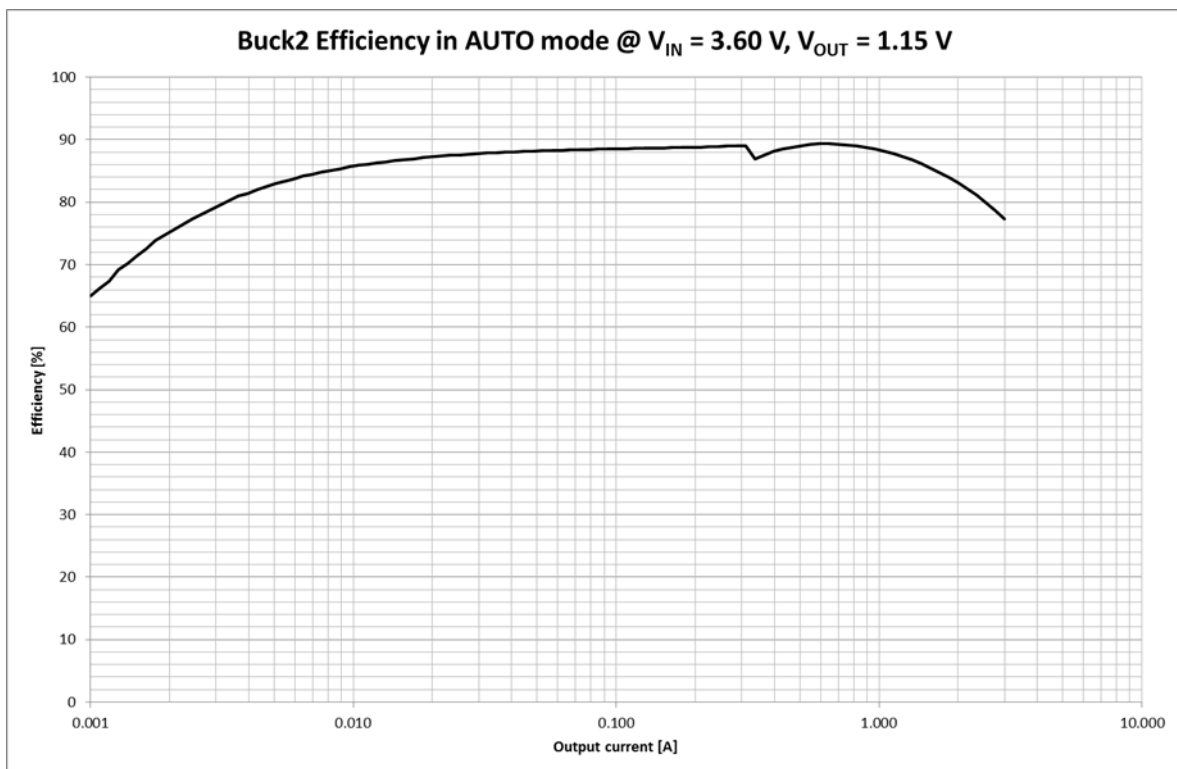


Figure 5: Buck2 efficiency in AUTO mode

Entry level PMIC for applications requiring up to 8.5 A

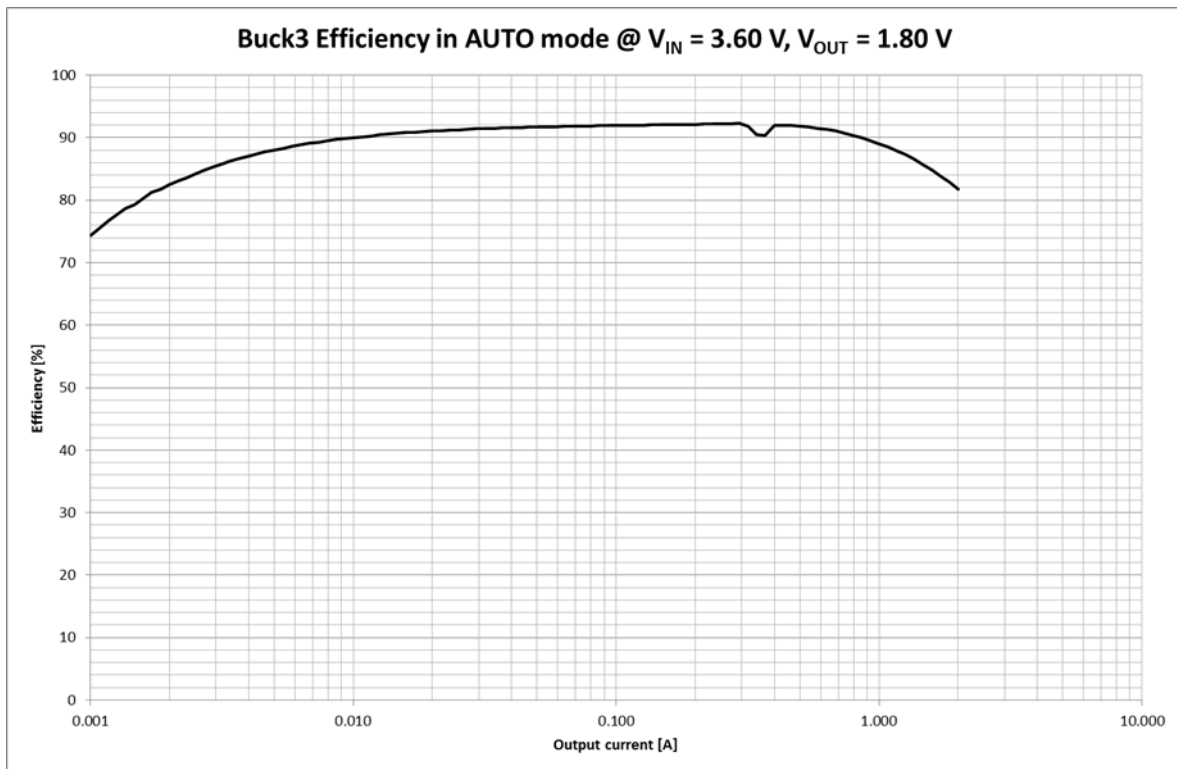


Figure 6: Buck3 efficiency in AUTO mode ($V_{IN} = 3.60\text{ V}$, $V_{OUT} = 1.80\text{ V}$)

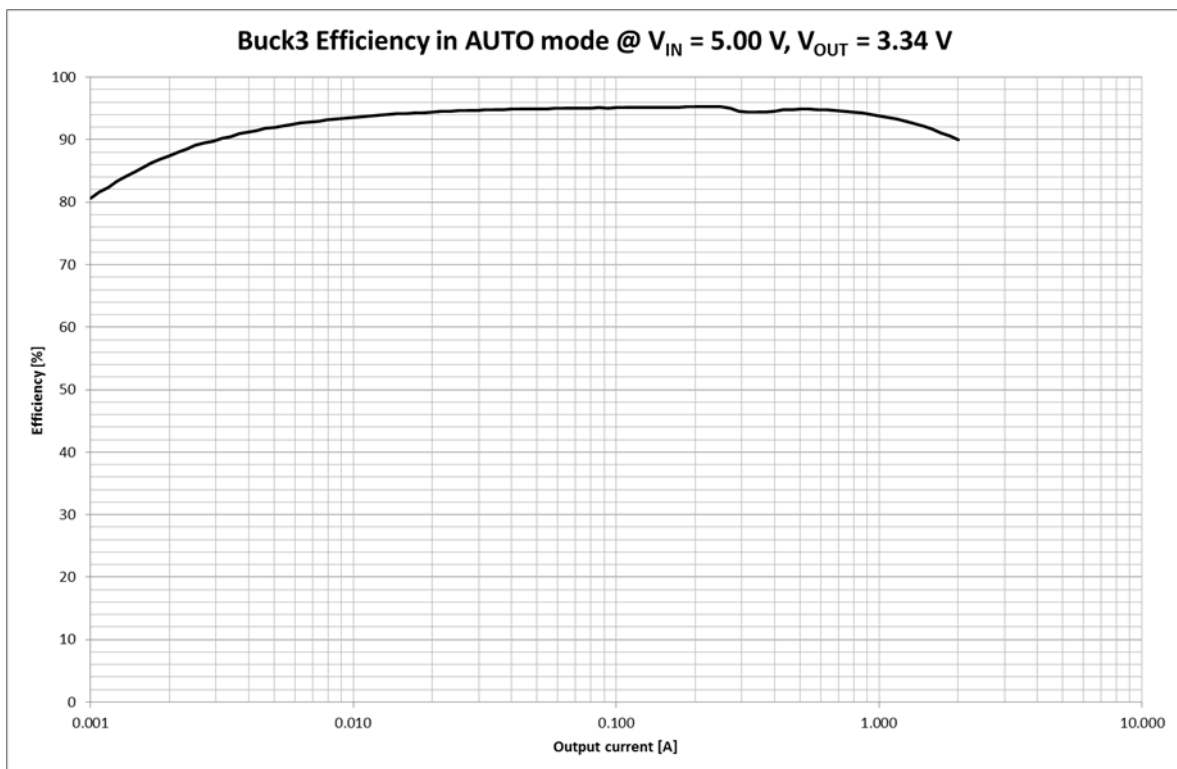


Figure 7: Buck3 efficiency in AUTO mode ($V_{IN} = 5.00\text{ V}$, $V_{OUT} = 3.34\text{ V}$)

Entry level PMIC for applications requiring up to 8.5 A

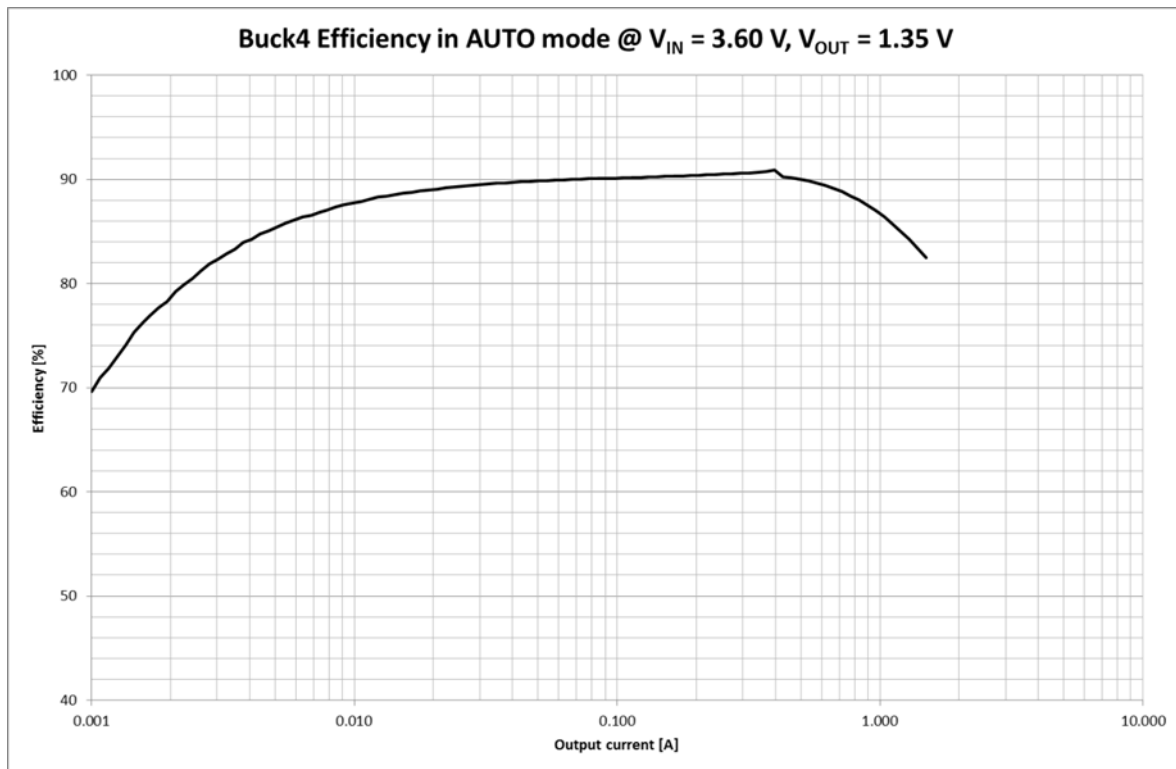


Figure 8: Buck4 efficiency in AUTO mode

Entry level PMIC for applications requiring up to 8.5 A

6 System block diagram

A block diagram for a typical application is illustrated in Figure 9.

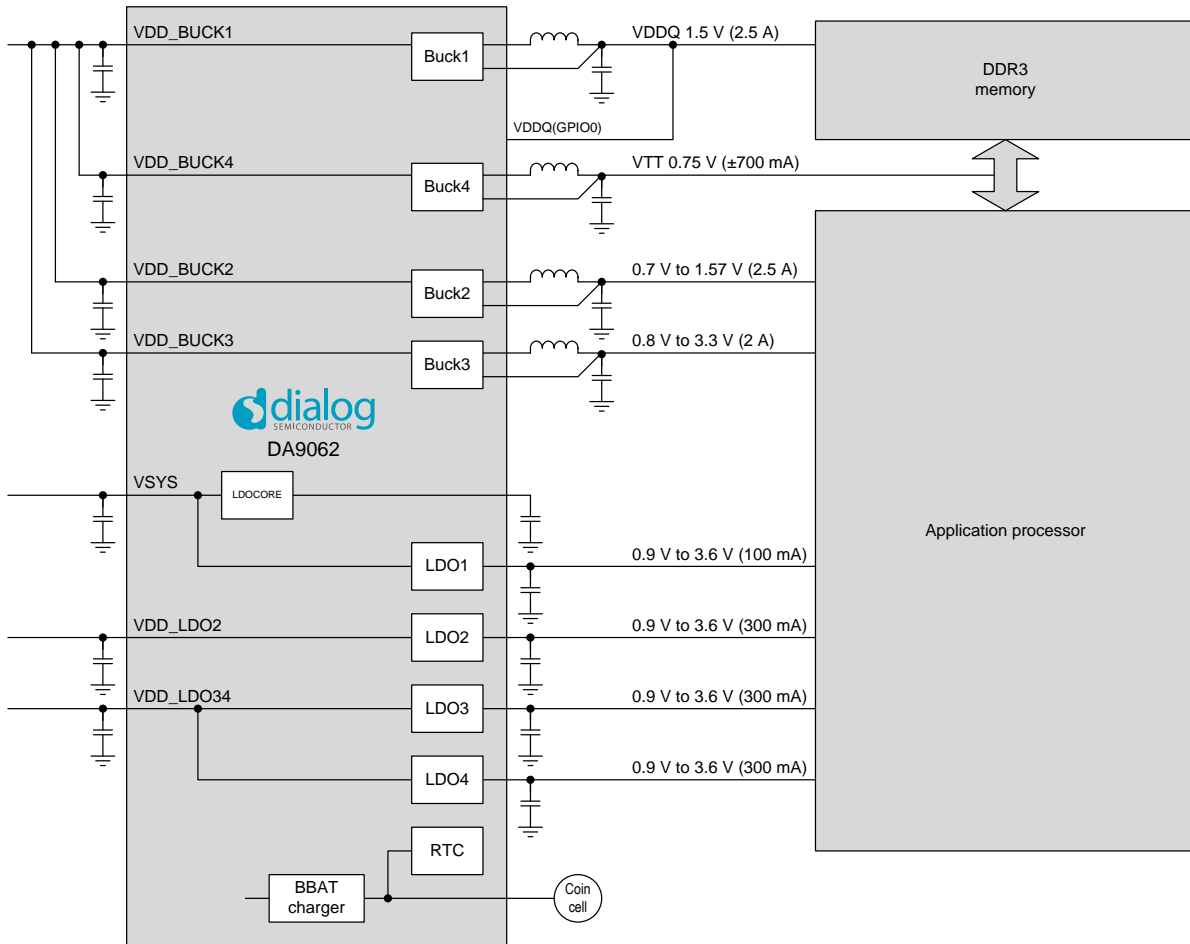


Figure 9: DA9062 typical system block diagram

Entry level PMIC for applications requiring up to 8.5 A

6.1 DDR power management

Using DA9062 for DDR power management is illustrated in Figure 10.

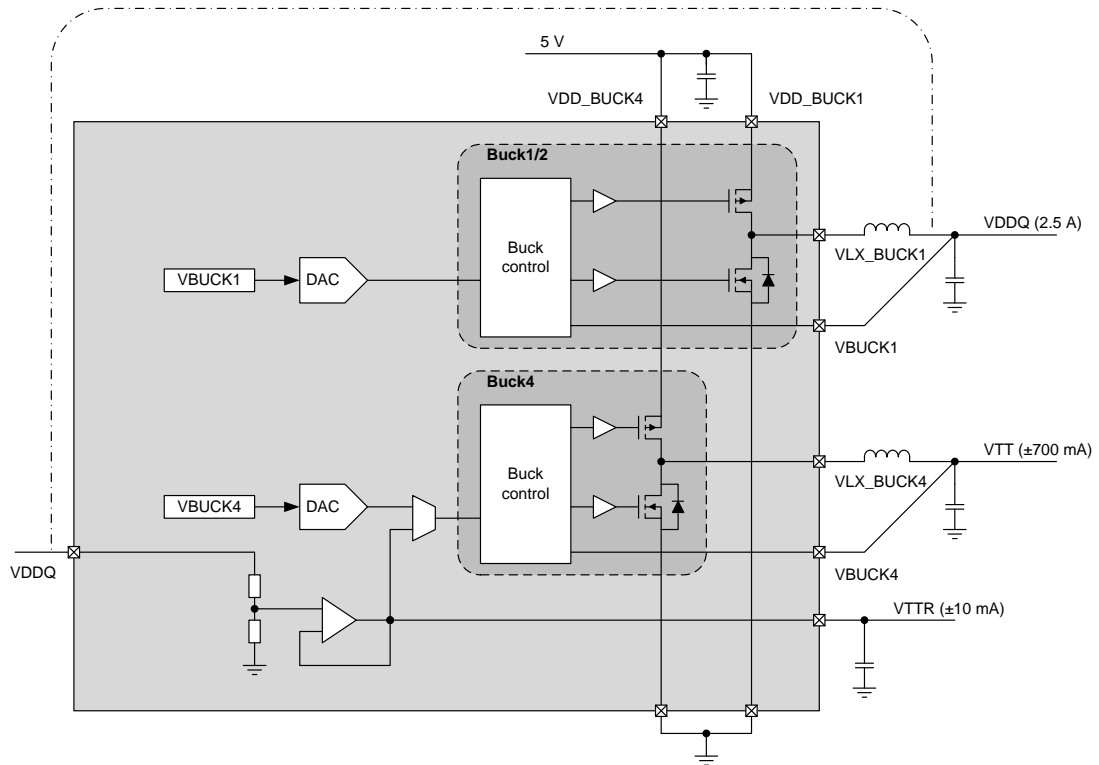


Figure 10: DA9062 DDR power management

Entry level PMIC for applications requiring up to 8.5 A

7 Functional description

7.1 Control signals

Each of the input signals described below feature a debounce filter. They share a common debounce time control (DEBOUNCING).

7.1.1 nONKEY

nONKEY is an edge-sensitive signal that controls the power mode of DA9062. Both falling and rising edges are detected and the time between the edges is measured. This enables different lengths of key press detection. The detection circuitry is enabled in all power modes of the device.

The status of the signal after debouncing can be read from NONKEY (reg. STATUS_A). The mask bit M_NONKEY prevents interrupt and wakeup events that would normally be caused by an nONKEY event.

nONKEY has four modes of operation, see [Table 20](#), which can be selected by NONKEY_PIN. NONKEY_LOCK controls the wakeup event generation of the nONKEY. If NONKEY_LOCK is asserted (depends on NONKEY_PIN), a short nONKEY press (shorter than KEY_DELAY) will not generate a wakeup.

Table 20: nONKEY functions

nONKEY_PIN	Function
00	An event (E_nONKEY) is generated when nONKEY is asserted. If not masked, the event causes an interrupt. A wakeup is triggered if the device is in POWERDOWN mode.
01	A timer is started when nONKEY is asserted. If the signal is de-asserted before the time programmed in KEY_DELAY, an event (E_nONKEY) is generated at the rising edge. If the signal stays asserted and the timer reaches the programmed value, an event is generated and nONKEY_LOCK is asserted.
10	A timer is started when nONKEY is asserted. If the signal is de-asserted before the time programmed in KEY_DELAY, an event (E_nONKEY) is generated at the rising edge. If the signal stays asserted and the timer reaches the programmed value, an event is generated, nONKEY_LOCK is asserted, and a power down is triggered by automatically clearing SYSTEM_EN.
11	A timer is started when nONKEY is asserted. If the signal is de-asserted before the time programmed in KEY_DELAY, an event (E_nONKEY) is generated at the rising edge, SYSTEM_EN is cleared, and STANDBY is asserted. If the signal stays asserted and the timer reaches the programmed value, an event is generated, nONKEY_LOCK is asserted, and SYSTEM_EN and STANDBY are cleared.

Whenever nONKEY_LOCK is asserted, a long key press (longer than the time programmed in KEY_DELAY) is required to wakeup from POWERDOWN mode. If the wakeup is also desired after a short key press, nONKEY_LOCK has to be cleared before entering the POWERDOWN mode.

7.1.2 nRESETREQ

nRESETREQ is an active-low reset request that causes DA9062 to enter RESET mode. The transition to the RESET mode is handled by the power sequencer and it can be sped up by setting the HOST_SD_MODE bit. Before entering the RESET mode, a fault log bit is set (nRESETREQ) and nRESET is asserted.

nRESETREQ should be tied to an always-on rail that is supplied in all modes of the DA9062 such as VSYS. It is not recommended to tie nRESETREQ to any of the regulator outputs. An internal pull-up resistor to V_{DDIO} can be enabled from nRESETREQ_PU. However, care should be taken to ensure that the V_{DDIO} is supplied in all power modes.

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7.1.3 nRESET

nRESET is an active-low reset output intended for resetting the host processor of the system. The signal can be configured as either push-pull or open drain output (PM_O_TYPE).

nRESET is always asserted upon a cold boot from the no-power mode. It is always asserted at the beginning of a shutdown sequence to the RESET mode. nRESET may also be asserted at the beginning of the sequence to the POWERDOWN mode, if configured in nRES_MODE.

De-assertion of nRESET is controlled by a reset timer. After being asserted, nRESET remains low until the reset timer, which was started from the selected trigger signal, expires. The reset timer trigger can be selected via RESET_EVENT and set to one of the following: an external signal triggering the wakeup (EXT_WAKEUP), an internal signal indicating the end of the first power-up sub-sequence (SYS_UP), an internal signal indicating the end of the second power-up sub-sequence (PWR_UP), or the transition of DA9062 from reset to POWERDOWN mode. The expiry time can be configured via RESET_TIMER from 1 ms to 1 s. If RESET_TIMER is set to 0 ms, nRESET is de-asserted immediately after the trigger selected with RESET_EVENT.

7.1.4 nIRQ

nIRQ is a level-sensitive interrupt signal. It can be configured either as a push-pull or an open drain output (selected via PM_O_TYPE). The polarity of nIRQ can be selected with IRQ_TYPE.

nIRQ is asserted when an unmasked event has occurred. The nIRQ will not be released until all event registers have been cleared. New events that occur while reading an event register are saved until the event register is cleared, ensuring that the host processor captures them. The same will happen to all events occurring when the power sequencer is in transition.

7.2 2-wire interface

The 2-wire interface provides access to the control and status registers. The interface supports operations compatible to the standard, fast, fast-plus, and high-speed modes of the I²C bus specification Rev. 3. Communication on the 2-wire bus is always between two devices; one acting as the master and the other as the slave. The DA9062 only operates as a slave.

SCL transmits 2-wire clock data and SDA transmits the bidirectional data. The 2-wire interface is open-drain supporting multiple devices on one line. The bus lines have to be pulled high by an external pull-up resistor (2 to 20 k Ω). The attached devices drive the bus lines low by connecting them to ground. As a result, two devices can drive the bus simultaneously without conflict. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the DA9062 internal clock signals. DA9062 stays within the described host clock speed limitations and does not initiate clock slow-down. An automatic interface reset is triggered when the clock signal ceases toggling for >35 ms (controlled in TWOWIRE_TO).

When the SDA is stuck, the bus clears after receiving nine clock pulses. Operation in high-speed mode at 3.4 MHz requires a minimum interface supply voltage of 1.8 V and a mode change in order to enable slope-control. The high-speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. The DA9062 does not make use of clock stretching and delivers read data without delay up to 3.4 MHz.

Alternatively, the interface can be configured to use high-speed mode continuously via PM_IF_HSM, so that the master code is not required at the beginning of every transfer. This reduces communication overhead on the bus and limits the attachable bus slaves to compatible devices.

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7.2.1 Register map paging

The 2-wire interface has direct access to two pages of the DA9062 register map (up to 256 addresses). The register at address zero on each page is used as a page control register (the LSB of control PAGE is ignored). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 is selected using control REVERT. Unless REVERT was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

DA9062 also offers an alternative way to access register pages which avoids writing explicitly to PAGE. DA9062 responds to multiple consecutive slave addresses and updates PAGE automatically based on the slave address. For example, when IF_BASE_ADDR[7:4] = 0xB the slave address changes PAGE as follows:

Slave address = 0xB0 ⇒ PAGE = 0x00

Slave address = 0xB2 ⇒ PAGE = 0x02

7.2.2 Details of the 2-wire protocol

All data is transmitted across the 2-wire bus in 8-bit groups. To send a bit, the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL stores the SDA bit in the receiver's shift register.

A 2-byte serial protocol is used: one address byte and one data byte. Data and address transfer transmits the MSB first for both read and write operations. All transmissions begin with the START condition from the master during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in high state. The START and STOP conditions are illustrated in [Figure 11](#).

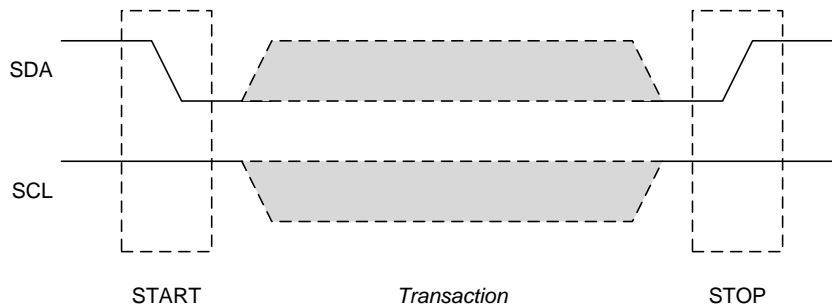


Figure 11: Timing of the START and STOP conditions

DA9062 monitors the 2-wire bus for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. DA9062 responds to all bytes with an ACK. A register write operation is illustrated in [Figure 12](#).

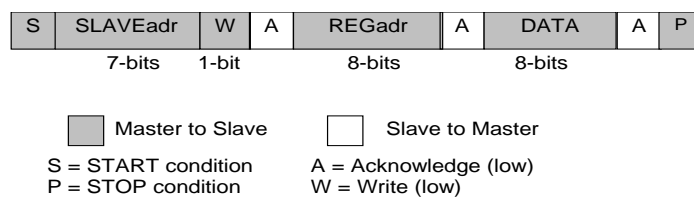


Figure 12: Byte write operation

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When the host reads register data the DA9062 first has to access the target register address with write access and then with read access and a repeated START, or alternatively a second START, condition. After receiving the data, the host sends NACK and terminates the transmission with a STOP condition, see [Figure 13](#).

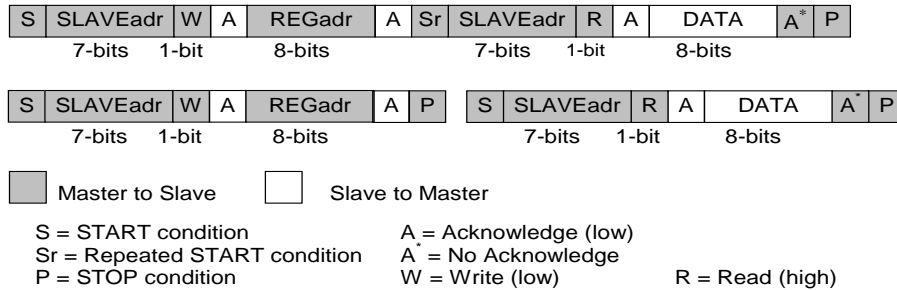


Figure 13: Examples of byte read operations

Consecutive (page) read-out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte, see [Figure 14](#). The 2-wire control block then increments the address pointer to the next register address and sends the data to the master. The data bytes are read continuously until the master sends a NACK followed by a subsequent STOP condition directly after receiving the data. If a non-existent 2-wire address is read out then the DA9062 will return code zero.

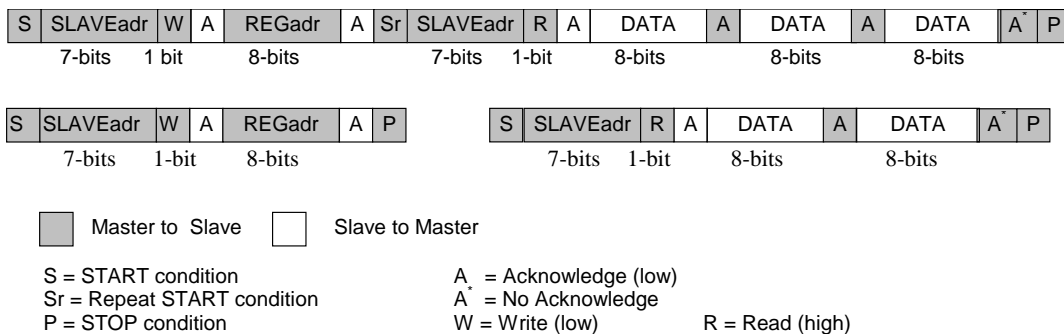


Figure 14: 2-wire page read

The slave address after the repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes after sending the register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data, and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in [Figure 15](#).

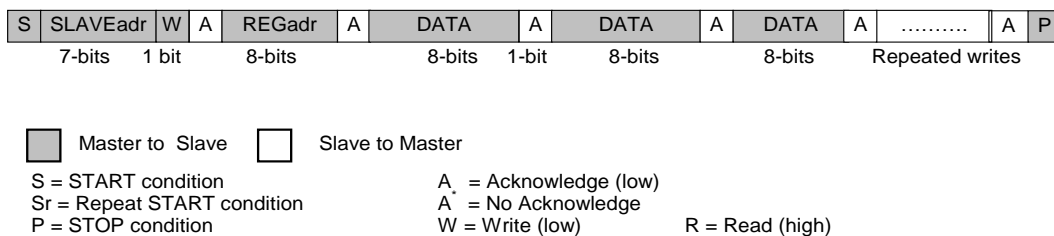


Figure 15: 2-wire page write

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A repeated write mode can be enabled with WRITE_MODE control. In this mode, the master can execute back-to-back write operations to non-consecutive addresses by transmitting register addresses and data pairs. The data is stored in the address specified by the preceding byte. The repeated write mode is illustrated in Figure 16.

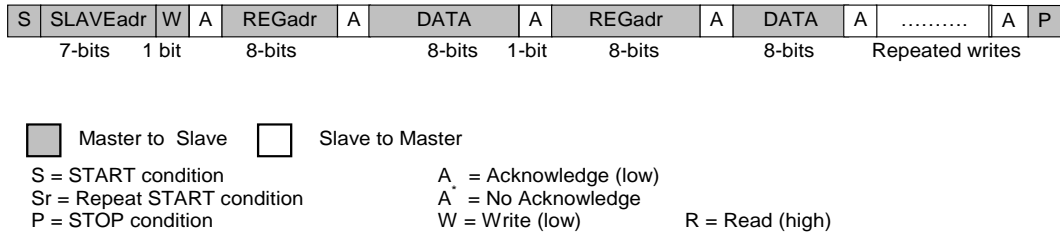


Figure 16: 2-wire repeated write

If a new START or STOP condition occurs within a message, the bus returns to idle mode.

7.3 GPIOs

DA9062 features five general purpose IO pins. The basic structure of the GPIOs is depicted in Figure 17. As illustrated, there are several additional functions:

- analog function
- alternate function
- forwarding
- regulator control
- sequencer WAIT_STEP
- interrupt and wakeup generation

The GPIOs are operational in POWERDOWN and ACTIVE modes. However, GPIOs can be configured as disabled in POWERDOWN mode in register PD_DIS (control GPI_DIS). In other modes, the GPIO is disabled and all ports are configured as open drain outputs in high impedance state. The level transitions on inputs will no longer be detected, but I/O drivers will keep their configuration and programmed levels.

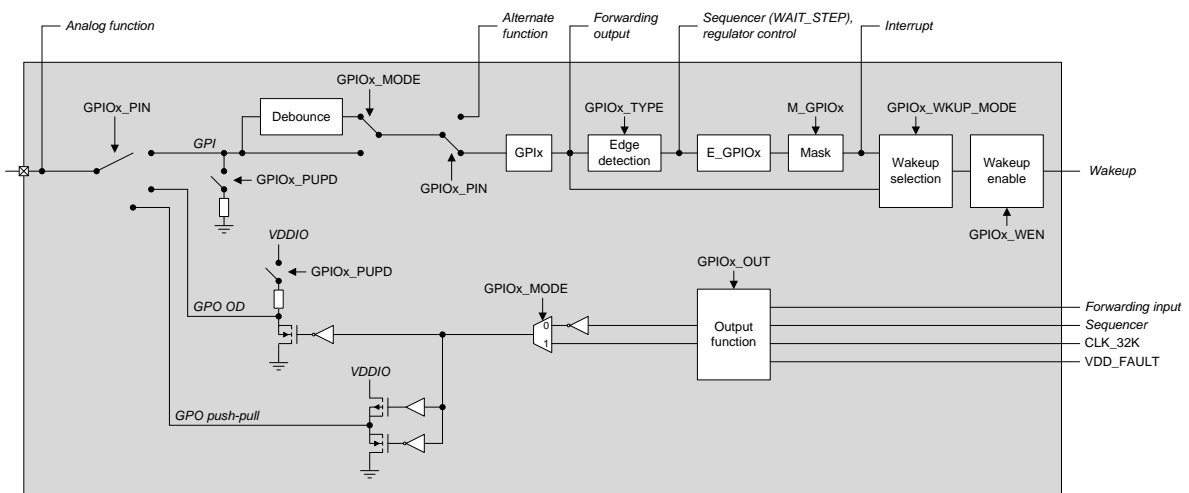


Figure 17: General GPIO block diagram

The functionality of a GPIO is configured in GPIO<x>_PIN, as listed in Table 21.

Entry level PMIC for applications requiring up to 8.5 A

Table 21: GPIO functions

GPIO<x>_PIN	Function	GPIO<x>_MODE	GPIO<x>_TYPE	GPIO<x>_WKUP_MODE	GPIO<x>_WEN
0	Alternate function	<i>No effect</i>	<i>No effect</i>	<i>No effect</i>	<i>No effect</i>
1	GPI	0: Debounce off 1: Debounce on	0: Active low 1: Active high	0: Edge-sensitive wakeup 1: Level-sensitive wakeup	0: Wakeup disabled 1: Wakeup enabled
2	GPO Open drain	0: Output low 1: Output high	<i>No effect</i>	<i>No effect</i>	<i>No effect</i>
3	GPO Push-pull	0: Output low 1: Output high	<i>No effect</i>	<i>No effect</i>	<i>No effect</i>

7.3.1 GPI functionality

In GPI mode, the polarity of the input can be selected with GPIO<x>_TYPE. A debouncing filter can be applied on the input signals with a configurable debouncing time (DEBOUNCING). An event is generated at the active edge of the input. The active edge is determined by the signal polarity configured in GPIO<x>_TYPE. The event can be further configured to generate a wakeup via GPIO<x>_WKUP_MODE and GPIO<x>_WEN. An internal pull-down can be activated for the inputs in GPIO<x>_PUPD.

A level sensitive wakeup event can also be configured for each GPI via GPIO<x>_WKUP_MODE and GPIO<x>_WEN. The functionality of the level-sensitive wakeup is described in [Table 26](#).

7.3.1.1 Regulator control

GPIO1, GPIO2, and GPIO3 can be used for controlling DA9062 regulators. When configured as GPIs, they can be used to enable regulators or select between their two output voltage settings.

As seen in [Figure 17](#), the regulator control is branched after the GPIO<x>_TYPE control allowing active edge delegation for the regulator control. Finally, the functionality for the GPI is selected with the regulator controls BUCK<x>_GPI, LDO<x>_GPI, VBUCK<x>_GPI, and VLDO<x>_GPI.

One GPI can be used to control the same function on multiple regulators simultaneously. When a regulator is controlled by a GPI, the same function (on/off or voltage selection) can no longer be controlled by the power supply sequencer. The regulator still responds normally to register writes to the control bit.

Enable/disable control

A GPI is used for enabling/disabling regulators when it is selected in one of the BUCK<x>_GPI or LDO<x>_GPI controls. A passive to active transition sets the regulator enable bit (BUCK<x>_EN, LDO<x>_EN), and an active to passive transition clears it.

Output voltage control

A GPI is used for the output voltage selection when it is selected in one of the VBUCK<x>_GPI or VLDO<x>_GPI controls. A passive to active transition sets the voltage selection bit (VBUCK<x>_SEL, VLDO<x>_SEL), and an active to passive edge clears it.

7.3.1.2 Sequencer WAIT_STEP

GPIO3 can be used for the WAIT_STEP functionality. The power sequencer can be programmed to wait for either a rising or falling edge of the WAIT_STEP input, see [Section 7.9.4](#). The active edge is selected from GPIO<x>_TYPE.

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7.3.2 GPO functionality

The outputs can be configured as push-pull or open drain outputs, see [Table 21](#). An internal pull-up can be enabled/disabled from GPIO<x>_PUPD (open drain mode). The GPIO<x>_MODE settings can control the output state.

Instead of controlling the output with GPIO<x>_MODE, a selection of alternatives is available in the GPIO<x>_OUT controls. These include: the forwarding function, see [Section 7.3.4](#), the power supply sequencer, see [Section 7.9](#), the 32 kHz clock, and the status of the voltage supervision (VDD_FAULT). When the GPIO is configured as an output and GPIO<x>_OUT is set to 0x0, the GPIO<x>_MODE determines the state of the output.

7.3.2.1 nVDD_FAULT

nVDD_FAULT gives the status of the system supply monitoring, see [Section 7.11](#). The assertion of nVDD_FAULT indicates that the main supply input voltage is low ($V_{SYS} < VDD_FAULT_UPPER$) and therefore informs the host processor that the power will soon shut down. It can be configured to drive a GPO from the GPIO<x>_OUT controls. The driver type (push-pull, open drain) selection and pull-up resistor control function normally. The GPIO<x>_MODE can be used to invert the incoming VDD_FAULT signal.

7.3.2.2 OUT_32K

OUT_32K feeds a buffered 32 kHz clock signal that is derived from the internal oscillator. The signal output buffer can be controlled either with the power sequencer or manually via EN_32KOUT, and paused automatically during POWERDOWN mode with the OUT_32K_PAUSE bit.

Glitch-free switching between a 32 kHz clock output and another GPIO configuration is not guaranteed. Therefore, configuring a GPIO for 32 kHz clock output should only be done in OTP. However, enabling and disabling the buffer is still dynamic as described above.

7.3.3 Alternate functions

GPIO0, GPIO2, and GPIO4 can be used for alternate functions. These are digital control signals that don't employ the debouncing, event detection, or interrupt generation functions. Only the input buffer of the GPIO block is employed. The alternate functions of DA9062 are listed in [Table 22](#) and described in the following subsections. A debouncing filter can be applied also on the alternate functions with a configurable debouncing time (DEBOUNCING).

Table 22: GPIO alternate input functions

GPIO	Alternate function	Description
GPIO0	WDKICK	Watchdog kick or disable
GPIO1	-	
GPIO2	PWR_EN	Power mode control
GPIO3	-	
GPIO4	SYS_EN	Power mode control

7.3.3.1 SYS_EN

SYS_EN (pin GPIO4) controls the SYSTEM_EN bit and thereby the power mode of DA9062. It is part of the power supply sequencer functionality described in [Section 7.9](#). SYS_EN is an edge-sensitive signal and its polarity can be chosen in the GPIO4_TYPE control.

Asserting SYS_EN causes an interrupt (E_GPIx) and a wakeup event. De-asserting SYS_EN triggers a power down sequence but no interrupt.

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7.3.3.2 PWR_EN

PWR_EN (pin GPIO2) controls the POWER_EN bit and thereby the power mode of DA9062. It is part of the power supply sequencer functionality described in Section 7.9. PWR_EN is an edge-sensitive signal and its polarity can be chosen in the GPIO2_TYPE control. A wakeup event can be generated after assertion of PWR_EN if so configured in GPIO2_WEN.

7.3.3.3 WDKICK

A rising edge of the WDKICK signal resets the watchdog counter. The polarity of the signal can be chosen in the GPIO0_TYPE control. If the signal is kept asserted, the watchdog is disabled as the counter is not incremented (WDG_MODE), see Section 7.15.

7.3.4 GPIO forwarding

GPIO forwarding works between GPIOs 0, 1, 2, and 3. Any of these GPIOs can be routed directly to GPO0, 1, and 3 after debouncing. Forwarding is one of the options for the GPIO<x>_OUT control.

7.3.5 Analog functions

GPIO0 and GPIO1 can be used as analog IOs. In this case, the normal GPIO functions are disabled. The analog functions and their corresponding control bits are listed in Table 23.

Table 23: GPIO analog functions

GPIO	Analog function	Control
GPIO0	VDDQ	BUCK4_VTT_EN
GPIO1	VTTR	BUCK4_VTTR_EN
GPIO2	-	
GPIO3	-	
GPIO4	-	

7.4 Dynamic voltage control

All of DA9062's buck converters can be controlled in several ways to achieve dynamic voltage control (DVC). The buck converters feature a voltage ramping feature that enables smooth transition from one voltage setting to another.

All output voltages can be controlled with SW via the 2-wire interface (VBUCK<x>_A). The 2-wire interface is operational when the device is in ACTIVE mode.

7.5 Regulator voltage A and B selection

In addition, all regulators feature A and B settings which can be programmed with different voltages (VBUCK<x>_A, VBUCK<x>_B), one of which is chosen according to the operating mode of the system (VBUCK<x>_SEL, VLDO<x>_SEL). In addition to the output voltage, the A and B settings include a bit to force the regulator into SLEEP mode which reduces the quiescent current.

The selection between the A and B settings can be done either with SW via the 2-wire interface or by the power sequencer, see Section 7.9. Furthermore, each regulator can be enabled with a GPI pin, see Section 7.3.1.1, and the selection between the A and B settings done with another GPI.

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7.6 LDOs

All LDOs employ Dialog Semiconductor's Smart Mirror™ dynamic biasing technology, see [Figure 18](#), which maintains high performance over a wide range of operating conditions and a power saving mode (SLEEP mode) to minimise the quiescent current during very low output current. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is maintained across the full operating current range however quiescent current consumption is scaled to demand improved efficiency when current demand is low.

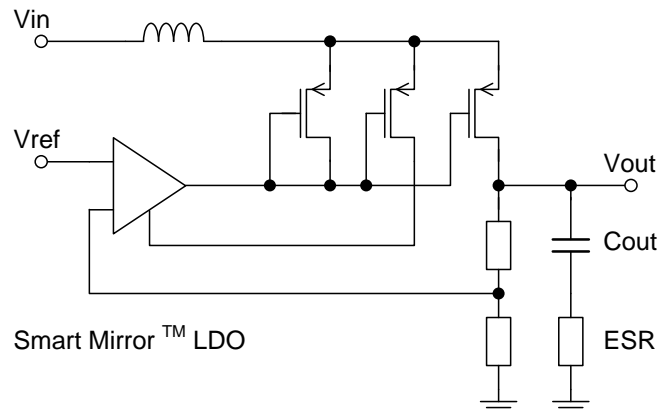


Figure 18: Smart Mirror™ voltage regulator

7.6.1 Control

The LDOs can be enabled by writing directly to a control bit (LDO<x>_EN), controlling it via a GPI, see [Section 7.3.1.1](#), or assigning it to a power sequencer step, see [Section 7.9.2](#). Each LDO features two voltage control registers (VLDO<x>_A/VLDO<x>_B) that allow two output voltage pre-configurations. The active setting can then be selected either with a control bit (VLDO<x>_SEL), via a GPI, see [Section 7.3.1.1](#), or automatically based on the DA9062 power mode. The SLEEP mode of the LDOs can be linked to either the A or B setting (LDO<x>_SL_A/LDO<x>_SL_B). Therefore, the LDO will switch to SLEEP mode when the setting is active.

LDO1 differs from the other LDOs because it can be configured as an always-on regulator. This means that it is also enabled in RESET mode, see [Section 7.8.3](#).

7.6.2 Current limit

Each LDO provides over-current detection. The current limit is fixed for each LDO based on their current capability. If any of the LDOs' current limit is exceeded for longer than 10 ms, an event, E_LDO_LIM, is triggered. The status of the limit comparator can be observed from LDO<x>_ILIM (reg. STATUS_D). If an LDO's current limit is exceeded for longer than 200 ms, the LDO is automatically disabled. This shutdown feature can be disabled by clearing the LDO_SD control. Once disabled due to an over-current, the LDO must be re-enabled by one of the sources described in [Section 7.6.1](#).

7.6.3 Output pull-down

When overvoltage ($1.06 \cdot VLDOx$) occurs, the voltage regulators enable an internal load to discharge the output back to its configured voltage. This feature can be disabled in LDO<x>_PD_DIS.

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7.7 Switching regulators

DA9062 includes four step-down switching regulators operating at 3 MHz. All switching regulators employ a synchronous topology with an internal NFET, thus eliminating the need for an external Schottky diode. The output voltage can be set in 10 mV steps (20 mV steps for Buck3) and the regulation accuracy is $\pm 3\%$ over the whole operating temperature range. Static line and load regulation are also considered in this accuracy.

The switching frequency (3 MHz) is high enough to warrant the use of a small 1.0 μH inductor. The programming of the converter current limit depends on the coil parameters, as illustrated in [Table 24](#).

Table 24: Buck current limit

Min. ISAT (mA)	Frequency (MHz)	Buck current limit (mA)
1750	3	1500
1460	3	1200
1180	3	950
940	3	750

7.7.1 Control

The buck can be enabled manually by writing directly to a control register, with an external signal connected to GPI, see [Section 7.3.1.1](#), or by assigning it to a power sequencer step, see [Section 7.9.2](#). Each buck converter features two voltage control registers (VBUCK<x>_A/VBUCK<x>_B) which can be programmed with two different voltages. The active setting can then be selected via a control bit (VBUCK<x>_SEL), via a GPI, see [Section 7.3.1.1](#), or automatically based on the power mode of DA9062.

7.7.2 Output voltage slewing

To limit in-rush current from the input supply, the buck converters can achieve a new output voltage with controlled ramping. Ramping is achieved by stepping through all the V_{BUCK} values between the old and new settings, at a rate defined by SLEW_RATE. The actual output slew rate, in $\text{mV}/\mu\text{s}$, for a particular buck converter is then defined by the minimum voltage step of that buck and the common step time programmed in SLEW_RATE. During PFM mode, the negative slew rate is load dependent and might be lower than the one mentioned above. An event E_DVC_RDY is triggered when all buck converters have reached their target voltage.

7.7.3 Soft-start

The buck converter supports two options for starting up. The normal startup option ramps up the power rail as fast as possible, typically within 1 ms. This implies a high in-rush current. The slow startup is selected by setting BUCK_SLOWSTART, which increases the startup time and limits the input current.

7.7.4 Active discharge

When switching off a buck converter the output rail can be actively discharged. This feature is enabled by setting BUCK_ACTV_DISCHRG. The discharge is implemented by ramping down the output voltage using DVC.

7.7.5 Peak current limit

All buck converters feature a programmable current limit (BUCK<x>_ILIM). The current limit protects the inductor and the pass devices from excessive current. If the current limit is exceeded, the buck continues to run normally but the duty cycle is limited.

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7.7.6 Operating mode

The operating mode of each converter can be set via the buck control (BUCK<x>_MODE) to synchronous (PWM), sleep (PFM), or auto. In auto mode the buck converter switches between PWM and PFM depending on the load current. This mode is recommended for applications that require fast transitions from synchronous to sleep operation. The current consumption during PWM operation is 10 mA and drops to <math><1 \mu\text{A}</math> in shutdown.

In addition, the buck mode can be controlled with the A and B setting. If BUCK<x>_SL_B is set, the buck is forced to SLEEP mode when the B setting is active. Similarly, if BUCK<x>_SL_A is set, the buck is forced to SLEEP mode when the A setting is active.

7.7.7 Half-current mode

Buck1 and Buck2 can operate in half-current mode where the quiescent current is reduced by disabling half of the pass devices. As the name implies, enabling this option halves the output current, and therefore, this feature is valuable in applications where quiescent current is critical and full current is not needed. This feature is controlled with BUCK1_FCM and BUCK2_FCM. If the bit is asserted (BUCK<x>_FCM = 1), the corresponding buck is in full-current mode and the full current is available. If the bit is de-asserted, the corresponding buck is in half-current mode. Operating the bucks in full-current mode requires twice as much output capacitance ($2 \times 47 \mu\text{F}$) as the half-current mode ($2 \times 22 \mu\text{F}$).

7.7.8 Buck4 in DDR memory bus termination mode

Buck4 can be used to generate the DDR memory termination voltage, VTT. In this mode, Buck4 tracks the divided VDDQ voltage and it is able to both sink and source current. As described in Section 7.3.5, GPIO0 can be configured to carry the VDDQ and GPIO1 can be configured to carry the VTTR signal. The VTTR output provides buffered version of the $VDDQ/2$ voltage with ± 10 mA source/sink capability (requires $0.1 \mu\text{F}$ stabilisation capacitor), see Figure 19. When used for memory termination, Buck4 has to be forced in the synchronous mode from the BUCK4_MODE control. If BUCK4_VTT_EN and BUCK4_VTTR_EN are asserted at the same time, the VTTR provides a buffered VTT reference, but otherwise Buck4 is running in a normal output voltage control mode.

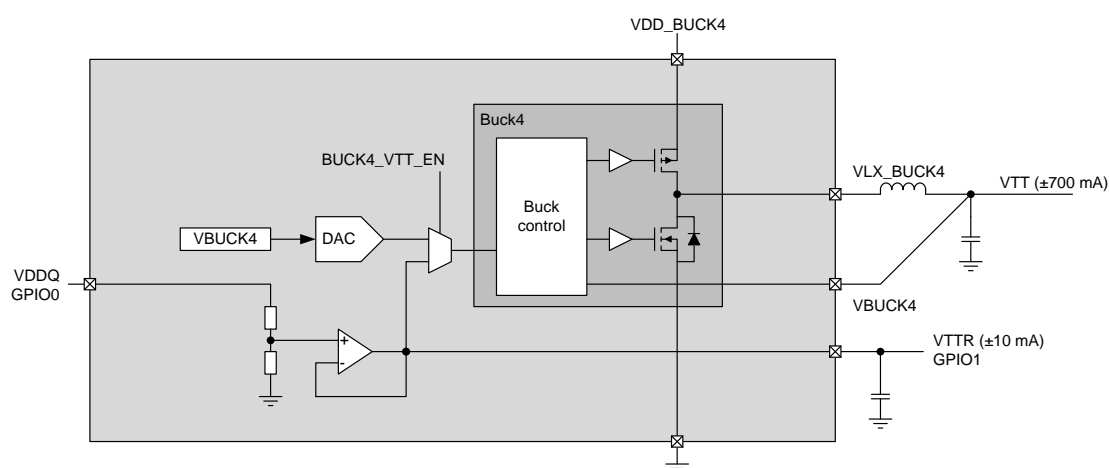


Figure 19: Buck4 DDR memory bus termination mode

Table 25: Buck4 VTT mode control

BUCK4_VTT_EN	BUCK4_VTTR_EN	Buck4 mode	Buck4 VREF	GPIO0	GPIO1
0	0	Normal	VDAC	Digital I/O	Digital I/O
0	1	Normal	VDAC	VDDQ	VTTR
1	0	VTT	$VDDQ/2$ un-buffered	VDDQ	Digital I/O
1	1	VTT	$VDDQ/2$ buffered	VDDQ	VTTR

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7.8 Power modes

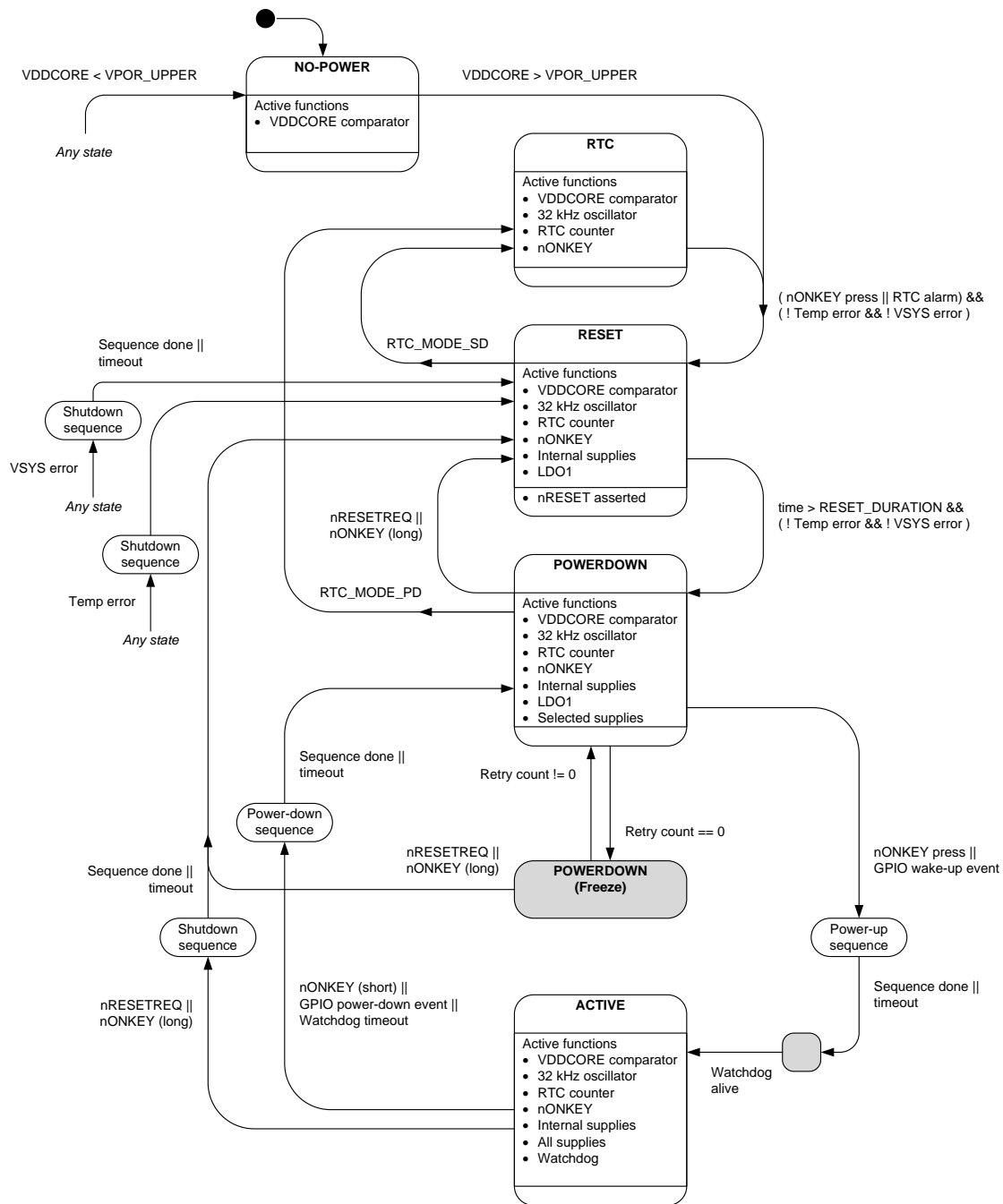


Figure 20: DA9062 power modes (state transition conditions follow C-language syntax)

7.8.1 NO-POWER mode

The NO-POWER mode is initial state when powering up the DA9062 for the first time. When the system supply rises above a threshold, DA9062 enters RESET mode.

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7.8.2 RTC mode

The RTC mode is a low-power mode with only a minimum set of functions to maintain the system time. All supplies are disabled. RTC mode is entered either after a SW request or when the backup battery is the only supply. If enabled in RTC_MODE_PD, the power sequencer proceeds automatically from the POWERDOWN state to RTC mode. If the system supply is removed, DA9062 will also enter RTC mode. Supply recovery will trigger an exit from RTC mode automatically. DA9062 will exit RTC mode when nONKEY is asserted, or an RTC alarm is raised. GPIOs are not operational in RTC mode.

7.8.3 RESET mode

In RESET mode, the internal supplies, and LDO1 (if configured as an always-on supply) are enabled. All other DA9062 supplies are disabled.

DA9062 is in RESET mode whenever a complete application shutdown is required. RESET mode can be triggered by the user, a host processor, or an internal event.

RESET mode can be triggered by the user:

- from a long press of nONKEY (interruptible by host)
- by pressing a reset switch that is connected to port nRESETREQ (non-interruptible)

RESET mode can be forced from the host processor (non-interruptible):

- by asserting port nRESETREQ (falling edge)
- by writing to register bit SHUTDOWN

DA9062 error conditions that force RESET mode (non-interruptible) are:

- no WATCHDOG write (WDKICK signal assertion) from the host inside the watchdog time window (if watchdog was enabled)
- an undervoltage detected at V_{SYS} ($V_{SYS} < VDD_FAULT_LOWER$)
- an internal die over-temperature

With the INT_SD_MODE, HOST_SD_MODE and KEY_SD_MODE controls, the shutdown sequences from internal fault, host or user triggered, are individually configured to either implement the reverse timing of the power-up sequence or transfer immediately to the RESET mode by skipping any delay from sequencer or dummy slot timers. For the host to determine the reason for the reset a FAULT_LOG register stores the root cause (either KEY_RESET or NRESETREQ). The host processor resets this register by writing asserted bits with '1'.

KEY_SD_MODE = 1 triggers a complete power on reset (POR) (instead of entering RESET mode) after the related keys are pressed extendedly.

If an OTP read is aborted, DA9062 enters RESET mode without an asserted bit inside register FAULT_LOG.

A shutdown sequence to RESET mode will start with the assertion of the nRESET port. After the sequencer completes the power down sequence (sequencer position 0), DA9062 continues to RESET mode with only the following active circuits: LDOCORE (at reduced output voltage 2.2 V), control interfaces and GPIOs, BCD counter, band-gap and over-temperature/VSYS comparators. All regulators, except for LDO1 and the backup battery charger, are automatically disabled to avoid battery drainage. As described in Section 7.1.3, nRESET is always asserted at the beginning of a shutdown sequence to RESET mode, and remains asserted when DA9062 is in RESET mode.

When entering the reset state, all user and system events are cleared and the DA9062's register configuration will be re-loaded from OTP when leaving the RESET mode (with the exception of AUTO_BOOT in case of a VDD_START fault).

FAULT_LOG, GP_ID_10 to GP_ID_19 and other non-OTP loaded registers, for example the RTC calendar and alarm, will not be changed when leaving the RESET mode.

Some reset conditions like asserting SHUTDOWN via register write, watchdog error, or junction over-temperature will automatically expire. Other reset triggers, like asserting nRESETREQ, need to be

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released to proceed from reset to POWERDOWN mode. If the application requires regulators to discharge completely before a power-up sequence, a minimum duration of the RESET mode can be selected via RESET_DURATION.

If the reset was initiated by a user's long press of nONKEY, initially only KEY_RESET is set and the nIRQ port will be asserted. KEY_RESET signals the host that a shutdown sequence is started. If the host does not then clear KEY_RESET within 1 second by writing a '1' to the related bit in register FAULT_LOG, the shutdown sequence will complete. When the reset condition has disappeared, DA9062 requires a supply (VSYS > VDD_FAULT_UPPER) that provides enough power to start-up from the POWERDOWN mode.

RESET mode also allows automatic transition to RTC mode where all features of DA9062, except the RTC oscillator and calendar (including LDOCORE), are disabled. This mode is selected in RTC_MODE_SD.

7.8.4 POWERDOWN mode

The POWERDOWN mode is a low-power state where most of the regulators are disabled. The transition from active to POWERDOWN mode (and vice versa) is handled by the programmable sequencer. Entry to POWERDOWN mode from ACTIVE mode is triggered by the de-assertion of SYSTEM_EN (either via SYS_EN or register access) or by a short press of nONKEY. The POWERDOWN mode is also passed during start-up and shutdown to RESET mode sequences.

In POWERDOWN mode the internal supplies are enabled, and the control interface and GPIOs are operational.

The power state machine features a retry counter that limits the number of transitions from POWERDOWN to ACTIVE under certain conditions. A watchdog timeout triggers POWERDOWN mode entry, but it does not necessarily clear the conditions that trigger a transition back to the ACTIVE mode. This could cause an endless loop between the ACTIVE and POWERDOWN modes. Therefore, after each watchdog timeout the retry counter is decremented, and after the retry counter reaches zero, DA9062 blocks all wakeup events and stays in POWERDOWN mode. This freeze function can be regarded as a substate of the POWERDOWN mode that is undetectable from outside the DA9062.

Table 26 describes the state transitions with a level-sensitive wakeup and the freeze function.

Table 26: State transitions with a level-sensitive (LS) GPI

Current state	LS GPI	SYS_EN	PWR_EN	Freeze Note 1	Next state
POWERDOWN	x	x	x	1	POWERDOWN
POWERDOWN	0	0	x	0	POWERDOWN
POWERDOWN	x	1	0	0	SYSTEM
POWERDOWN	x	1	1	0	ACTIVE
POWERDOWN	1	x	0	0	SYSTEM
POWERDOWN	1	x	1	0	ACTIVE
SYSTEM	0	0	x	x	POWERDOWN
SYSTEM	x	1	0	x	SYSTEM
SYSTEM	x	1	1	x	ACTIVE
SYSTEM	1	x	0	x	SYSTEM
SYSTEM	1	x	1	x	ACTIVE
ACTIVE	0	0	x	x	POWERDOWN
ACTIVE	x	1	0	x	SYSTEM
ACTIVE	x	1	1	x	ACTIVE

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Current state	LS GPI	SYS_EN	PWR_EN	Freeze Note 1	Next state
ACTIVE	1	x	0	x	SYSTEM
ACTIVE	1	x	1	x	ACTIVE

Note 1 In this table, “Freeze” represents the result of the comparison retry count = 0.

The following events will reset the retry counter and release the state machine from the freeze state:

- De-assertion of all blocked level-sensitive wakeup conditions
- Entry to the RESET mode (over-temperature error, nRESETREQ or long press of nONKEY)
- Entry to the RTC mode (system supply error)

The freeze operation is illustrated in [Figure 21](#). Once the freeze state is cleared, DA9062 continues operating normally. The freeze function can be enabled in the FREEZE_EN register and the number of retries triggering the freeze can be configured in NFREEZE.

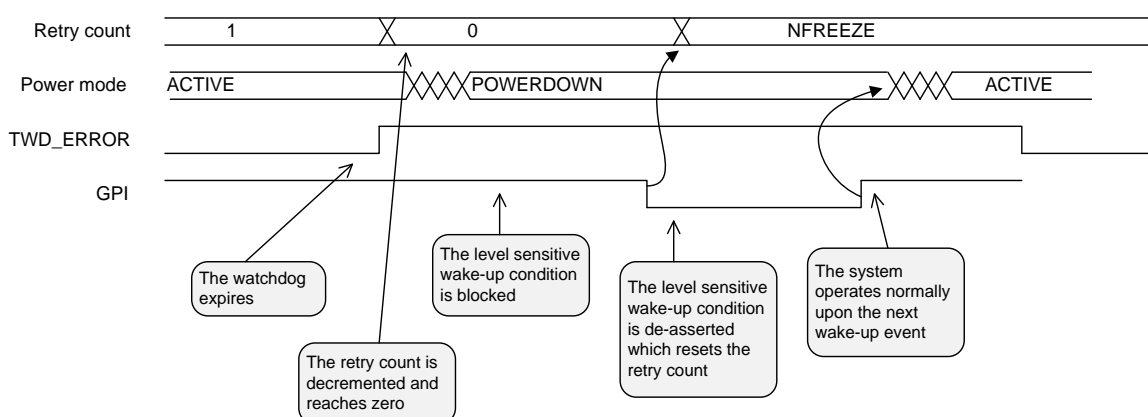


Figure 21: Freeze function

7.8.5 Power-up, power-down, and shutdown sequences

The power-up, power-down, and shutdown sequences, see [Figure 20](#), are handled by the power supply sequencer, see [Section 7.9](#). All power-up sequences are identical, and the power-down sequences mirror the power-up sequences.

The shutdown sequences are also identical to the power-down sequence, but after reaching POWERDOWN mode, the state machine automatically proceeds to RESET mode. The shutdown sequences caused by an internal error or nRESETREQ can be sped up from the INT_SD_MODE and HOST_SD_MODE controls: see [Section 7.8.3](#).

7.8.6 ACTIVE mode

In the ACTIVE mode, all supplies and functions are active. The transition from POWERDOWN to ACTIVE mode is handled by the programmable sequencer. DA9062 enters ACTIVE mode after the sequence has completed and the watchdog is enabled (if configured to use watchdog).

Status information can be read from the host processor via the 2-wire interface and DA9062 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ).

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7.9 Power supply sequencer

DA9062 features a programmable power sequencer that handles the system power-up, power-down, and shutdown sequences. The sequencer has a step-up counter, a timer that controls the step period, and a set of comparators that trigger power-on/off events at specific steps of the counter. The structure of the sequencer is depicted in Figure 22.

The sequencer is composed of 16 steps, and the step time can be programmed between 32 μs and 8.192 ms. The sequencer will step until it reaches a programmable maximum value (MAX_COUNT), whereupon an interrupt is issued. At each step, the sequencer will enable all the functions that are pointing to that particular step.

The power-up and -down sequences cannot be configured separately. When DA9062 is powering down, the sequencer will execute whatever was configured for the power-up sequence but in reverse order. Supplies can also be configured to stay on in POWERDOWN mode. In this case, the sequencer does not disable the regulator but switches to its B-configuration, see Section 7.4.

If any pointer is programmed to a step higher than MAX_COUNT, the function is no longer controlled by the sequencer. Only the regulator control pointers (LDO<x>_STEP, BUCK<x>_STEP) are allowed to point to step 0. Setting any other pointer to step 0, effectively disables that function.

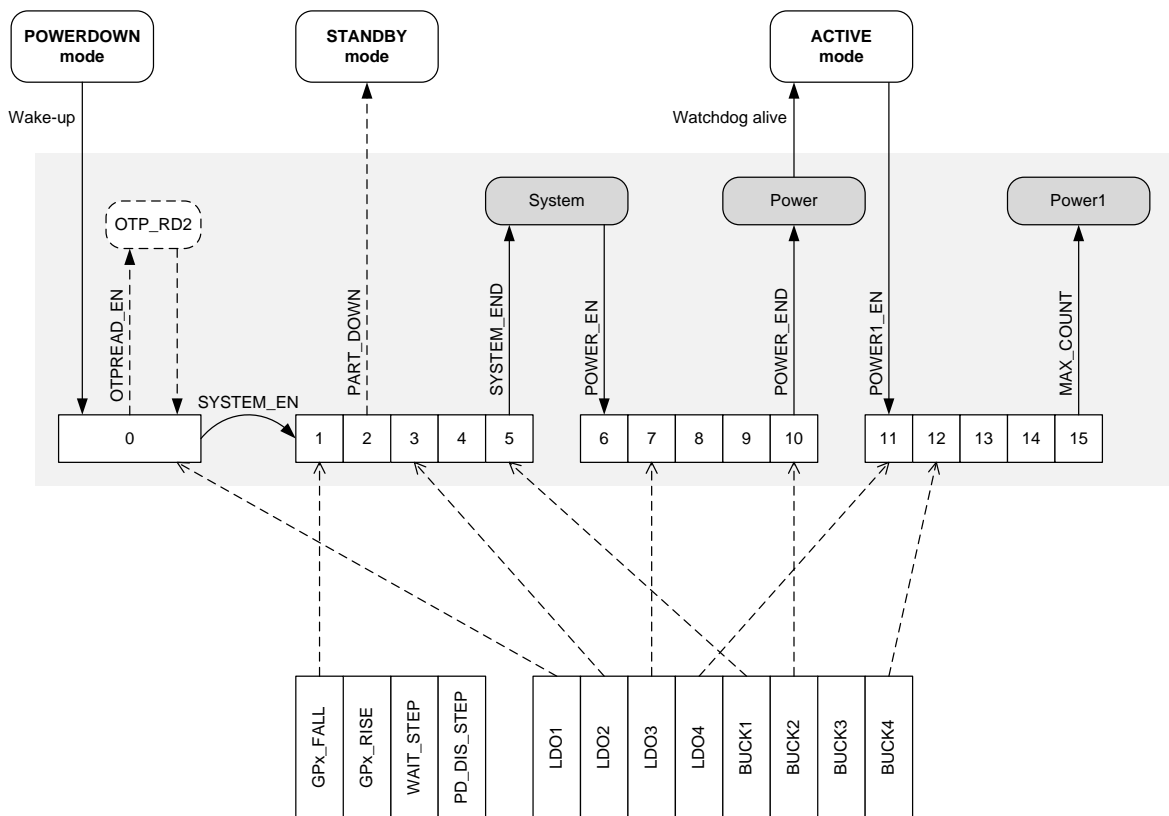


Figure 22: Structure of the power sequencer

NOTE
 STANDBY mode can only be reached on power-down, not power-up.

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7.9.1 Sub-sequences

As illustrated in [Figure 22](#), the sequencer is partitioned into three sub-sequences. These three sub-sequences can be used to define three power modes for the target application and to move between them in a controlled sequence as a response to control signals or register writes.

The first sub-sequence starts from step 0 and ends at a step defined by the SYSTEM_END pointer. After the power-up is triggered, DA9062 performs a partial OTP read (OTP_RD2) if OTPREAD_EN is set. It then waits for SYSTEM_EN to trigger the first sub-sequence. If SYSTEM_EN is already set in the OTP the first sub-sequence starts automatically after the power-up trigger. Alternatively, SYSTEM_EN can be asserted through the SYS_EN input. When the sequencer reaches the SYSTEM_END step the first sub-sequence is completed and the sequencer starts waiting for POWER_EN to trigger the second sub-sequence. If POWER_EN is already set in the OTP, the sequencer does not stop after the first sub-sequence. Alternatively, POWER_EN can be asserted through the PWR_EN input or via a register access.

The second sub-sequence starts from the step following SYSTEM_END and stops at a step defined by the POWER_END pointer. When the sequencer reaches the POWER_END step (and the watchdog is active), DA9062 enters ACTIVE mode. The final sub-sequence is triggered by asserting POWER1_EN via a register write. The third sub-sequence starts from the step following POWER_END and stops at a step defined by the MAX_COUNT pointer. If MAX_COUNT points to an earlier step than SYSTEM_END or POWER_END the remaining steps of the sequencer are disabled.

The power-down sequences are executed in reverse order to the power-up sequences. If the power-down sequence is triggered from the ACTIVE mode by de-asserting POWER_EN, the sequencer stops after reversing to the SYSTEM_END step. However, if the power-down sequence is triggered by de-asserting SYSTEM_EN, the sequencer does not stop and reverses back to step 0. Furthermore, if the power-down sequence is triggered by a watchdog timeout, the sequencer reverses to step 0 immediately.

A partial power-down can be achieved by setting STANDBY. This makes the sequencer stop at the step pointed to by the PART_DOWN pointer. The next power-up will then start from the PART_DOWN step, instead of step 0. The PART_DOWN pointer has to point to a step smaller than the SYSTEM_END pointer.

7.9.2 Regulator control

Each of DA9062's buck converters and LDOs can be assigned to any of the sequencer steps. In general, when the sequencer reaches a step to which a regulator is assigned, that regulator is enabled by the sequencer. Likewise, when the sequencer reaches the same step on the way down, the regulator is disabled. Multiple supplies can point to the same counter step, however, enabling multiple regulators in the same slot can lead to increased in-rush currents.

In the simplest scheme, the sequencer enables regulators during a power-up, and disables them during a power-down. This functionality is achieved by setting BUCK<x>_AUTO/LDO<x>_AUTO and clearing BUCK<x>_CONF/LDO<x>_CONF. Alternatively, the sequencer can be configured to keep the regulator enabled, but switch between the A and B settings in ACTIVE and POWERDOWN modes. The functionality of the BUCK<x>_AUTO/LDO<x>_AUTO and BUCK<x>_CONF/LDO<x>_CONF controls is summarised in [Table 27](#).

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Table 27: Regulator control functionality of the power supply sequencer

Power-up (sequencer direction up)						
AUTO	CONF	POWERDOWN mode (before)		ACTIVE mode (after)		Sequencer functionality
		EN	SEL	EN	SEL	
0	0	x	x	0	0	The regulator is disabled at the step pointed to by BUCK<x>_STEP/LDO<x>_STEP and the A-setting (VBUCK<x>_A/VLDO<x>_A) is activated.
x	1	x	x	1	0	The regulator is enabled at the step pointed to by BUCK<x>_STEP/LDO<x>_STEP and the A-setting (VBUCK<x>_A/VLDO<x>_A) is activated.
1	x	x	x	1	0	
Power-down (sequencer direction down)						
AUTO	CONF	ACTIVE mode (before)		POWERDOWN mode (after)		
		EN	SEL	EN	SEL	
x	0	x	x	0	0	The regulator is disabled at the step pointed to by BUCK<x>_STEP/LDO<x>_STEP and the A-setting (VBUCK<x>_A/VLDO<x>_A) is activated.
x	1	x	x	1	1	The regulator stays enabled but it is switched to the B-setting (VBUCK<x>_B/VLDO<x>_B).

Step 0 of the sequencer has a special meaning. If DEF_SUPPLY is set, the sequencer treats all regulators pointing to step 0 as default supplies. This means that the regulators are enabled automatically when entering the POWERDOWN mode. Regulators assigned to other steps are only enabled after a wakeup condition occurs. Apart from this, step 0 acts the same as steps 1 to 15. If DEF_SUPPLY is '0', step 0 of the sequencer does not have any affect.

As mentioned in Section 7.6.1, LDO1 can be programmed as an always-on supply. This is achieved by setting DEF_SUPPLY, LDO1_CONF, and LDO1_EN in the OTP. In normal operation, when the sequencer moves between ACTIVE and POWERDOWN modes, LDO1 behaves as presented in Table 27. However, if DA9062 moves to the RESET mode, this configuration keeps LDO1 enabled. This is not the case for any other regulator.

7.9.3 GPO control

Any GPO can be asserted or de-asserted in a sequencer step (GP_RISE<x>_STEP, GP_FALL<x>_STEP). The GPO control is summarised in Table 28. If a GPO is controlled by the sequencer, it is driven to its inactive state when DA9062 is in RESET mode. The GPIO control only works in sequencer steps greater than zero.

Table 28: GPO control functionality of the power supply sequencer

GPIO<x>_MODE	GPO state after reset	Sequencer direction	Previous GPO state	GPO transition at GP_RISE<x>	GPO transition at GP_FALL<x>
0 (active low)	High	Up	High	High to low	-
			Low	-	Low to high
		Down	High	-	High to low
			Low	Low to high	-
1 (active high)	Low	Up	High	-	High to low
			Low	Low to high	-
		Down	High	High to low	-
			Low	-	Low to high

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7.9.4 Wait step

One of the sequencer steps (any step greater than zero) can be configured as a wait step, in which the sequencer stays until an event is detected in the GPI3 input, see Section 7.3.1.2.

NOTE

The E_GPI3 event has to be cleared after the power-up sequence completes. Otherwise, the wait step in the next power-up sequence will be ineffective.

The wait step features an optional 500 ms timeout, which can be used when the wait event never occurs. If the timeout occurs, the steps following the wait step are not executed and a shutdown sequence to RESET mode is triggered. The shutdown reason is signalled with the WAIT_SHUT bit. Alternatively, the wait step can be used as a configurable delay in the sequence (WAIT_MODE, WAIT_TIME).

7.9.5 32 kHz clock output

If a GPO is used as a 32 kHz clock output see Section 7.3.2.2, the clock buffer can be enabled/disabled in one of the sequencer steps (any step greater than zero). The clock buffer is enabled when, during power-up, the sequencer reaches the step EN32K_STEP. Likewise, the buffer is disabled when the sequencer reaches the step EN32K_STEP on the way down.

7.9.6 Power-down disable

The PD_DIS_STEP pointer can be used to define a step in the power-up sequence above which a group of functions will be enabled. The functions concerned can be controlled in the PD_DIS register. Similarly, in the power-down sequence, the same groups of functions will be disabled when the sequencer proceeds below the PD_DIS_STEP.

7.10 Junction temperature supervision

To protect DA9062 from damage due to excessive power dissipation, the junction temperature is continuously monitored. The monitoring is split into three temperature ranges TEMP_WARN (125 °C), TEMP_CRIT (140 °C), and TEMP_POR (150 °C).

If the junction temperature rises above the first threshold (TEMP_WARN), the event E_TEMP is asserted. If the event is not masked, this will issue an interrupt. This first level of temperature supervision is intended for non-invasive temperature control, where the necessary measures for cooling the system down are left to the host software.

If the junction temperature increases even further and crosses the second threshold (TEMP_CRIT) a temperature error flag is issued and a shutdown sequence to RESET mode is triggered, see Section 7.8.3. The nRESET output is asserted at the beginning of the shutdown sequence. Therefore, the second level of the temperature supervision does not rely on the host software to take counter-measures. The fault flag can be evaluated by the application after the next power up.

There is also a third temperature threshold (TEMP_POR) which causes DA9062 to enter RESET mode without any sequencing and stop all functions except the RTC. This prevents possible permanent damage due to fast temperature increases.

7.11 System supply voltage supervision

Two comparators supervise the system supply V_{SYS} . One is monitoring the undervoltage level (VDD_FAULT_LOWER) and the other is indicating a good system supply (VDD_FAULT_UPPER). The VDD_FAULT_LOWER threshold is OTP configurable and can be set via the VDD_FAULT_ADJ control from 2.5 to 3.25 V in 50 mV steps. The VDD_FAULT_UPPER level is also OTP configurable and can be set via the VDD_HYST_ADJ control from 100 to 450 mV higher than the VDD_FAULT_LOWER threshold.

The high-to-low transition of the VDD_FAULT_UPPER signal asserts the event E_VDD_WARN. If the event is not masked, this will issue an interrupt, which can be used by the host processor as an

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indication to decrease its activity. The status can also be signalled with a dedicated nVDD_FAULT signal, see Section 7.3.2.1.

If V_{SYS} drops below VDD_FAULT_LOWER, the error flag VDD_FAULT is asserted and a shutdown sequence to RESET mode is triggered, see Section 7.8.3. The nRESET output is asserted at the beginning of the shutdown sequence.

7.12 Backup battery charger

The backup battery charger is designed to charge lithium-manganese coin cell batteries and super capacitors. The charger provides a constant charge current with a programmable target voltage. The charging current is programmable from 100 to 1000 μ A in 100 μ A steps and from 1 to 6 mA in 1 mA steps. End-of-charge termination voltage is programmable in 100/200 mV steps from 1.1 to 3.1 V. When enabled, the charger will always keep the backup battery charged at its target voltage. The backup battery charger can be temporarily disabled in POWERDOWN mode via register PD_DIS.

The backup battery charger includes a reverse current protection and can also be used as an always-on supply for low-power rails.

The backup battery provides an internal supply voltage for the 32 kHz crystal oscillator and RTC.

7.13 Real-time clock (RTC)

The RTC provides a real-time clock and alarm function that can be supplied from the backup battery. RTC mode is described in Section 7.8.2.

The RTC counter will count the number of 32 kHz clock periods, providing a seconds, minutes, hours, days, months, and years output. Year 0 corresponds to 2000. It is able to count up to 63 years. The value of the RTC calendar is read- and writeable via the 2-wire interface. A read of COUNT_S (seconds) saves the current RTC calendar count into registers COUNT_S to COUNT_Y. Registers are only valid when the RTC_READ status bit is asserted (assertion may take several ms from leaving POR). After MONITOR has been set, host writing to CRYSTAL and RTC_EN is prohibited to ensure that the RTC registers SECOND_A to SECOND_D are never stopped.

There is an alarm register containing min, hrs, day, month, and year. When the RTC counter register value corresponds to the value set in the alarm an interrupt and a wakeup event are generated. The trigger will also set a bit in an event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic tick signal that, depending on control TICK_TYPE, is either asserted every second or minute. After modifying TICK_TYPE or TICK_WAKE, a write to register ALARM_Y is required to activate the new settings.

The power manager controls, ALARM_ON and TICK_ON, enable/disable the alarm/tick.

The power manager register bit MONITOR is set to 0 each time the RTC is powered up. Software sets this bit to '1' when setting the time and date, which allows detection of a subsequent loss of the clock. Values written to the RTC calendar and alarm registers have to comply with the allowed value range (see register description, for example, less than 60 for seconds or minutes).

7.13.1 32 kHz crystal oscillator

The oscillator is used to drive the real time clock (RTC) counter. It works with an external piezoelectric oscillator crystal at 32 kHz. The oscillator output can be fed to a GPIO and used as a clock source in the platform. The buffer can be enabled/disabled from a control register or with the power sequencer.

In order to achieve the desired crystal frequency an external capacitor (10 to 20 pF, depending on the parasitic capacitance of the board) is connected to ground from each of the crystal pins. The start-up time of the oscillator is typically between 0.5 and 1 second over the voltage range. When the crystal is not mounted, the XTAL pins should be grounded.

The oscillator can be enabled from control CRYSTAL. A stabilisation timer can be used to blank the clock output during the start-up. The timer can be started simultaneously with the oscillator or it can be configured to wait until the clock's duty cycle is within the range 30 to 70 %. The start is configured from the DELAY_MODE control and the stabilisation time is programmed in the

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STABILISATION_TIME control. OUT_CLOCK controls whether the clock feed to the OUT_32K output (GPIO) is affected by the stabilisation timer. The RTC_CLOCK control provides a similar gating function for the clock feed to the internal RTC counter.

The clock feed to the OUT_32K output can be controlled with the power sequencer, as described in Section 7.9.5. In addition, the clock output is one of the features that can be disabled in the POWERDOWN mode, as described in Section 7.9.6. When the OUT32K_PAUSE control is set, the clock output is disabled in POWERDOWN.

7.14 Internal oscillator

An internal oscillator provides a nominal 6.0 MHz clock that is divided to 3.0 MHz for the buck converters. The frequency of the internal oscillator is adjusted during the initial start-up sequence of DA9062 to within 5 % of the nominal 6.0 MHz. It can be further adjusted (± 10 %) via a control OSC_FRQ. The tolerance of this frequency will affect most absolute timer values and PWM repetition rates.

7.15 Watchdog

The watchdog provides system monitoring functionality. A watchdog timeout triggers shutdown to POWERDOWN mode, signalled in register FAULT_LOG. The watchdog can also be configured to control a secondary reset output in addition to nRESET. This requires that one of the GPIOs is configured as a GPO, controlled by the sequencer. The assertion/de-assertion is used as a reset, and the GPIO is configured as a sequencer controlled GPO. This way, after the watchdog triggers the power-down, the reset output is asserted by the sequencer during the power-down sequence.

Once enabled, the watchdog cannot be stopped and it runs in ACTIVE mode (this feature can be bypassed with an OTP configuration). The source clock of the watchdog is automatically chosen between the 32 kHz clock generated from the crystal oscillator and an internally generated slow frequency clock.

After a cold boot, the watchdog is activated when entering ACTIVE mode. This first watchdog kick is required for DA9062 to move to the ACTIVE mode after a cold boot, as illustrated in Figure 20. After the watchdog is activated, the host must kick the watchdog periodically within the watchdog period programmed with the TWDSCALE control. An interrupt can be generated to warn the host processor of the watchdog timeout. The time for the warning interrupt is half of the watchdog period.

The kick can be done by a register write to control WATCHDOG (reg. CONTROL_F) or with the WDKICK input. If the WDKICK input (pin GPIO0) is asserted constantly, the watchdog is virtually disabled as the counter is not incremented (WDG_MODE).

If the host processor fails to feed the watchdog, DA9062 will assert a fault bit and enter POWERDOWN mode. The watchdog timeout can also be configured to assert a reset output. This requires that one of the GPIOs is configured as a reset output and assigned to a power sequencer step, see Section 7.9.

After each watchdog timeout a retry counter is decremented. If the retry counter reaches zero, DA9062 will stay in POWERDOWN mode, as described in Section 7.8.4. The number of allowed retries can be programmed in the NFREEZE control.

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8 Register map

8.1 Register page control

The device register map is larger than the address range directly addressable from the host interface. The page control register provides the higher address bits and control for using the paging mechanism. There are several copies of this register, one per host interface. These copies are mirrored to addresses 0x080, 0x100 and 0x180.

8.2 Overview

Table 29 provides a summary of the registers. A description of each register is provided in [Appendix A](#).

Table 29: Register summary

Addr	Register	7	6	5	4	3	2	1	0	
Page Control										
0x000	PAGE_CON	REVERT	WRITE_MODE	PAGE						
Power Manager Control and Monitoring (except IRQs and events)										
0x001	STATUS_A						DVC_BUSY			NONKEY
0x002	STATUS_B				GPI4	GPI3	GPI2	GPI1	GPI0	
0x004	STATUS_D					LDO4_ILIM	LDO3_ILIM	LDO2_ILIM	LDO1_ILIM	
0x005	FAULT_LOG	WAIT_SHUT	NRESETREQ	KEY_RESET	TEMP_CRIT	VDD_START	VDD_FAULT	POR	TWD_ERROR	
IRQ Events										
0x006	EVENT_A	EVENTS_C		EVENTS_B	E_SEQ_RDY	E_WDG_WARN			E_ALARM	E_NONKEY
0x007	EVENT_B	E_VDD_WARN	E_DVC_RDY					E_LDO_LIM	E_TEMP	
0x008	EVENT_C				E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0	
IRQ Masks										
0x00A	IRQ_MASK_A				M_SEQ_RDY	M_WDG_WARN			M_ALARM	M_NONKEY
0x00B	IRQ_MASK_B	M_VDD_WARN	M_DVC_RDY					M_LDO_LIM	M_TEMP	
0x00C	IRQ_MASK_C				M_GPI4	M_GPI3	M_GPI2	M_GPI1	M_GPI0	
System control										
0x00E	CONTROL_A	M_POWER1_EN		M_POWER_EN	M_SYSTEM_EN	STANDBY	POWER1_EN	POWER_EN	SYSTEM_EN	
0x00F	CONTROL_B	BUCK_SLOWSTART	NFREEZE		NONKEY_LOCK	NRES_MODE	FREEZE_EN	WATCHDOG_PD		
0x010	CONTROL_C	DEF_SUPPLY	SLEW_RATE		OTPREAD_EN	AUTO_BOOT	DEBOUNCING			
0x011	CONTROL_D									TWDSCALE
0x012	CONTROL_E	V_LOCK					RTC_EN	RTC_MODE_SD	RTC_MODE_PD	
0x013	CONTROL_F						WAKE_UP	SHUTDOWN	WATCHDOG	
0x014	PD_DIS	PMCONT_DIS	OUT32K_PAUSE	BBAT_DIS	CLDR_PAUSE			PMIF_DIS	GPI_DIS	
GPIO control										
0x015	GPIO_0_1	GPIO1_WEN	GPIO1_TYPE	GPIO1_PIN		GPIO0_WEN	GPIO0_TYPE	GPIO0_PIN		
0x016	GPIO_2_3	GPIO3_WEN	GPIO3_TYPE	GPIO3_PIN		GPIO2_WEN	GPIO2_TYPE	GPIO2_PIN		
0x017	GPIO_4					GPIO4_WEN	GPIO4_TYPE	GPIO4_PIN		
0x01C	GPIO_WKUP_MODE				GPIO4_WKUP_MODE	GPIO3_WKUP_MODE	GPIO2_WKUP_MODE	GPIO1_WKUP_MODE	GPIO0_WKUP_MODE	
0x01D	GPIO_MODE0_4				GPIO4_MODE	GPIO3_MODE	GPIO2_MODE	GPIO1_MODE	GPIO0_MODE	
0x01E	GPIO_OUT0_2	GPIO2_OUT		GPIO1_OUT		GPIO0_OUT				
0x01F	GPIO_OUT3_4				GPIO4_OUT		GPIO3_OUT			
Power supply control										
0x020	BUCK2_CONT	VBUCK2_GPI					BUCK2_CONF	BUCK2_GPI	BUCK2_EN	
0x021	BUCK1_CONT	VBUCK1_GPI					BUCK1_CONF	BUCK1_GPI	BUCK1_EN	
0x022	BUCK4_CONT	VBUCK4_GPI					BUCK4_CONF	BUCK4_GPI	BUCK4_EN	
0x024	BUCK3_CONT	VBUCK3_GPI					BUCK3_CONF	BUCK3_GPI	BUCK3_EN	
0x026	LDO1_CONT	LDO1_CONF	VLDO1_GPI				LDO1_PD_DIS	LDO1_GPI	LDO1_EN	
0x027	LDO2_CONT	LDO2_CONF	VLDO2_GPI				LDO2_PD_DIS	LDO2_GPI	LDO2_EN	
0x028	LDO3_CONT	LDO3_CONF	VLDO3_GPI				LDO3_PD_DIS	LDO3_GPI	LDO3_EN	
0x029	LDO4_CONT	LDO4_CONF	VLDO4_GPI				LDO4_PD_DIS	LDO4_GPI	LDO4_EN	
0x032	DVC_1	VLDO4_SEL	VLDO3_SEL	VLDO2_SEL	VLDO1_SEL	VBUCK3_SEL	VBUCK4_SEL	VBUCK2_SEL	VBUCK1_SEL	
RTC calendar and alarm										
0x040	COUNT_S	RTC_READ			COUNT_SEC					

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Addr	Register	7	6	5	4	3	2	1	0
0x041	COUNT_MI			COUNT_MIN					
0x042	COUNT_H				COUNT_HOUR				
0x043	COUNT_D				COUNT_DAY				
0x044	COUNT_MO					COUNT_MONTH			
0x045	COUNT_Y		MONITOR	COUNT_YEAR					
0x046	ALARM_S	ALARM_STATUS		ALARM_SEC					
0x047	ALARM_MI			ALARM_MIN					
0x048	ALARM_H				ALARM_HOUR				
0x049	ALARM_D				ALARM_DAY				
0x04A	ALARM_MO			TICK_WAKE	TICK_TYPE	ALARM_MONTH			
0x04B	ALARM_Y	TICK_ON	ALARM_ON	ALARM_YEAR					
0x04C	SECOND_A	SECONDS_A							
0x04D	SECOND_B	SECONDS_B							
0x04E	SECOND_C	SECONDS_C							
0x04F	SECOND_D	SECONDS_D							
Power Sequencer									
0x081	SEQ	NXT_SEQ_START				SEQ_POINTER			
0x082	SEQ_TIMER	SEQ_DUMMY				SEQ_TIME			
0x083	ID_2_1	LDO2_STEP				LDO1_STEP			
0x084	ID_4_3	LDO4_STEP				LDO3_STEP			
0x088	ID_12_11	PD_DIS_STEP							
0x089	ID_14_13	BUCK2_STEP				BUCK1_STEP			
0x08A	ID_16_15	BUCK3_STEP				BUCK4_STEP			
0x08D	ID_22_21	GP_FALL1_STEP				GP_RISE1_STEP			
0x08E	ID_24_23	GP_FALL2_STEP				GP_RISE2_STEP			
0x08F	ID_26_25	GP_FALL3_STEP				GP_RISE3_STEP			
0x090	ID_28_27	GP_FALL4_STEP				GP_RISE4_STEP			
0x091	ID_30_29	GP_FALL5_STEP				GP_RISE5_STEP			
0x092	ID_32_31	EN32K_STEP				WAIT_STEP			
0x095	SEQ_A	POWER_END				SYSTEM_END			
0x096	SEQ_B	PART_DOWN				MAX_COUNT			
0x097	WAIT	WAIT_DIR		TIME_OUT	WAIT_MODE	WAIT_TIME			
0x098	EN_32K	EN_32KOUT		OUT_CLOCK	DELAY_MODE	CRYSTAL	STABILISATION_TIME		
0x099	RESET	RESET_EVENT		RESET_TIMER					
Power supply control									
0x09A	BUCK_ILIM_A					BUCK3_ILIM			
0x09B	BUCK_ILIM_B					BUCK4_ILIM			
0x09C	BUCK_ILIM_C	BUCK2_ILIM				BUCK1_ILIM			
0x09D	BUCK2_CFG	BUCK2_MODE		BUCK2_PD_DIS					
0x09E	BUCK1_CFG	BUCK1_MODE		BUCK1_PD_DIS					
0x09F	BUCK4_CFG	BUCK4_MODE		BUCK4_PD_DIS	BUCK4_VTT_EN	BUCK4_VTTR_EN			
0x0A0	BUCK3_CFG	BUCK3_MODE		BUCK3_PD_DIS					
0x0A3	VBUCK2_A	BUCK2_SL_A	VBUCK2_A						
0x0A4	VBUCK1_A	BUCK1_SL_A	VBUCK1_A						
0x0A5	VBUCK4_A	BUCK4_SL_A	VBUCK4_A						
0x0A7	VBUCK3_A	BUCK3_SL_A	VBUCK3_A						
0x0A9	VLDO1_A	LDO1_SL_A		VLDO1_A					
0x0AA	VLDO2_A	LDO2_SL_A		VLDO2_A					
0x0AB	VLDO3_A	LDO3_SL_A		VLDO3_A					
0x0AC	VLDO4_A	LDO4_SL_A		VLDO4_A					
0x0B4	VBUCK2_B	BUCK2_SL_B	VBUCK2_B						
0x0B5	VBUCK1_B	BUCK1_SL_B	VBUCK1_B						
0x0B6	VBUCK4_B	BUCK4_SL_B	VBUCK4_B						
0x0B8	VBUCK3_B	BUCK3_SL_B	VBUCK3_B						
0x0BA	VLDO1_B	LDO1_SL_B		VLDO1_B					
0x0BB	VLDO2_B	LDO2_SL_B		VLDO2_B					
0x0BC	VLDO3_B	LDO3_SL_B		VLDO3_B					
0x0BD	VLDO4_B	LDO4_SL_B		VLDO4_B					
BBAT charger control									
0x0C5	BBAT_CONT	BCHG_ISET				BCHG_VSET			

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Addr	Register	7	6	5	4	3	2	1	0	
Customer Trim and Configuration										
0x105	INTERFACE	IF_BASE_ADDR								
0x106	CONFIG_A		PM_IF_HSM	PM_IF_FMP	PM_IF_V	IRQ_TYPE	PM_O_TYPE		PM_I_V	
0x107	CONFIG_B		VDD_HYST_ADJ		VDD_FAULT_ADJ					
0x108	CONFIG_C		BUCK3_CLK_INV		BUCK4_CLK_INV	BUCK1_CLK_INV	BUCK_ACTV_DISC HRG			
0x109	CONFIG_D		FORCE_RESET					SYSTEM_EN_RD	NIRQ_MODE	GPI_V
0x10A	CONFIG_E				BUCK3_AUTO		BUCK4_AUTO	BUCK2_AUTO	BUCK1_AUTO	
0x10C	CONFIG_G					LDO4_AUTO	LDO3_AUTO	LDO2_AUTO	LDO1_AUTO	
0x10D	CONFIG_H		BUCK1_FCM	BUCK2_FCM		BUCK_MERGE				
0x10E	CONFIG_I	LDO_SD	INT_SD_MODE	HOST_SD_MODE	KEY_SD_MODE	WATCHDOG_SD	nONKEY_SD	NONKEY_PIN		
0x10F	CONFIG_J	IF_RESET	TWOWIRE_TO	RESET_DURATION		SHUT_DELAY		KEY_DELAY		
0x110	CONFIG_K				GPIO4_PUPD	GPIO3_PUPD	GPIO2_PUPD	GPIO1_PUPD	GPIO0_PUPD	
0x112	CONFIG_M	OSC_FRQ				WDG_MODE		NRESETREQ_PU		
Customer device specific										
0x121	GP_ID_0	GP_0								
0x122	GP_ID_1	GP_1								
0x123	GP_ID_2	GP_2								
0x124	GP_ID_3	GP_3								
0x125	GP_ID_4	GP_4								
0x126	GP_ID_5	GP_5								
0x127	GP_ID_6	GP_6								
0x128	GP_ID_7	GP_7								
0x129	GP_ID_8	GP_8								
0x12A	GP_ID_9	GP_9								
0x12B	GP_ID_10	GP_10								
0x12C	GP_ID_11	GP_11								
0x12D	GP_ID_12	GP_12								
0x12E	GP_ID_13	GP_13								
0x12F	GP_ID_14	GP_14								
0x130	GP_ID_15	GP_15								
0x131	GP_ID_16	GP_16								
0x132	GP_ID_17	GP_17								
0x133	GP_ID_18	GP_18								
0x134	GP_ID_19	GP_19								
0x181	DEVICE_ID	DEV_ID								
0x182	VARIANT_ID	MRC				VRC				
0x183	CUSTOMER_ID	CUST_ID								
0x184	CONFIG_ID	CONFIG_REV								

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9 Application information

9.1 Component selection

The following recommended components are examples selected from requirements of a typical application. The final component selection will be dependent on the specific application. The electrical characteristics (for example, supported voltage/current range) have to be cross-checked and component types may need to be adapted from the individual needs of the target circuitry.

9.1.1 Resistors

Table 30: Recommended resistors

Pin	Value	Tol.	Size (mm)	Rating (mW)	Part
IREF	200 k Ω	$\pm 1\%$	1005	100	Panasonic ERJ2RKF2003x

9.1.2 Capacitors

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially ones with high capacitance and small size, the DC bias characteristic has to be taken into account.

On the VSYS main supply rail, a minimum distributed capacitance of 40 μF (actual capacitance after voltage and temperature derating) is required.

Buck input capacitors should be within 1.5 mm distance from the supply pin, and the output capacitor should be close to the inductor.

Table 31: Recommended capacitors

Pin	Value	Tol.	Size (mm)	Height (mm)	Temp. char.	Rating (V)	Part
VLDO1	1 μF	$\pm 10\%$	1005	0.55	X5R	10	GRM155R61A105KE15
VLDOx	2.2 μF	$\pm 20\%$	1005	0.55	X5R	10	GRM155R60J225ME95#
VBUCK3 $I_{\text{OUT}} \leq 1.5 \text{ A}$	2 x 22 μF	$\pm 20\%$	2012	0.95	X5R	6.3	GRM219R60J226M***
		$\pm 20\%$	1005	0.5	X5R	4.0	CL05A226MR5NZNC
VBUCK3 $I_{\text{OUT}} > 1.5 \text{ A}$	2 x 47 μF	$\pm 20\%$	2012	0.95	X5R	4.0	GRM219R60G476M***
		$\pm 20\%$	1608	0.8	X5R	4.0	CL10A476MR8NZN
VBUCK4	2 x 22 μF	$\pm 20\%$	1608	1	X5R	6.3	GRM188R60J226MEA0
		$\pm 20\%$	1005	0.5	X5R	4.0	CL05A226MR5NZNC
VBUCK4 (VTT mode)	2 x 47 μF	$\pm 20\%$	2012	0.95	X5R	4.0	GRM219R60G476M***61
		$\pm 20\%$	1608	0.8	X5R	4.0	CL10A476MR8NZN
VBUCK1, VBUCK2 (half-current mode)	2 x 22 μF	$\pm 20\%$	1608	1	X5R	6.3	GRM188R60J226MEA0
		$\pm 20\%$	1005	0.5	X5R	4.0	CL05A226MR5NZNC
VBUCK1, VBUCK2 (full-current mode)	2 x 47 μF	$\pm 20\%$	2012	0.95	X5R	4.0	GRM219R60G476M***61
		$\pm 20\%$	1608	0.8	X5R	4.0	CL10A476MR8NZN
VSYS	1 x 1 μF	$\pm 10\%$	1005	0.5	X5R	10	GRM155R61A105KE15D
VDD_BUCKx	2 x 22 μF	$\pm 20\%$	2012	1.25	X5R	10	LMK212BJ226MG-T
	4 x 10 μF	$\pm 20\%$	1005	0.5	X5R	10	GRM155R61A106ME21

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Pin	Value	Tol.	Size (mm)	Height (mm)	Temp. char.	Rating (V)	Part
VDD_LDO2	1 x 1 μ F	\pm 10%	1005	0.5	X5R	10	GRM155R61A105KE15D
VDD_LDO34	1 x 1 μ F	\pm 10%	1005	0.5	X5R	10	GRM155R61A105KE15D
VBBAT	470 nF	\pm 10%	1005	0.55	X5R	10	GRM155R61A474KE15#
VDDCORE, VREF	2.2 μ F	\pm 20%	1005	0.55	X5R	6.3	GRM155R60J225ME95#
XTAL_IN, XTAL_OUT	12 pF	\pm 5%	1005	0.55	U2J	50	GRM1557U1H120JZ01#

9.1.3 Inductors

Inductors should be selected based upon the following parameters:

- ISAT specifies the current causing a reduction in the inductance by a specific amount, typically 30 %
- IRMS specifies the current causing a temperature rise of a specific amount
- DC resistance (DCR) is critical for converter efficiency and should be therefore minimised.
- ESR at the buck switching frequency is critical to converter efficiency in PFM mode and should be therefore minimised.

Inductance is given in [Table 32](#).

Table 32: Recommended inductors

Buck	Value	ISAT (A)	IRMS (A)	DCR (typ. m Ω)	Size (WxLxH mm)	Part
Buck1 and Buck2 (half-current mode), Buck3, Buck4	1 μ H	2.7	2.3	55	2.0x1.6x1.0	Toko 1285AS-H-1R0N
		2.65	2.45	60	2.0x1.6x1.0	Tayo Yuden MAKK2016T1R0M
		2.9	2.2	60	2.0x1.6x1.0	TDK TFM201610A-1R0M
Buck4 (VTT mode)	0.24 μ H	1.65	2.3	43	1.6x0.8x1.0	Taiyo Yuden MBKK1608TR24N
		9.7	11.45	7.64	4.0x4.0x1.2	Coilcraft XFL4012-251ME
Buck1, Buck2 (full-current mode)	1 μ H	3.4	3	60	2.5x2.0x1.0	Toko1269AS-H-1R0N
		3.6	3.1	45	2.5x2.0x1.2	Tayo Yuden MAMK2520T1R0M
		3.8	3.5	45	2.5x2.0x1.2	Toko 1239AS-H-1R0N
		3.9	3.1	48	3.2x2.5x1.0	Toko1276AS-H-1R0N
		3.5	2.5	54	2.5x2.0x1.0	TDK TFM252010A-1R0M
		3.35	2.5	52	3.0x3.0x1.2	Cyntec PST031B-1R0MS
	5.4	11	10.8	4.0x4.0x2.1	Coilcraft XFL4020-102ME	

9.1.4 Crystal

The real-time clock module requires an external 32.768 kHz crystal. For correct component selection, the effective load capacitance must be taken into account. This includes external capacitors on pins XTAL_IN and XTAL_OUT in series combination, plus the PCB and stray capacitances. For example, if two 12 pF external capacitors are used, resulting in a total capacitance of 6 pF, and assuming the stray capacitances are 3 pF, then a crystal that specifies a load capacitance of 9 pF

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should be chosen. Different stray capacitances may require different external capacitors and/or a different crystal type. Furthermore, the series resistance of the crystal must not exceed 100 kΩ.

Table 33: Recommended crystal

Type	Size (W×L×H mm)	Manufacturer
CC7V-T1A 32.768 kHz 9.0 pF ±30 ppm	3.2×1.5×0.9	Micro Crystal

9.1.5 Backup battery

The backup battery charger supports lithium coin cells as well as Supercaps/Goldcaps.

Table 34: Recommended backup battery

Type	Size (mm)	Manufacturer
Lithium battery (rechargeable) ML414, 1.0 mAh, 3.1 V	4.8 (∅), 1.4 (h)	Sanyo, Panasonic
Starcap SC SM 2R8, 0.1 F, 2.8 V	4.8 (∅), 1.4 (h)	Korchip
Electric double layer capacitor (Gold Capacitor) EECEP0E333A, 0.033 F, 2.6 V	3.8 (∅), 1.5 (h)	Panasonic

9.2 PCB layout

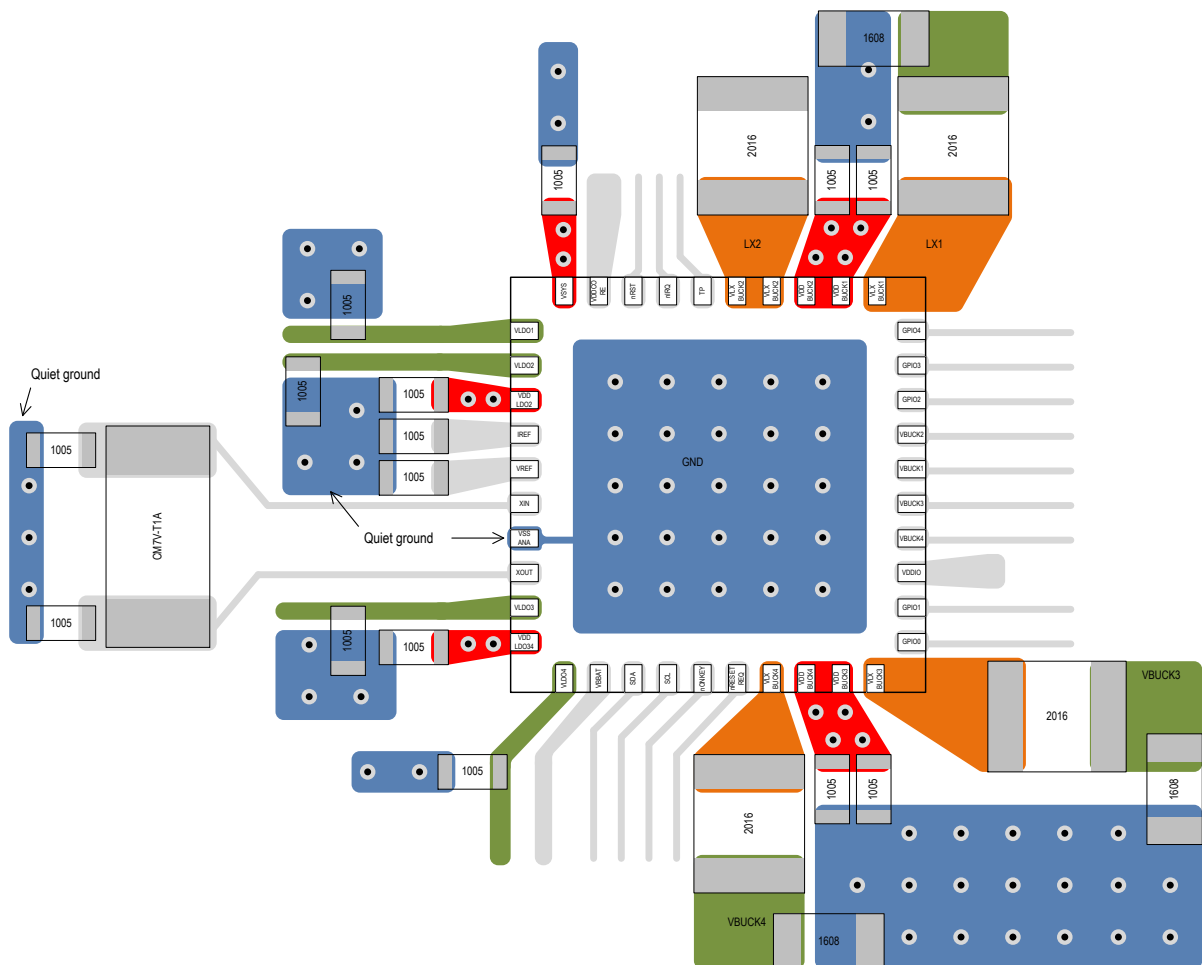


Figure 23: PCB layout for DA9062

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9.2.1 General recommendations

Appropriate trace width and quantity of vias should be used for all power supply paths.

Too high trace resistances can prevent the system from achieving the best performance, for example, the efficiency and the current ratings of switching converters might be degraded. Furthermore, the PCB may be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.

Special care must be taken with the DA9062 pad connections. The traces connecting the pads should be of the same width as the pads and they should become wider as soon as possible.

It is recommended to create a separate quiet ground to which the VREF capacitor, IREF resistor, and the crystal capacitors are connected. The PCB layout should ensure these component grounds are kept quiet, that is, they should be separated from the main ground return path for the noisy power ground. The quiet ground can then be connected to the main ground at the paddle, as shown in [Figure 23](#).

All traces carrying high discontinuous currents should be kept as short as possible.

Noise sensitive analog signals, such as feedback lines or crystal connections, should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation or shielding with quiet signals or ground traces.

9.2.2 LDOs and switched mode supplies

The placement of the distributed capacitors on the VSYS rail must ensure that all VDD inputs and VSYS are connected to a bypass capacitor close to the pad. It is recommended placing at least two 1 μ F capacitors close to the VDD_LDOx pads and at least one 10 μ F close to the VDD_BUCKx pads.

Using a local power plane underneath the device for VSYS might be considered.

Transient current loops in the area of the switching converters should be minimised.

The common references (IREF, VREF) should be placed close to the device and cross-coupling to any noisy digital or analog trace must be avoided.

Output capacitors of the LDOs can be placed close to the input pins of the supplied devices (remote from the DA9062).

Care must be taken with trace routing to ensure that no current is carried on feedback lines of the buck output voltages (VBUCKx).

The inductor placement is less critical since parasitic inductances have negligible effect.

9.2.3 32 kHz crystal oscillator

The crystal and its load capacitors should be placed as close as possible to the IC with short and symmetrical traces.

The traces must be isolated from noisy signals, especially from clocked digital ones. Ideally the lines should be buried between two ground layers, surrounded by additional ground traces.

9.2.4 Optimising thermal performance

DA9062 features a ground paddle which should be connected with as many vias as possible to the PCB's main ground plane in order to achieve good thermal performance.

Solder mask openings for the ball landing pads must be arranged to prohibit solder balls flowing into vias.

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10 Ordering information

The ordering number consists of the part number followed by a suffix indicating the packing method. The “xx” represents a placeholder for the specific OTP variant. For details and availability, please consult Dialog Semiconductor’s [customer portal](#) or your local sales representative.

Table 35: Ordering information

Part number	Package	Package description	Comment
DA9062-xxAM1	QFN40, 6 x 6 mm	Tray, 490 pcs	
DA9062-xxAM1-A	QFN40, 6 x 6 mm	Tray, 490 pcs	Automotive AEC-Q100 Grade 3
DA9062-xxAM2	QFN40, 6 x 6 mm	T&R, 4000 pcs	
DA9062-xxAM2-A	QFN40, 6 x 6 mm	T&R, 4000 pcs	Automotive AEC-Q100 Grade 3

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Appendix A Register descriptions

This appendix describes the registers summarised in Section 8.

A.1 PAGE 0

A.1.1 Page control

Table 36: PAGE_CON (0x000)

Field	Slice	Description	Reset
REVERT	7:7	0: PAGE switches the regmap page until rewritten. 1: PAGE reverts to 0 after one access.	0
WRITE_MODE	6:6	2-WIRE sequential write style. 0: Write data to consecutive addresses 1: Write data to random addresses using address/data pairs	0
PAGE	5:0	The top 6 bits of the register address. For 2-WIRE, PAGE[0] is ignored.	0x0

A.1.2 Power manager control and monitoring (except IRQs and events)

Table 37: STATUS_A (0x001)

Field	Slice	Description	Reset
<i>Reserved</i>	7:3	<i>Reserved</i>	
DVC_BUSY	2:2	One or more DVC capable supplies are ramping	0
<i>Reserved</i>	1:1	<i>Reserved</i>	
NONKEY	0:0		0

Table 38: STATUS_B (0x002)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
GPI4	4:4	GPI level	0
GPI3	3:3	GPI level	0
GPI2	2:2	GPI level	0
GPI1	1:1	GPI level	0
GPI0	0:0	GPI level	0

Table 39: STATUS_D (0x004)

Field	Slice	Description	Reset
<i>Reserved</i>	7:4	<i>Reserved</i>	
LDO4_ILIM	3:3	LDO over-current indicator	0
LDO3_ILIM	2:2	LDO over-current indicator	0
LDO2_ILIM	1:1	LDO over-current indicator	0
LDO1_ILIM	0:0	LDO over-current indicator	0

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Table 40: FAULT_LOG (0x005)

Field	Slice	Description	Reset
WAIT_SHUT	7:7	Power-down due to PSS WAIT slot timeout.	0
NRESETREQ	6:6	Power-down due to nRESETREQ or SHUTDOWN.	0
KEY_RESET	5:5	Power-down due to nONKEY.	0
TEMP_CRIT	4:4	Junction over-temperature	0
VDD_START	3:3	Power-down due to VSYS undervoltage before or within 16 sec after nRESET.	0
VDD_FAULT	2:2	Power-down due to VSYS undervoltage.	0
POR	1:1	DA9062 starts up from no power or RTC / DELIVERY mode.	1
TWD_ERROR	0:0	Watchdog timeout	0

A.1.3 IRQ events

Table 41: EVENT_A (0x006)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
EVENTS_C	6:6	Event in register EVENT_C is active.	0
EVENTS_B	5:5	Event in register EVENT_B is active.	0
E_SEQ_RDY	4:4	Sequencer reached final position.	0
E_WDG_WARN	3:3	Watchdog timeout warning	0
<i>Reserved</i>	2:2	<i>Reserved</i>	
E_ALARM	1:1	RTC Alarm	
E_NONKEY	0:0	nONKEY	0

Table 42: EVENT_B (0x007)

Field	Slice	Description	Reset
E_VDD_WARN	7:7	VSYS dropped below VDD_FAULT_UPPER threshold.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
E_DVC_RDY	5:5	All supplies have finished DVC ramping.	0
<i>Reserved</i>	4:4	<i>Reserved</i>	
E_LDO_LIM	3:3	Any LDO over-current	0
<i>Reserved</i>	2:2	<i>Reserved</i>	
E_TEMP	1:1	Junction over-temperature	0
<i>Reserved</i>	0:0	<i>Reserved</i>	

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Table 43: EVENT_C (0x008)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
E_GPI4	4:4	GPI event according to ACTIVE state setting	0
E_GPI3	3:3	GPI event according to ACTIVE state setting	0
E_GPI2	2:2	GPI event according to ACTIVE state setting	0
E_GPI1	1:1	GPI event according to ACTIVE state setting	0
E_GPI0	0:0	GPI event according to ACTIVE state setting	0

A.1.4 IRQ masks

Table 44: IRQ_MASK_A (0x00A)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
M_SEQ_RDY	4:4	Sequencer final position indication	0
M_WDG_WARN	3:3	Watchdog timeout warning	0
<i>Reserved</i>	2:2	<i>Reserved</i>	
M_ALARM	1:1	RTC Alarm	
M_NONKEY	0:0	nONKEY	0

Table 45: IRQ_MASK_B (0x00B)

Field	Slice	Description	Reset
M_VDD_WARN	7:7	VSYS dropped below VDD_FAULT_UPPER threshold.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
M_DVC_RDY	5:5	All supplies have finished DVC ramping.	0
<i>Reserved</i>	4:4	<i>Reserved</i>	
M_LDO_LIM	3:3	Any LDO over-current	0
<i>Reserved</i>	2:2	<i>Reserved</i>	
M_TEMP	1:1	Junction over-temperature	0
<i>Reserved</i>	0:0	<i>Reserved</i>	

Table 46: IRQ_MASK_C (0x00C)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
M_GPI4	4:4	GPI IRQ mask	0
M_GPI3	3:3	GPI IRQ mask	0
M_GPI2	2:2	GPI IRQ mask	0
M_GPI1	1:1	GPI IRQ mask	0
M_GPI0	0:0	GPI IRQ mask	0

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A.1.5 System control

Table 47: CONTROL_A (0x00E)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
M_POWER1_EN	6:6	Write mask for POWER1_EN	0
M_POWER_EN	5:5	Write mask for POWER_EN	0
M_SYSTEM_EN	4:4	Write mask for SYSTEM_EN	0
STANDBY	3:3	Clearing SYSTEM_EN / releasing SYS_EN or powering down domain SYSTEM by nONKEY will ... 0: ... completely power down to slot 0. 1: ... stop at PART_DOWN.	0
POWER1_EN	2:2	Target status of power domain POWER1. Bus write masked with M_POWER1_EN.	0
POWER_EN	1:1	Target status of power domain POWER. Bus write masked with M_POWER_EN.	0
SYSTEM_EN	0:0	Target status of power domain SYSTEM. Bus write masked with M_SYSTEM_EN.	0

Table 48: CONTROL_B (0x00F)

Field	Slice	Description	Reset
BUCK_SLOWSTART	7:7	Enable buck slow start (reduced inrush current; increased start-up time).	0
NFREEZE	6:5	Block all wakeups after NFREEZE watchdog restart trials.	00
nONKEY_LOCK	4:4	0: normal POWERDOWN mode 1: POWERDOWN controlled by KEY_DELAY	1
NRES_MODE	3:3	If powering down / up ... 0: ... keep nRESET not asserted. 1: ... assert / clear nRESET when entering / leaving POWERDOWN.	1
FREEZE_EN	2:2	Enable watchdog restart limit NFREEZE.	0
WATCHDOG_PD	1:1	Watchdog timer is on (1) / off (0) in POWERDOWN mode.	0
<i>Reserved</i>	0:0	<i>Reserved</i>	

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Table 49: CONTROL_C (0x010)

Field	Slice	Description	Reset
DEF_SUPPLY	7:7	1: OTP enables / disables all supplies (except LDOCORE) when PSS enters slot 0.	0
SLEW_RATE	6:5	Buck DVC slew rate step width [10 mV/step (20 mV/step for Buck3)] 0: 4 μ s 1: 2 μ s 2: 1 μ s 3: 0.5 μ s	10
OTPREAD_EN	4:4	When leaving POWERDOWN mode supplies are configured from OTP.	1
AUTO_BOOT	3:3	After progressing from RESET mode the PSS ... 0: ... requires a wakeup event to start-up. 1: ... starts up automatically.	0
DEBOUNCING	2:0	GPI, nONKEY and nRESETREQ debounce time 0: no debouncing 1: 0.1 ms 2: 1.0 ms 3: 10.24 ms 4: 51.2 ms 5: 256 ms 6: 512 ms 7: 1024 ms	011

Table 50: CONTROL_D (0x011)

Field	Slice	Description	Reset
<i>Reserved</i>	7:3	<i>Reserved</i>	
TWDSCALE	2:0	Watchdog timeout scaling 0: Watchdog disabled other: Timeout = $2.5 * 2^{(TWDSCALE-1)}$ s	000

Table 51: CONTROL_E (0x012)

Field	Slice	Description	Reset
V_LOCK	7:7	Prevent host from writing to registers 0x81 - 0x120 except 0x100.	0
<i>Reserved</i>	6:3	<i>Reserved</i>	
RTC_EN	2:2	Enable Real Time Clock and Alarm. Fetched from VDDRRTC domain at VDDCORE POR.	0
RTC_MODE_SD	1:1	Disable all supplies and blocks and LDOCORE if PSM enters RESET.	1
RTC_MODE_PD	0:0	Disable all supplies and blocks and LDOCORE if PSM enters POWERDOWN.	0

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Table 52: CONTROL_F (0x013)

Field	Slice	Description	Reset
<i>Reserved</i>	7:3	<i>Reserved</i>	
WAKE_UP	2:2	Wake-up from POWERDOWN mode. Cleared automatically.	0
SHUTDOWN	1:1	POWERDOWN to RESET mode. Cleared automatically.	0
WATCHDOG	0:0	Reset watchdog timer. Cleared automatically.	0

Table 53: PD_DIS (0x014)

Field	Slice	Description	Reset
PMCONT_DIS	7:7	Disable SYS_EN, PWR_EN and PWR1_EN in POWERDOWN mode.	0
OUT32K_PAUSE	6:6	Disable OUT32K pad in POWERDOWN mode.	0
BBAT_DIS	5:5	Disable backup battery charger in POWERDOWN mode.	0
CLDR_PAUSE	4:4	Disable calendar update in POWERDOWN mode.	0
<i>Reserved</i>	3:3	<i>Reserved</i>	
PMIF_DIS	2:2	Disable 2-WIRE interface in POWERDOWN mode.	0
<i>Reserved</i>	1:1	<i>Reserved</i>	
GPI_DIS	0:0	Disable E_GPIx events in POWERDOWN mode.	0

A.1.6 GPIO control

Table 54: GPIO_0_1 (0x015)

Field	Slice	Description	Reset
GPIO1_WEN	7:7	0: Passive-to-active transition triggers wakeup. 1: No wakeup	0
GPIO1_TYPE	6:6	GPI: active high (1) / low (0)	1
GPIO1_PIN	5:4	<i>Function of GPIO pad (see GPIO*_OUT if output)</i> 0: reserved (pad configured as analog IO) 1: input (opt. regul. HW ctrl.) 2: output (open drain) 3: output (push-pull)	01
GPIO0_WEN	3:3	0: Passive-to-active transition triggers wakeup. 1: No wakeup	0
GPIO0_TYPE	2:2	GPI: active high (1) / low (0)	1
GPIO0_PIN	1:0	<i>Function of GPIO pad (see GPIO*_OUT if output)</i> 0: Watchdog trigger input 1: input 2: output (open drain) 3: output (push-pull)	01

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Table 55: GPIO_2_3 (0x016)

Field	Slice	Description	Reset
GPIO3_WEN	7:7	0: Passive-to-active transition triggers wakeup. 1: No wakeup	0
GPIO3_TYPE	6:6	GPI: active high (1) / low (0)	1
GPIO3_PIN	5:4	Function of GPIO pad (see GPIO*_OUT if output) 0: reserved (pad configured as analog IO) 1: input (opt. regul. HW ctrl.) 2: output (open drain) 3: output (push-pull)	01
GPIO2_WEN	3:3	0: Passive-to-active transition triggers wakeup. 1: No wakeup	0
GPIO2_TYPE	2:2	GPI: active high (1) / low (0)	1
GPIO2_PIN	1:0	Function of GPIO pad (see GPIO*_OUT if output) 0: Sequencer control input 1: input (opt. regul. HW ctrl.) 2: output (open drain) 3: VDD_FAULT	01

Table 56: GPIO_4 (0x017)

Field	Slice	Description	Reset
<i>Reserved</i>	7:4	<i>Reserved</i>	
GPIO4_WEN	3:3	0: Passive-to-active transition triggers wakeup. 1: No wakeup	0
GPIO4_TYPE	2:2	GPI: active high (1) / low (0)	1
GPIO4_PIN	1:0	Function of GPIO pad (see GPIO*_OUT if output) 0: Sequencer control input 1: input 2: output (open drain) 3: output (push-pull)	01

Table 57: GPIO_WKUP_MODE (0x01C)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
GPIO4_WKUP_MODE	4:4	GPI wakeup is edge (0) / level (1) sensitive.	0
GPIO3_WKUP_MODE	3:3	GPI wakeup is edge (0) / level (1) sensitive.	0
GPIO2_WKUP_MODE	2:2	GPI wakeup is edge (0) / level (1) sensitive.	0
GPIO1_WKUP_MODE	1:1	GPI wakeup is edge (0) / level (1) sensitive.	0
GPIO0_WKUP_MODE	0:0	GPI wakeup is edge (0) / level (1) sensitive.	0

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Table 58: GPIO_MODE0_4 (0x01D)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
GPIO4_MODE	4:4	Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1)	0
GPIO3_MODE	3:3	Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1)	0
GPIO2_MODE	2:2	Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1)	0
GPIO1_MODE	1:1	Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1)	0
GPIO0_MODE	0:0	Output, STATIC: the output value Output, other: active low (0) / high (1) Input: debouncing off (0) / on (1)	0

Table 59: GPIO_OUT0_2 (0x01E)

Field	Slice	Description	Reset
GPIO2_OUT	7:6	GPIO output function 0: Static value according GPIO*_MODE 1: VDD_FAULT 2: 32 kHz crystal clock 3: Sequencer controlled	00
GPIO1_OUT	5:3	<i>GPIO output function</i> 0: <i>Static value according GPIO*_MODE</i> 1: <i>VDD_FAULT</i> 2: <i>32 kHz crystal clock</i> 3: <i>Sequencer controlled</i> 4: <i>Forward GPIO</i> 5: <i>reserved</i> 6: <i>Forward GPI2</i> 7: <i>Forward GPI3</i>	000
GPIO0_OUT	2:0	<i>GPIO output function</i> 0: <i>Static value according GPIO*_MODE</i> 1: <i>VDD_FAULT</i> 2: <i>32 kHz crystal clock</i> 3: <i>Sequencer controlled</i> 4: <i>reserved</i> 5: <i>Forward GPI1</i> 6: <i>Forward GPI2</i> 7: <i>Forward GPI3</i>	000

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Table 60: GPIO_OUT3_4 (0x01F)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
GPIO4_OUT	4:3	GPIO output function 0: Static value according GPIO*_MODE 1: VDD_FAULT 2: 32 kHz crystal clock 3: Sequencer controlled	00
GPIO3_OUT	2:0	<i>GPIO output function</i> <i>0: Static value according GPIO*_MODE</i> <i>1: VDD_FAULT</i> <i>2: 32 kHz crystal clock</i> <i>3: Sequencer controlled</i> <i>4: Forward GPIO</i> <i>5: Forward GPI1</i> <i>6: Forward GPI2</i> <i>7: reserved</i>	000

A.1.7 Power supply control

Table 61: BUCK2_CONT (0x020)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
VBUCK2_GPI	6:5	Voltage controlling GPI (passive to active transition: VB*_B, act. to pas.: VB*_A)	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
BUCK2_CONF	3:3	Default supply, or sequenced and on in POWERDOWN	0
BUCK2_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable)	00
BUCK2_EN	0:0	Disable (0) / enable (1) the buck (dependent on on/off priority order), except in BUCK1/2 dual phase mode	0

Entry level PMIC for applications requiring up to 8.5 A

Table 62: BUCK1_CONT (0x021)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
VBUCK1_GPI	6:5	Voltage controlling GPI (passive to active transition: VB*_B, act. to pas.: VB*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
BUCK1_CONF	3:3	Default supply, or sequenced and on in POWERDOWN	0
BUCK1_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
BUCK1_EN	0:0	Enable (dependent on on/off priority order)	0

Table 63: BUCK4_CONT (0x022)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
VBUCK4_GPI	6:5	Voltage controlling GPI (passive to active transition: VB*_B, act. to pas.: VB*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
BUCK4_CONF	3:3	Default supply, or sequenced and on in POWERDOWN	0
BUCK4_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
BUCK4_EN	0:0	Enable (dependent on on/off priority order)	0

Entry level PMIC for applications requiring up to 8.5 A

Table 64: BUCK3_CONT (0x024)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
VBUCK3_GPI	6:5	Voltage controlling GPI (passive to active transition: VB*_B, act. to pas.: VB*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
BUCK3_CONF	3:3	Default supply, or sequenced and on in POWERDOWN	0
BUCK3_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
BUCK3_EN	0:0	Enable (dependent on on/off priority order)	0

Table 65: LDO1_CONT (0x026)

Field	Slice	Description	Reset
LDO1_CONF	7:7	Default supply, or sequenced and on in POWERDOWN	0
VLDO1_GPI	6:5	Voltage controlling GPI (passive to active transition: VLDO*_B, act. to pas.: VLDO*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
LDO1_PD_DIS	3:3	Disable pull-down resistor when disabled.	0
LDO1_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
LDO1_EN	0:0	Enable (dependent on on/off priority order)	0

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Table 66: LDO2_CONT (0x027)

Field	Slice	Description	Reset
LDO2_CONF	7:7	Default supply, or sequenced and on in POWERDOWN	0
VLDO2_GPI	6:5	Voltage controlling GPI (passive to active transition: VLDO*_B, act. to pas.: VLDO*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
LDO2_PD_DIS	3:3	Disable pull-down resistor when disabled.	0
LDO2_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
LDO2_EN	0:0	Enable (dependent on on/off priority order)	0

Table 67: LDO3_CONT (0x028)

Field	Slice	Description	Reset
LDO3_CONF	7:7	Default supply, or sequenced and on in POWERDOWN	0
VLDO3_GPI	6:5	Voltage controlling GPI (passive to active transition: VLDO*_B, act. to pas.: VLDO*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
LDO3_PD_DIS	3:3	Disable pull-down resistor when disabled.	0
LDO3_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
LDO3_EN	0:0	Enable (dependent on on/off priority order)	0

Entry level PMIC for applications requiring up to 8.5 A

Table 68: LDO4_CONT (0x029)

Field	Slice	Description	Reset
LDO4_CONF	7:7	Default supply, or sequenced and on in POWERDOWN	0
VLDO4_GPI	6:5	Voltage controlling GPI (passive to active transition: VLDO*_B, act. to pas.: VLDO*_A) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
<i>Reserved</i>	4:4	<i>Reserved</i>	
LDO4_PD_DIS	3:3	Disable pull-down resistor when disabled.	0
LDO4_GPI	2:1	Enabling GPI (passive to active transition: enable, act. to pas.: disable) 0: Sequencer controlled 1: Select GPI1 2: Select GPI2 3: Select GPI3	00
LDO4_EN	0:0	Enable (dependent on on/off priority order)	0

Table 69: DVC_1 (0x032)

Field	Slice	Description	Reset
VLDO4_SEL	7:7	Select VLDO4_A (0) / VLDO4_B (1).	0
VLDO3_SEL	6:6	Select VLDO3_A (0) / VLDO3_B (1).	0
VLDO2_SEL	5:5	Select VLDO2_A (0) / VLDO2_B (1).	0
VLDO1_SEL	4:4	Select VLDO1_A (0) / VLDO1_B (1).	0
VBUCK3_SEL	3:3	Select VBUCK3_A (0) / VBUCK3_B (1).	0
VBUCK4_SEL	2:2	Select VBUCK4_A (0) / VBUCK4_B (1).	0
VBUCK2_SEL	1:1	Select VBUCK2_A (0) / VBUCK2_B (1).	0
VBUCK1_SEL	0:0	Select VBUCK1_A (0) / VBUCK1_B (1).	0

Entry level PMIC for applications requiring up to 8.5 A

A.1.8 RTC calendar and alarm

Table 70: COUNT_S (0x040)

Field	Slice	Description	Reset
RTC_READ	7:7	Indicates that RTC calendar is ready to be read by the host.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
COUNT_SEC	5:0	Calendar seconds Bus write is snapshot and updated on a write to COUNT_YEAR. Bus read loads RTC calendar into 0x104-0x109.	0x0

Table 71: COUNT_MI (0x041)

Field	Slice	Description	Reset
<i>Reserved</i>	6:6	<i>Reserved</i>	
COUNT_MIN	5:0	Calendar minutes 0-59 Bus write is snapshot and updated on a write to COUNT_YEAR. Bus read is snapshot and updated on a read from COUNT_SEC.	0x0

Table 72: COUNT_H (0x042)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
COUNT_HOUR	4:0	Calendar hours 0-23 Bus write is snapshot and updated on a write to COUNT_YEAR. Bus read is snapshot and updated on a read from COUNT_SEC.	0x0

Table 73: COUNT_D (0x043)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
COUNT_DAY	4:0	Calendar day 1-31 Bus write is snapshot and updated on a write to COUNT_YEAR. Bus read is snapshot and updated on a read from COUNT_SEC.	0x1

Table 74: COUNT_MO (0x044)

Field	Slice	Description	Reset
<i>Reserved</i>	7:4	<i>Reserved</i>	
COUNT_MONTH	3:0	Calendar month 1-12 Bus write is snapshot and updated on a write to COUNT_YEAR. Bus read is snapshot and updated on a read from COUNT_SEC.	0x1

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Table 75: COUNT_Y (0x045)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
MONITOR	6:6	Read: RTC power has been lost (0) / RTC clock okay (1). Write: RTC_EN and CRYSTAL writing enabled (0) / disabled (1). Fetched from VDDRRTC domain at VDDCORE POR. If set, host writes to this register are ignored; thus the host cannot clear it.	1
COUNT_YEAR	5:0	Calendar year 2000 - 2063 Bus write turns on the RTC clock and sets RTC calendar. Bus read is snapshot and updated on a read from COUNT_SEC.	0x0

Table 76: ALARM_S (0x046)

Field	Slice	Description	Reset
ALARM_STATUS	7:6	Alarm reason 0: No alarm 1: Tick 2: Timer 3: Tick + Timer	00
ALARM_SEC	5:0	Alarm seconds 0-59 Bus write is snapshot and updated on a write to ALARM_YEAR.	0x0

Table 77: ALARM_MI (0x047)

Field	Slice	Description	Reset
<i>Reserved</i>	7:6	<i>Reserved</i>	
ALARM_MIN	5:0	Alarm minutes 0-59 Bus write is snapshot and updated on a write to ALARM_YEAR.	0x0

Table 78: ALARM_H (0x048)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
ALARM_HOUR	4:0	Alarm hour 0-23 Bus write is snapshot and updated on a write to ALARM_YEAR.	0x0

Table 79: ALARM_D (0x049)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
ALARM_DAY	4:0	Alarm day 1-31 Bus write is snapshot and updated on a write to ALARM_YEAR.	0x1

Entry level PMIC for applications requiring up to 8.5 A

Table 80: ALARM_MO (0x04A)

Field	Slice	Description	Reset
<i>Reserved</i>	7:6	<i>Reserved</i>	
TICK_WAKE	5:5	Allows a TICK to wake the chip from RTC mode	1
TICK_TYPE	4:4	Period of the TICK 0: TICK every second 1: TICK every minute	1
ALARM_MONTH	3:0	Alarm month 1-12 Bus write is snapshot and updated on a write to ALARM_YEAR.	0x1

Table 81: ALARM_Y (0x04B)

Field	Slice	Description	Reset
TICK_ON	7:7	Enable the tick function.	0
ALARM_ON	6:6	Enable the alarm function. Alarm time is set with the ALARM_* registers	0
ALARM_YEAR	5:0	Alarm year 2000 - 2063	0x0

Table 82: SECOND_A (0x04C)

Field	Slice	Description	Reset
SECONDS_A	7:0	RTC seconds counter LS byte	0x0

Table 83: SECOND_B (0x04D)

Field	Slice	Description	Reset
SECONDS_B	7:0	RTC seconds counter byte Bus read is snapshot and updated on a read from SECONDS_A.	0x0

Table 84: SECOND_C (0x04E)

Field	Slice	Description	Reset
SECONDS_C	7:0	RTC seconds counter byte Bus read is snapshot and updated on a read from SECONDS_A.	0x0

Table 85: SECOND_D (0x04F)

Field	Slice	Description	Reset
SECONDS_D	7:0	RTC seconds counter MS byte Bus read is snapshot and updated on a read from SECONDS_A.	0x0

Entry level PMIC for applications requiring up to 8.5 A

A.2 PAGE 1

A.2.1 Power sequencer

Table 86: SEQ (0x081)

Field	Slice	Description	Reset
NXT_SEQ_START	7:4	Start position of next sequence	0x0
SEQ_POINTER	3:0	Actual power sequencer position	0x0

Table 87: SEQ_TIMER (0x082)

Field	Slice	Description	Reset
SEQ_DUMMY	7:4	Waiting time for power sequencer slots which do not have an associated power supply. 0: 32 μ s 1: 64 μ s 2: 96 μ s 3: 128 μ s 4: 160 μ s 5: 192 μ s 6: 224 μ s 7: 256 μ s 8: 288 μ s 9: 384 μ s 10: 448 μ s 11: 512 μ s 12: 1.024 ms 13: 2.048 ms 14: 4.096 ms 15: 8.192 ms	0xD
SEQ_TIME	3:0	Length of each PSS sequencer time slot 0: 32 μ s 1: 64 μ s 2: 96 μ s 3: 128 μ s 4: 160 μ s 5: 192 μ s 6: 224 μ s 7: 256 μ s 8: 288 μ s 9: 384 μ s 10: 448 μ s 11: 512 μ s 12: 1.024 ms 13: 2.048 ms 14: 4.096 ms 15: 8.192 ms	0xC

Entry level PMIC for applications requiring up to 8.5 A

Table 88: ID_2_1 (0x083)

Field	Slice	Description	Reset
LDO2_STEP	7:4	Sequencer step for LDO2	0x0
LDO1_STEP	3:0	Sequencer step for LDO1	0x0

Table 89: ID_4_3 (0x084)

Field	Slice	Description	Reset
LDO4_STEP	7:4	Sequencer step for LDO4	0x0
LDO3_STEP	3:0	Sequencer step for LDO3	0x0

Table 90: ID_12_11 (0x088)

Field	Slice	Description	Reset
PD_DIS_STEP	7:4	Sequencer step for Power-down Disable	0x0
<i>Reserved</i>	3:0	<i>Reserved</i>	

Table 91: ID_14_13 (0x089)

Field	Slice	Description	Reset
BUCK2_STEP	7:4	Sequencer step for Buck2	0x0
BUCK1_STEP	3:0	Sequencer step for Buck1	0x0

Table 92: ID_16_15 (0x08A)

Field	Slice	Description	Reset
BUCK3_STEP	7:4	Sequencer step for Buck3	0x0
BUCK4_STEP	3:0	Sequencer step for Buck4	0x0

Table 93: ID_22_21 (0x08D)

Field	Slice	Description	Reset
GP_FALL1_STEP	7:4	Sequencer step for de-assert GPO0	0x0
GP_RISE0_STEP	3:0	Sequencer step for assert GPO0	0x0

Table 94: ID_24_23 (0x08E)

Field	Slice	Description	Reset
GP_FALL2_STEP	7:4	Sequencer step for de-assert GPO1	0x0
GP_RISE1_STEP	3:0	Sequencer step for assert GPO1	0x0

Table 95: ID_26_25 (0x08F)

Field	Slice	Description	Reset
GP_FALL3_STEP	7:4	Sequencer step for de-assert GPO2	0x0
GP_RISE2_STEP	3:0	Sequencer step for assert GPO2	0x0

Entry level PMIC for applications requiring up to 8.5 A

Table 96: ID_28_27 (0x090)

Field	Slice	Description	Reset
GP_FALL4_STEP	7:4	Sequencer step for de-assert GPO3	0x0
GP_RISE3_STEP	3:0	Sequencer step for assert GPO3	0x0

Table 97: ID_30_29 (0x091)

Field	Slice	Description	Reset
GP_FALL5_STEP	7:4	Sequencer step for de-assert GPO4	0x0
GP_RISE4_STEP	3:0	Sequencer step for assert GPO4	0x0

Table 98: ID_32_31 (0x092)

Field	Slice	Description	Reset
EN32K_STEP	7:4	Sequencer step for enabling GPO and RTC clock	0x0
WAIT_STEP	3:0	Sequencer step for WAIT	0x0

Table 99: SEQ_A (0x095)

Field	Slice	Description	Reset
POWER_END	7:4	End of POWER power domain in the PSS sequencer SYSTEM_END <= POWER_END <= MAX_COUNT must be true.	0x3
SYSTEM_END	3:0	End of SYSTEM power domain in the PSS sequencer PART_DOWN <= SYSTEM_END <= POWER_END must be true.	0x2

Table 100: SEQ_B (0x096)

Field	Slice	Description	Reset
PART_DOWN	7:4	PSS sequencer slot to stop at, when going down into STANDBY state. 1 <= PART_DOWN <= SYSTEM_END must be true.	0x1
MAX_COUNT	3:0	End of POWER1 power domain in the PSS sequencer POWER_END <= MAX_COUNT must be true.	0x4

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Table 101: WAIT (0x097)

Field	Slice	Description	Reset
WAIT_DIR	7:6	WAIT STEP power sequence selection 0: Do not wait during WAIT_STEP of power sequencer except for normal slot time. 1: Wait during up sequence. 2: Wait during down sequence. 3: Wait during up and down sequence.	00
TIME_OUT	5:5	Timeout when WAIT_MODE = 0 0: no timeout when waiting for external signal (GPIO3). 1: 500 ms timeout when waiting for external signal (GPIO3).	0
WAIT_MODE	4:4	0: Wait for external signal (GPIO3) to be active. 1: Start timer and wait for expiration.	1
WAIT_TIME	3:0	Wait timer during WAIT STEP of power sequencer (+/- 10%) 0: Do not wait during WAIT_STEP of power sequencer except for normal slot time. 1: 512 μ s 2: 1.0 ms 3: 2.0 ms 4: 4.1 ms 5: 8.2 ms 6: 16.4 ms 7: 32.8 ms 8: 65.5 ms 9: 128 ms 10: 256 ms 11: 512 ms 12: 1.0 s 13: 2.0 s 14: 4.1 s 15: 8.2 s	0xB

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Table 102: EN_32K (0x098)

Field	Slice	Description	Reset
EN_32KOUT	7:7	Enable the OUT_32K GPO (may be delayed depending on OUT32K_PAUSE).	1
<i>Reserved</i>	6:6	<i>Reserved</i>	
OUT_CLOCK	5:5	Disable clock to GPOs until stabilisation timer has expired.	1
DELAY_MODE	4:4	Start stabilisation timer ... 0: ... when oscillator signal is available (third falling edge) 1: ... when oscillator has been switched on (CRYSTAL risen)	0
CRYSTAL	3:3	External RTC crystal is present. Fetched from VDDRTC domain at VDDCORE POR.	1
STABILISATION_TIME	2:0	Time to allow crystal oscillator to stabilise. 0: Delay off 1: 0.52 s 2: 1.0 s 3: 1.5 s 4: 2.1 s 5: 2.6 s 6: 3.1 s 7: 3.6 s	001

Table 103: RESET (0x099)

Field	Slice	Description	Reset
RESET_EVENT	7:6	Reset timer started by: 0: EXT_WAKEUP 1: SYS_UP (register control or pin) 2: PWR_UP (register control or pin) 3: Leaving PMIC RESET mode	01
RESET_TIMER	5:0	0: Release nRESET immediately after the event selected by RESET_EVENT. 1 - 31: 1.024 ms * RESET_TIMER 32-63: 1.024 ms * 32 * (RESET_TIMER-31)	0x5

A.2.2 Power supply control

Table 104: BUCK_ILIM_A (0x09A)

Field	Slice	Description	Reset
<i>Reserved</i>	7:4	<i>Reserved</i>	
BUCK3_ILIM	3:0	Buck current limit = (1500 + n * 100) mA	0xA

Table 105: BUCK_ILIM_B (0x09B)

Field	Slice	Description	Reset
<i>Reserved</i>	7:4	<i>Reserved</i>	
BUCK4_ILIM	3:0	Buck current limit = (500 + n * 100) mA	0xA

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Table 106: BUCK_ILIM_C (0x09C)

Field	Slice	Description	Reset
BUCK2_ILIM	7:4	Buck current limit = $(500 + n * 100)$ mA In full-current mode the limit is internally doubled.	0xA
BUCK1_ILIM	3:0	Buck current limit = $(500 + n * 100)$ mA In full-current mode the limit is internally doubled.	0xA

Table 107: BUCK2_CFG (0x09D)

Field	Slice	Description	Reset
BUCK2_MODE	7:6		11
BUCK2_PD_DIS	5:5	Disable pull-down resistor when disabled.	0
<i>Reserved</i>	4:0	<i>Reserved</i>	

Table 108: BUCK1_CFG (0x09E)

Field	Slice	Description	Reset
BUCK1_MODE	7:6	0: Controlled by B*_SL_A/B 1: Sleep 2: Synchronous 3: Automatic	11
BUCK1_PD_DIS	5:5	Disable pull-down resistor when disabled.	0
<i>Reserved</i>	4:1	<i>Reserved</i>	
<i>Reserved</i>	0:0	<i>Reserved</i>	

Table 109: BUCK4_CFG (0x09F)

Field	Slice	Description	Reset
BUCK4_MODE	7:6	0: Controlled by B*_SL_A/B 1: Sleep 2: Synchronous 3: Automatic	11
BUCK4_PD_DIS	5:5	Disable pull-down resistor when disabled.	0
BUCK4_VTT_EN	4:4	Enable Buck4 memory bus termination mode.	0
BUCK4_VTTR_EN	3:3	Enable Buck4 memory bus termination reference voltage output.	0
<i>Reserved</i>	2:0	<i>Reserved</i>	

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Table 110: BUCK3_CFG (0x0A0)

Field	Slice	Description	Reset
BUCK3_MODE	7:6	0: Controlled by B*_SL_A/B 1: Sleep 2: Synchronous 3: Automatic	11
BUCK3_PD_DIS	5:5	Disable pull-down resistor when disabled.	0
<i>Reserved</i>	4:0	<i>Reserved</i>	

Table 111: VBUCK2_A (0x0A3)

Field	Slice	Description	Reset
BUCK2_SL_A	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_A is active.	0
VBUCK2_A	6:0	From 0.3 V (0x00) to 1.57 V (0x7F) in steps of 10 mV	0x50

Table 112: VBUCK1_A (0x0A4)

Field	Slice	Description	Reset
BUCK1_SL_A	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_A is active.	0
VBUCK1_A	6:0	From 0.3 V (0x00) to 1.57 V (0x7F) in steps of 10 mV	0x50

Table 113: VBUCK4_A (0x0A5)

Field	Slice	Description	Reset
BUCK4_SL_A	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_A is active.	0
VBUCK4_A	6:0	From 0.53 V (0x00) to 1.8 V (0x7F) in steps of 10 mV	0x43

Table 114: VBUCK3_A (0x0A7)

Field	Slice	Description	Reset
BUCK3_SL_A	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_A is active.	0
VBUCK3_A	6:0	From 0.80 V (0x00) to 3.34 V (0x7F) in steps of 20 mV	0x14

Table 115: VLDO1_A (0x0A9)

Field	Slice	Description	Reset
LDO1_SL_A	7:7	Force LDO sleep mode if VLDO*_A is active.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO1_A	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

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Table 116: VLDO2_A (0x0AA)

Field	Slice	Description	Reset
LDO2_SL_A	7:7	Force LDO sleep mode if VLDO*_A is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO2_A	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

Table 117: VLDO3_A (0x0AB)

Field	Slice	Description	Reset
LDO3_SL_A	7:7	Force LDO sleep mode if VLDO*_A is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO3_A	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

Table 118: VLDO4_A (0x0AC)

Field	Slice	Description	Reset
LDO4_SL_A	7:7	Force LDO sleep mode if VLDO*_A is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO4_A	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

Table 119: VBUCK2_B (0x0B4)

Field	Slice	Description	Reset
BUCK2_SL_B	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_B is active.	1
VBUCK2_B	6:0	From 0.3 V (0x00) to 1.57 V (0x7F) in steps of 10 mV	0x3C

Table 120: VBUCK1_B (0x0B5)

Field	Slice	Description	Reset
BUCK1_SL_B	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_B is active.	1
VBUCK1_B	6:0	From 0.3 V (0x00) to 1.57 V (0x7F) in steps of 10 mV	0x3C

Table 121: VBUCK4_B (0x0B6)

Field	Slice	Description	Reset
BUCK4_SL_B	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_B is active.	1
VBUCK4_B	6:0	From 0.53 V (0x00) to 1.8 V (0x7F) in steps of 10 mV	0x43

Table 122: VBUCK3_B (0x0B8)

Field	Slice	Description	Reset
BUCK3_SL_B	7:7	Force sync (0) / sleep (1) mode if B*_MODE==VSELCTL and VB*_B is active.	1
VBUCK3_B	6:0	From 0.80 V (0x00) to 3.34 V (0x7F) in steps of 20 mV	0x14

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Table 123: VLDO1_B (0x0BA)

Field	Slice	Description	Reset
LDO1_SL_B	7:7	Force LDO sleep mode if VLDO*_B is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO1_B	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

Table 124: VLDO2_B (0x0BB)

Field	Slice	Description	Reset
LDO2_SL_B	7:7	Force LDO sleep mode if VLDO*_B is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO2_B	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

Table 125: VLDO3_B (0x0BC)

Field	Slice	Description	Reset
LDO3_SL_B	7:7	Force LDO sleep mode if VLDO*_B is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO3_B	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

Table 126: VLDO4_B (0x0BD)

Field	Slice	Description	Reset
LDO4_SL_B	7:7	Force LDO sleep mode if VLDO*_B is selected.	0
<i>Reserved</i>	6:6	<i>Reserved</i>	
VLDO4_B	5:0	From 0.90 V (0x02) to 3.60 V (0x38) in steps of 50 mV Less than 0x02: 0.90 V; greater than 0x38: 3.60 V	0x31

A.2.3 BBAT charger control

Table 127: BBAT_CONT (0x0C5)

Field	Slice	Description	Reset
BCHG_ISET	7:4	Charging current setting 0000: disabled 0001: 100 μ A 0010: 200 μ A 0011: 300 μ A 0100: 400 μ A 0101: 500 μ A 0110: 600 μ A 0111: 700 μ A 1000: 800 μ A 1001: 900 μ A 1010: 1 mA 1011: 2 mA 1100: 3 mA 1101: 4 mA 1110: 5 mA 1111: 6 mA	0x0

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BCHG_VSET	3:0	Termination voltage setting 0000: disabled 0001: 1.1 V 0010: 1.2 V 0011: 1.4 V 0100: 1.6 V 0101: 1.8 V 0110: 2.0 V 0111: 2.2 V 1000: 2.4 V 1001: 2.5 V 1010: 2.6 V 1011: 2.7 V 1100: 2.8 V 1101: 2.9 V 1110: 3.0 V 1111: 3.1 V	0xE
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A.3.1 Customer trim and configuration

Table 128: INTERFACE (0x105)

Field	Slice	Description	Reset
IF_BASE_ADDR	7:4	2-WIRE slave address MSBs. The LSBs of the slave address are "000". The complete slave address is then $IF_BASE_ADDR * 2^3$. However, the device also responds to $IF_BASE_ADDR * 2^3 + 1$.	0xB
<i>Reserved</i>	3:0	<i>Reserved</i>	

Table 129: CONFIG_A (0x106)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
PM_IF_HSM	6:6	2-WIRE interface permanently in high speed mode	0
PM_IF_FMP	5:5	2-WIRE interface selects fast-mode+ timings	0
PM_IF_V	4:4	2-WIRE supplied from VDDCORE (0) / V _{DDIO} (1).	0
IRQ_TYPE	3:3	nIRQ is active low (0) / high (1).	0
PM_O_TYPE	2:2	nRESET and nIRQ are push pull (0) / open drain (1).	1
<i>Reserved</i>	1:1	<i>Reserved</i>	
PM_I_V	0:0	nRESETREQ, SYS_EN, PWR_EN and KEEPACT supplied from VDDCORE (0) / V _{DDIO} (1).	0

Table 130: CONFIG_B (0x107)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
VDD_HYST_ADJ	6:4	VDD_FAULT comparator hysteresis from 100 mV (0x0) to 450 mV (0x7) in 50 mV steps	001
VDD_FAULT_ADJ	3:0	VDD_FAULT comparator level from 2.5 V (0x0) to 3.25 V (0xF) in 50 mV steps	0x6

Table 131: CONFIG_C (0x108)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
BUCK3_CLK_INV	6:6	Buck clock polarity inverted.	0
<i>Reserved</i>	5:5	<i>Reserved</i>	
BUCK4_CLK_INV	4:4	Buck clock polarity inverted.	1
BUCK1_CLK_INV	3:3	Buck clock polarity inverted.	0
BUCK_ACTV_DISCHRG	2:2	Enable active discharging of buck rails.	1
<i>Reserved</i>	1:0	<i>Reserved</i>	

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Table 132: CONFIG_D (0x109)

Field	Slice	Description	Reset
<i>Reserved</i>	7:6	<i>Reserved</i>	
FORCE_RESET	5:5	Keep nRESET always asserted	0
<i>Reserved</i>	4:3	<i>Reserved</i>	
SYSTEM_EN_RD	2:2	Suppress loading SYSTEM_EN during OTP_RD2	0
NIRQ_MODE	1:1	nIRQ will be asserted from events during POWERDOWN ...	0
GPI_V	0:0	GPIs, except power manager controls, supplied from VDDCORE (0) / V _{DDIO} (1).	0

Table 133: CONFIG_E (0x10A)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
BUCK3_AUTO	4:4	When powering up, enable and select VBUCK3_A.	0
<i>Reserved</i>	3:3	<i>Reserved</i>	
BUCK4_AUTO	2:2	When powering up, enable and select VBUCK4_A.	0
BUCK2_AUTO	1:1	When powering up, enable and select VBUCK2_A.	0
BUCK1_AUTO	0:0	When powering up, enable and select VBUCK1_A.	0

Table 134: CONFIG_G (0x10C)

Field	Slice	Description	Reset
<i>Reserved</i>	7:4	<i>Reserved</i>	
LDO4_AUTO	3:3	When powering up, enable and select VLDO4_A.	0
LDO3_AUTO	2:2	When powering up, enable and select VLDO3_A.	0
LDO2_AUTO	1:1	When powering up, enable and select VLDO2_A.	0
LDO1_AUTO	0:0	When powering up, enable and select VLDO1_A.	0

Table 135: CONFIG_H (0x10D)

Field	Slice	Description	Reset
<i>Reserved</i>	7:7	<i>Reserved</i>	
BUCK1_FCM	6:6	Buck full-current mode (double pass device and current limit).	0
BUCK2_FCM	5:5	Buck full-current mode (double pass device and current limit).	0
<i>Reserved</i>	4:4	<i>Reserved</i>	
BUCK_MERGE	3:3	Buck1 and Buck2 output are merged (dual phase buck).	0
<i>Reserved</i>	2:0	<i>Reserved</i>	

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Table 136: CONFIG_I (0x10E)

Field	Slice	Description	Reset
LDO_SD	7:7	Enable switching off an LDO if an over-current is detected longer than 200 ms.	0
INT_SD_MODE	6:6	Skip seq and dummy slot on shutdown from internal fault.	0
HOST_SD_MODE	5:5	Skip seq and dummy slot on shutdown from SHUTDOWN or nRESETREQ.	1
KEY_SD_MODE	4:4	Enable power-on reset on shutdown from nONKEY.	0
WATCHDOG_SD	3:3	Enable shutdown instead of power-down on watchdog timeout.	1
nONKEY_SD	2:2	Enable shutdown via long pressing nONKEY.	0
NONKEY_PIN	1:0	nONKEY function	01

Table 137: CONFIG_J (0x10F)

Field	Slice	Description	Reset
IF_RESET	7:7	Enable host interface reset via nRESETREQ pin	0
TWOWIRE_TO	6:6	Enable 35 ms timeout for 2-wire interfaces	0
RESET_DURATION	5:4	Minimum RESET mode duration: 0x00 = 22 ms 0x01 = 100 ms 0x10 = 500 ms 0x11 = 1 s	00
SHUT_DELAY	3:2	Shut down delay (+ KEY_DELAY) for nONKEY	10
KEY_DELAY	1:0	nONKEY locking threshold	10

Table 138: CONFIG_K (0x110)

Field	Slice	Description	Reset
<i>Reserved</i>	7:5	<i>Reserved</i>	
GPIO4_PUPD	4:4	GPI: pull-down enabled open drain GPO: pull-up enabled	0
GPIO3_PUPD	3:3	GPI: pull-down enabled open drain GPO: pull-up enabled	0
GPIO2_PUPD	2:2	GPI: pull-down enabled open drain GPO: pull-up enabled	0
GPIO1_PUPD	1:1	GPI: pull-down enabled open drain GPO: pull-up enabled	0
GPIO0_PUPD	0:0	GPI: pull-down enabled open drain GPO: pull-up enabled	0

Table 139: CONFIG_M (0x112)

Field	Slice	Description	Reset
OSC_FRQ	7:4	Modify HF oscillator frequency by about $\pm 10\%$ (-8/+7 steps).	0x0
WDG_MODE	3:3	Select watchdog Halt operation mode.	0
<i>Reserved</i>	2:2	<i>Reserved</i>	
NRESETREQ_PU	1:1	nRESETREQ: pull-up enabled	0
<i>Reserved</i>	0:0	<i>Reserved</i>	

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A.3.2 Customer device specific

Table 140: GP_ID_0 (0x121)

Field	Slice	Description	Reset
GP_0	7:0	General purpose register	0x0

Table 141: GP_ID_1 (0x122)

Field	Slice	Description	Reset
GP_1	7:0	General purpose register	0x0

Table 142: GP_ID_2 (0x123)

Field	Slice	Description	Reset
GP_2	7:0	General purpose register	0x0

Table 143: GP_ID_3 (0x124)

Field	Slice	Description	Reset
GP_3	7:0	General purpose register	0x0

Table 144: GP_ID_4 (0x125)

Field	Slice	Description	Reset
GP_4	7:0	General purpose register	0x0

Table 145: GP_ID_5 (0x126)

Field	Slice	Description	Reset
GP_5	7:0	General purpose register	0x0

Table 146: GP_ID_6 (0x127)

Field	Slice	Description	Reset
GP_6	7:0	General purpose register	0x0

Table 147: GP_ID_7 (0x128)

Field	Slice	Description	Reset
GP_7	7:0	General purpose register	0x0

Table 148: GP_ID_8 (0x129)

Field	Slice	Description	Reset
GP_8	7:0	General purpose register	0x0

Table 149: GP_ID_9 (0x12A)

Field	Slice	Description	Reset
GP_9	7:0	General purpose register	0x0

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Table 150: GP_ID_10 (0x12B)

Field	Slice	Description	Reset
GP_10	7:0	General purpose register	0x0

Table 151: GP_ID_11 (0x12C)

Field	Slice	Description	Reset
GP_11	7:0	General purpose register	0x0

Table 152: GP_ID_12 (0x12D)

Field	Slice	Description	Reset
GP_12	7:0	General purpose register	0x0

Table 153: GP_ID_13 (0x12E)

Field	Slice	Description	Reset
GP_13	7:0	General purpose register	0x0

Table 154: GP_ID_14 (0x12F)

Field	Slice	Description	Reset
GP_14	7:0	General purpose register	0x0

Table 155: GP_ID_15 (0x130)

Field	Slice	Description	Reset
GP_15	7:0	General purpose register	0x0

Table 156: GP_ID_16 (0x131)

Field	Slice	Description	Reset
GP_16	7:0	General purpose register	0x0

Table 157: GP_ID_17 (0x132)

Field	Slice	Description	Reset
GP_17	7:0	General purpose register	0x0

Table 158: GP_ID_18 (0x133)

Field	Slice	Description	Reset
GP_18	7:0	General purpose register	0x0

Table 159: GP_ID_19 (0x134)

Field	Slice	Description	Reset
GP_19	7:0	General purpose register	0x0

Table 160: DEVICE_ID (0x181)

Field	Slice	Description	Reset
DEV_ID	7:0	Device ID	0x0

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Table 161: VARIANT_ID (0x182)

Field	Slice	Description	Reset
MRC	7:4	Mask revision code	0x0
VRC	3:0	Chip variant code	

Table 162: CUSTOMER_ID (0x183)

Field	Slice	Description	Reset
CUST_ID	7:0	Customer ID	0x0

Table 163: CONFIG_ID (0x184)

Field	Slice	Description	Reset
CONFIG_REV	7:0	OTP settings revision	0x0

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Revision history

Table 164: Revision history

Revision	Date	Changes
3.2	17-Feb-2016	<p>Table 3: Absolute maximum ratings</p> <ul style="list-style-type: none"> replaced T_A parameter with T_J replaced Note 1 ESD tolerance renamed to ESD protection HBM and moved the value to Min added ESD protection CDM parameters <p>Table 4: Recommended operating conditions</p> <ul style="list-style-type: none"> added Maximum power dissipation added Note 2 <p>Table 5: Digital I/O electrical characteristics</p> <ul style="list-style-type: none"> R_{PU}: values aligned with characterisation results: <ul style="list-style-type: none"> $V_{DDIO} = 1.5\text{ V}$: Min value changed from 100 to 60 kΩ $V_{DDIO} = 1.5\text{ V}$: Max value changed from 340 to 310 kΩ $V_{DDIO} = 1.8\text{ V}$: Min value changed from 65 to 45 kΩ $V_{DDIO} = 1.8\text{ V}$: Max value changed from 175 to 190 kΩ $V_{DDIO} = 3.3\text{ V}$: Min value changed from 25 to 20 kΩ <p>Table 10: LDOCORE electrical characteristics</p> <ul style="list-style-type: none"> removed V_{DD} parameter added $V_{DROPOUT}$ parameter added Note 1 and Note 2 added NOTE <p>Table 11, Table 12, Table 13: Buck1 to Buck4 electrical characteristics</p> <ul style="list-style-type: none"> V_{BUCK_ACC}: added Note 1 <p>Table 13: Buck4 electrical characteristics</p> <ul style="list-style-type: none"> V_{TTR}: removed I_{OUT} test condition C_{OUT}: renamed to C_{VTTR} <p>Table 14: Backup battery charger electrical characteristics</p> <ul style="list-style-type: none"> I_{SET_BCHG}: removed 1 to 6 mA test condition added C_{OUT}, R_{COUT_ESR}, $V_{DROPOUT}$ parameters added Note 1 and Note 2 <p>Table 17: System supply voltage supervision electrical characteristics</p> <ul style="list-style-type: none"> added Note 1 and Note 2 $V_{DD_FAULT_LOWER}$: removed test condition V_{HYS}: renamed to $V_{DD_FAULT_HYS}$ and removed test condition added V_{REF}, C_{VREF}, R_{IREF} parameters <p>Table 18: Junction temperature supervision electrical characteristics</p> <ul style="list-style-type: none"> added Note 1 <p>Figure 22: Structure of the power sequencer</p> <ul style="list-style-type: none"> added STANDBY mode added NOTE <p>Register map</p> <ul style="list-style-type: none"> Table 29 CONFIG_A control names corrected to PM_IF_HSM, PM_IF_FMP, and PM_IF_V Table 49: SLEW_RATE: 20 mV/step for Buck3 added Table 105: BUCK_ILIM_B and BUCK4_ILIM: Note removed regarding full-current mode <p>Other:</p> <ul style="list-style-type: none"> REG_PAGE corrected to PAGE NSHUTDOWN corrected to NRESETREQ Editorial changes
3.1	30-Oct-2015	First production datasheet release

Entry level PMIC for applications requiring up to 8.5 A

Status definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
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