LSI/CSI

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (631) 271-0400 FAX (631) 271-0405

LS7030

8 DECADE MULTIPLEXED COUNTER

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FEATURES:
- DC to 7.5 MHz Count Frequency
- Multiplexed BCD and 7 Segment Outputs
- DC to 500 kHz Scan Frequency
- +4.75V to +15V Operation (V_{SS} - V_{DD})
- Compatible with CMOS Logic
- High Input Noise Immunity
- Counter Output Latches
- Leading Zero Blanking
- Low Power Dissipation
- All inputs protected
- 40 Pin DIP - See Figure 1

DESCRIPTION: (See Block Diagram, Figure 4.)
The LS7030 is a MOS, 8 decade up counter. The circuit includes latches, multiplexer, leading zero blanking and 7 segment data outputs.

8 DECADE UP COUNTER
The eight decade ripple through counter increments on the negative edge of the input count pulse. Maximum ripple time is 12µs (99999999 to 00000000). Maximum count frequency is 7.5MHz.

RESET
All decades are reset to zero when $\overline{\text{Reset}}$ input is brought low for a minimum of 4µs. The Overflow flip-flop is reset at the same time. $\overline{\text{Reset}}$ must be high for a minimum of 1µs before next valid count can be recorded.

LATCHES
Contents of counter are transferred to latches when $\overline{\text{LOAD}}$ signal is brought low for a minimum of 4µs and kept low until a minimum of 12µs has elapsed from previous negative edge of count pulse (ripple time). Storage of valid data occurs when $\overline{\text{LOAD}}$ signal is high for a minimum of 1µs before next negative edge of count pulse or reset. Data is transferred for Overflow flip-flop to Overflow latch at the same time.

SCAN OSCILLATOR AND COUNTER
The scan counter is driven by an internal oscillator whose frequency is determined by a capacitor connected between Oscillator input and Scan input. An external scan clock applied to Scan input can also drive the scan counter. Scan counter advances on negative edge of scan clock.

The counter scans from MSD to LSD. When Scan Reset input is brought high the scan counter is forced to MSD state. Internal synchonization guarantees proper scanning no matter when Scan Reset is brought low relative to scan clock. Maximum scan frequency is 500kHz.

DECIMAL POINT
A high at the Decimal Point input resets the Blanking flip-flop causing the display to unblank. Decimal Point should be brought high at start of digit time which has active Decimal Point.

CONNECTION DIAGRAM - TOP VIEW

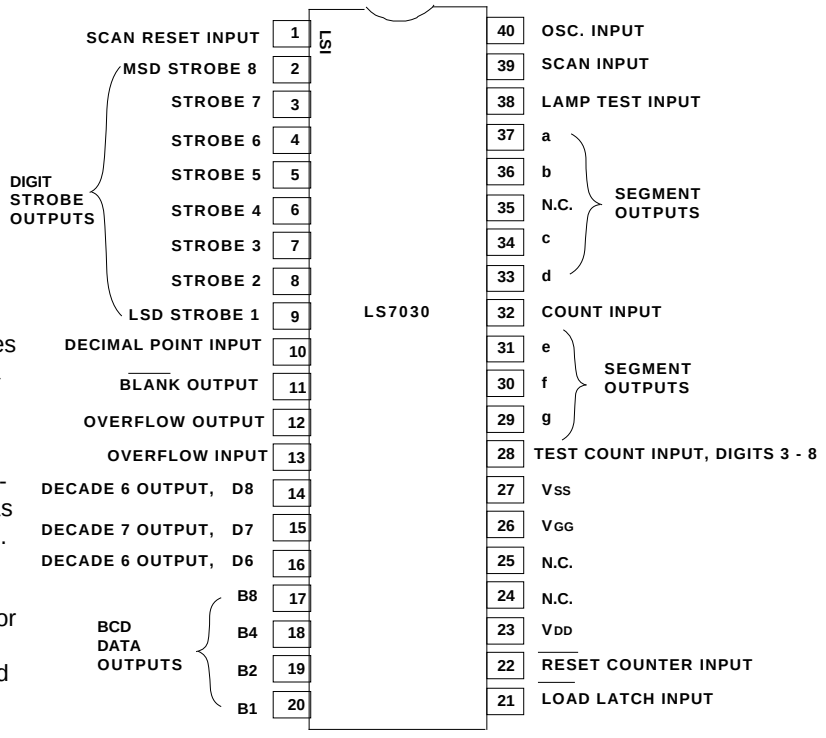

FIGURE 1

DIGIT STROBES
Timing of Digit Strobes is arranged such that both edges of strobe are guardbanded by a minimum 400ns within valid BCD data when scan frequency is 100kHz or less. The guardband is a minimum of 200ns at 250kHz scan frequency. At 500kHz only negative edge of Strobe is guaranteed to be within valid BCD data by a minimum 200ns.

OVERFLOW
The Overflow flip-flop sets on the first negative transition of the Overflow Input and remains set until $\overline{\text{Reset}}$ is brought low. Data is transferred from Overflow flip-flop to Overflow Latch when $\overline{\text{Load}}$ is brought low. A high at the Overflow Latch causes display to unblank. Overflow Output is output of Overflow Latch. MSB outputs of Decades 6, 7, 8 are available for use as Overflow Input.

BLANKING
Leading zero blanking is employed. At start of each MSD to LSD scan, display is blanked until a nonzero digit or active decimal point is encountered. Displaly unblanks during LSD time and for a whole scan when Overflow output is high. When Scan Reset is applied, display blanks to prevent display damage.

Blanking information is available at $\overline{\text{Blank}}$ output and is incorporated into 7 segment information.

BCD and 7 SEGMENT DATA

Data is available in BCD and 7 segment format. BCD data can be demultiplexed using Digit Strobes as latch enable signals.

POWER SUPPLIES

+4.75 Volts to +15 Volts single power supply operation is obtained when V_{GG} and V_{DD} are tied together. Inputs and outputs are CMOS compatible and Minimum Input Noise Immunity of 25% of power supply is guaranteed except for Test Count Input. (Inputs are TTL compatible at +4.75V to +5.25V operation.)

With V_{GG} at -12V, V_{DD} at OV and Vss at +5V, all inputs are TTL and CMOS compatible. All outputs are CMOS compatible and BCD and $\overline{\text{BLANK}}$ outputs also provide standard TTL compatibility. In addition, Overflow Output is low power TTL compatible. In either mode outputs swing between V_{DD} and Vss.

MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperature	T_A	-25 to +70	°C
Voltage (any pin to Vss)	Vmax	-30 to +0.5	V

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{GG} = OV, Vss = +4.75 to +15V, -25°C ≤ T_A ≥ +70°C unless otherwise specified.)

	PARAMETER	SYMBOL	MIN	MAX	UNITS
	Operating Supply Current (f_C = 7.5MHz)	Idds	-	15	mA
	Input Noise Immunity Low and High	Vni	25% (Vss - V_{DD})	-	V
	Test Count Input	Vil	Vss - 20	Vss - 3.95	V
		Vih	Vss - 1.0	Vss	V
D6, D7, D8 $\overline{\text{OF}}$, BCD Blank **(See Note 1)**	Output Voltage "0"	Vol	-	+0.2	V
	Output Voltage "1"	Voh	Vss - 1.0	-	V
Segment and Strobe Outputs **(See Note 2)**	Output Voltage "0" (sinking 10µA) Output Voltage "1"	Vol	-	+0.5	V
	Vss = 4.75 (Voh = Vss - 0.5V)	-	0.05	-	mA
	(Voh = Vss - 1V)	-	0.25	-	mA
	(Voh = Vss - 4V)	-	0.90	-	mA
	Vss = 10V (Voh = Vss - 2V)	-	2.0	-	mA
	(Voh = Vss - 3V)	-	3.0	-	mA
	Vss = 15V (Voh = Vss - 2V)	-	3.0	-	mA
	(Voh = Vss - 3V)	-	4.5	-	mA

NOTE 1: Current Sink = Same as segment and strobe outputs.
Current Source = N/A at Voh = Vss - 0.5V for Vss = +4.75V
35µA at Voh = Vss - 1V for Vss = +4.75V
40% of segment and strobe outputs at all other specified operating points.

NOTE 2: Limit segment current to 4.5mA maximum.
Limit strobe current to 6mA maximum.

The following inputs have internal pull down resistors to V_{DD} with maximum sink current of 5µA at Vss input.

Scan Reset	Test Count	Count
Decimal Point	Overflow	Lamp Test

SCAN OSCILLATOR

CAPACITANCE	TYPICAL OSCILLATOR FREQUENCY		
	4.75V	**10V**	**15V**
50pF	40.0 kHz	24.2kHz	22.2 kHz
100pF	22.2 kHz	14.8kHz	13.8 kHz
470pF	5.0 kHz	3.6kHz	3.5 kHz
750pF	3.3 kHz	2.4kHz	2.2 kHz
2000pF	1.3 kHz	0.91kHz	0.85 kHz

ELECTRICAL CHARACTERISTICS:
(V_{DD} = V_{GG} = OV, Vss = +4.75 to +15V, -25˚C ≤ T_A ≤ +70˚C unless otherwise specified.)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Count test and Count frequency				
(Vss = +5V ± 5%)	f_c, f_{tc}	DC	7.5	MHz
(Vss = +10V)	f_c, f_{tc}	DC	6	MHz
(Vss = +15V)	f_c, f_{tc}	DC	5	MHz
Scan frequency	f_{sc}	DC	500	kHz
Count Pulse Width				
(Vss = +5V ± 5%)	t_{cpw}	66	-	ns
(Vss = +10V)	t_{cpw}	83	-	ns
(Vss = +15V)	t_{cpw}	100	-	ns
Count Ripple Time	t_{cr}	-	12	µs
$\overline{\text{Load}}$ Pulse Width	t_{lpw}	4	-	µs
$\overline{\text{Load}}$ Removal Tme	t_{lr}	-	1	µs
$\overline{\text{Reset}}$ Pulse Width	t_{rpw}	4	-	µs
$\overline{\text{Reset}}$ Removal Time	t_{rr}	-	1	µs
Rise and fall time				
Count Pulse	t_{rfc}	-	4	µs
Reset Pulse	t_{rfr}	-	4	µs
test Count Pulse	t_{rftc}	-	80	µs
*Strobe Guard Band time (f_{SC} ≤ 100kHz)	t_{gb}	400	-	ns
*Strobe Guard Band time (100kHz ≤ f_{SC} ≤ 250kHz)	t_{gb}	200	-	ns
*Strobe Guard Band time (250kHz ≤ f_{SC} ≤ 500kHz) negative edge only	t_{gb}	200	-	ns

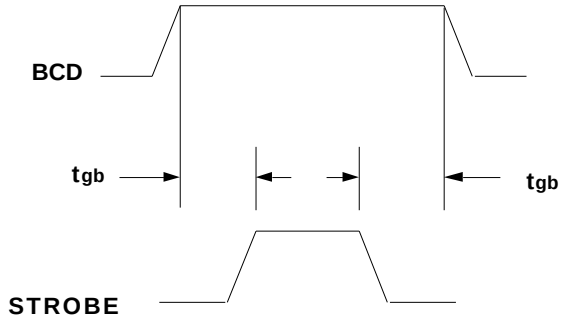

FIGURE 2. GUARD BANDED STROBE

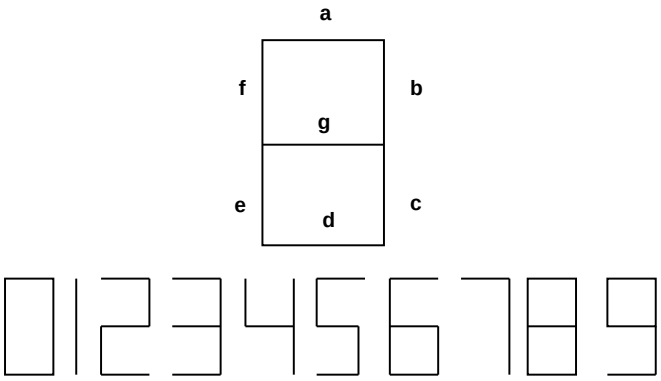

FIGURE 3. SEVEN SEGMENT FONT

TTL COMPATIBLE OUTPUTS:

POWER SUPPLIES: Vss = +5V ± 5%, V_{DD} = 0V, V_{GG} = -12V ± 5%

OUTPUT LEVELS: "1" Level ≥ Vss - 0.5V (sourcing 100µA)
"0" Level ≤ 0.4V (sinking 1.6mA) } $\overline{\text{BLANK}}$ AND BCD DATA OUTPUTS

"1" Level ≥ Vss - 0.5V (sourcing 40µA)
"0" Level ≤ 0.4V (sinking 0.18mA) } OVERFLOW OUTPUT

All other outputs as specified for single power supply, Vss = + 15V, operation.
Inputs as specified for single power supply, Vss = +5V ± 5% operation.

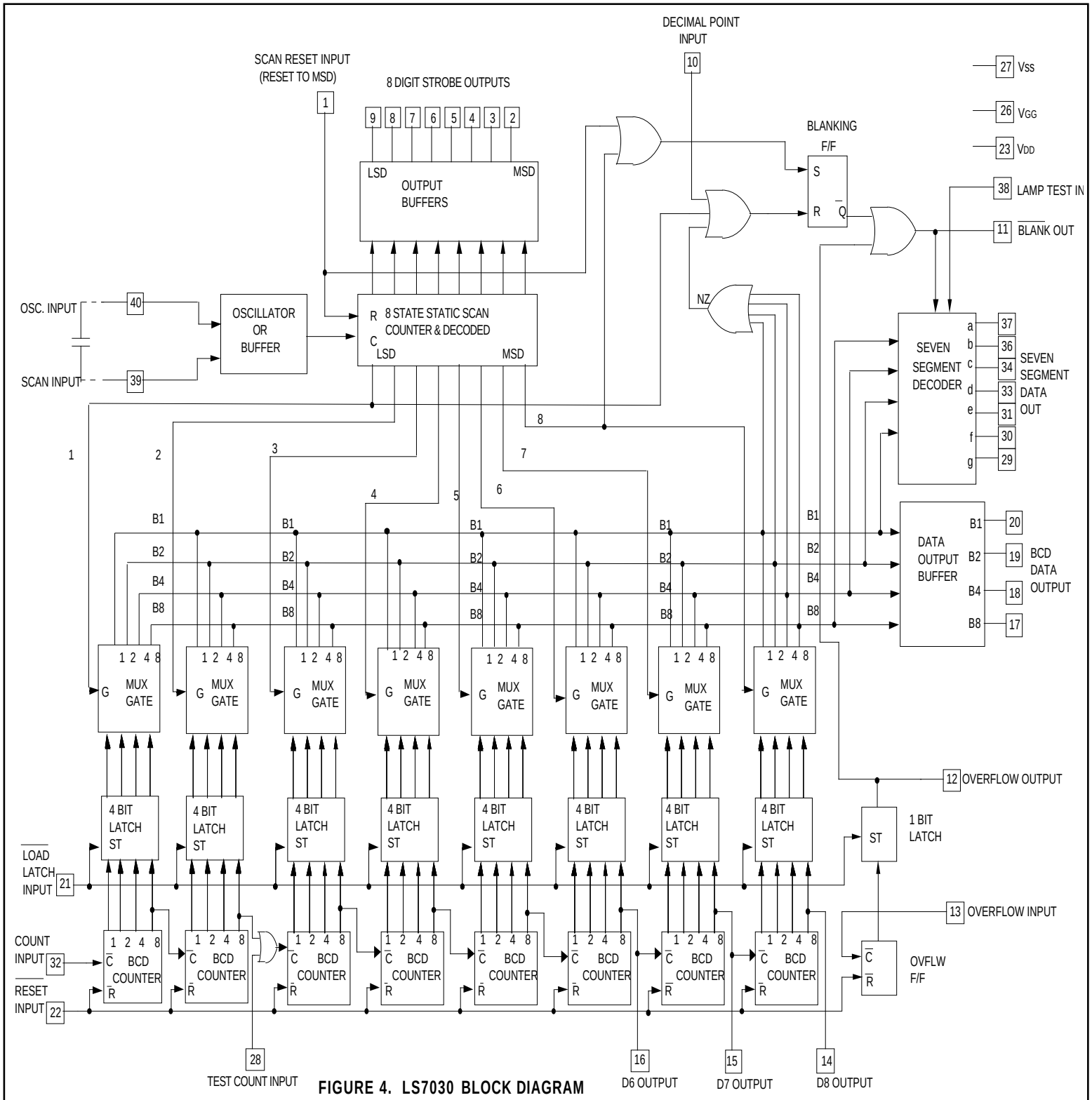

FIGURE 4. LS7030 BLOCK DIAGRAM

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