

LPM3400 - 20V/4.2A

N-Channel Enhancement Mode Field Effect Transistor

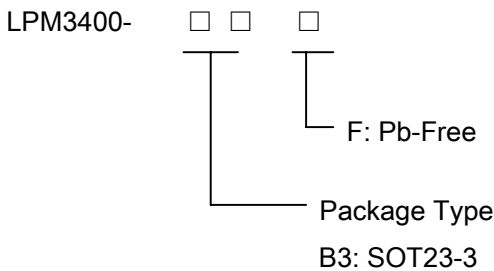
General Description

The LPM3400 is N-channel logic enhancement mode power field effect transistor, which are produced by using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suitable for low voltage applications, notebook computer power management and other battery powered circuits where high-side switching are needed.

Ordering Information



Features

- 20V/4.2A, RDC(ON)≤50mΩ(typ.)@VGS=4.5V
- 20V/3.9A, RDC(ON)≤63mΩ(typ.)@VGS=2.5V
- 20V/3.0A, RDC(ON)≤87mΩ(typ.)@VGS=1.8V
- Super high density cell design for extremely low RDC(ON)
- SOT23 Package

Applications

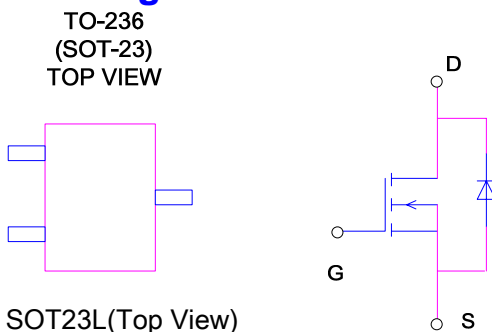
- ✧ Portable Media Players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

Marking Information

Device	Marking	Package	Shipping
LPM3400B3F	A2XXX	SOT23-3	3K/REEL

XXX : The production cycle and the batch.

Pin Configurations



Functional Pin Description

Name	Description
G	Gate Electrode
S	Source
D	Drain Electrode

Absolute Maximum Ratings

Absolute Maximum Ratings TA=25°C Unless Otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		VDS	20	V	
Gate-Source Voltage		VGS	±8	V	
Continuous Drain Current A	TA=25°C	ID	4.2	A	
	TA=70°C		3.2		
Pulsed Drain Current E		IDM	15		
Power Dissipation	TA=25°C	PO	1.4	W	
	TA=70°C		0.9		
Junction and Storage Temperature Range		TJ, TSTG	-55 to 150	°C	
Thermal Characteristics					
Parameter		Symbol	Typ.	Max.	Units
Maximum Junction-to-Ambient A	t ≤ 10S	RθJA	70	90	°C/W
Maximum Junction-to-Ambient A	Steady-state		100	125	°C/W
Maximum Junction-to-Lead C	Steady-state	RθJL	63	80	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
STATIC PARAMETER						
BVDSS	Drain-Source Breakdown Voltage	ID=250 μ A , VGS=0V	20			V
IDSS	Zero-Gate Voltage Drain Current	VDS=16V,VGS=0V TJ=55°C			1	μ A
					5	
IGSS	Gate-Body Leakage Current	VDS=0V,VGS= \pm 8V			100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=250 μ A	0.4	0.6	1	V
ID(ON)	On State Drain Current	VDS=5V,VGS=4.5V	15			A
RDS(ON)	Static Drain-Source On-Resistance	VGS=4.5V, ID=4.2 A TJ=125°C		41	50	m Ω
				58	70	
				52	63	m Ω
		VGS=1.8V, ID=3A		67	87	m Ω
gFS	Forward Transconductance	VDS=5V,ID=4.2A		11		S
VSD	Diode Forward Voltage	IS=1A,VGS=0V		0.76	1	V
IS	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	VDS=10V,VGS=0V f = 1MHz		436		pF
CDSS	Output Capacitance			66		pF
Crss	Reverse Transfer Capacitance			44		pF
Rg	Gate Resistance	VDS=0V,VGS=0V f = 1MHz		3		Ω
SWITCHING PARAMETERS						
Qg	Total Gate Charge	VDS=10V,VGS=4.5V ID=4.2A		6.2		nC
Qgs	Gate Source Charge			1.6		nC
Qgd	Gate Drain Charge			0.5		nC
t D(ON)	Turn-On Delay Time	VDS=10V,VGS=5V RL=2.7 Ω ,RGEN=6 Ω		5.5		nS
tr	Turn-On Rise Time			6.3		nS
t D(OFF)	Turn-Off Delay Time			40		nS
tf	Turn-Off Fall Time			12.7		nS
trr	Body-Diode Reverse Recovery Time	IF=4A,d I/dt=100/ μ S		12.3		nS
Qrr	Body-Diode Reverse Recovery Charge	IF=4A,d I/dt=100/ μ S		3.5		nC

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

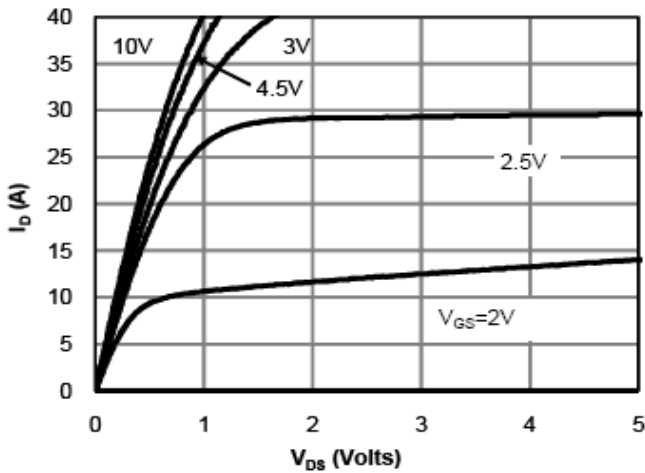


Fig 1: On-Region Characteristics (Note E)

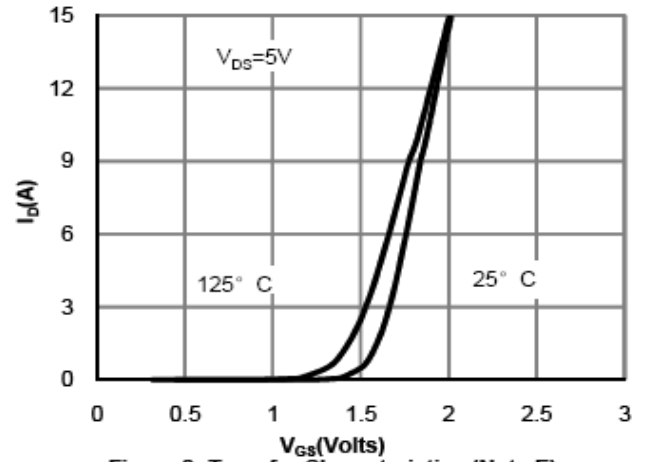


Figure 2: Transfer Characteristics (Note E)

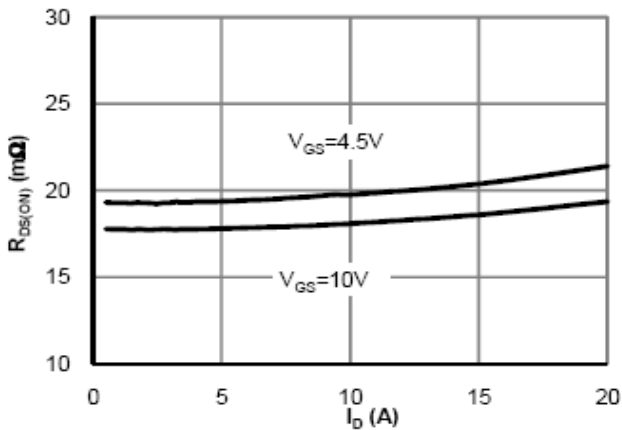


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

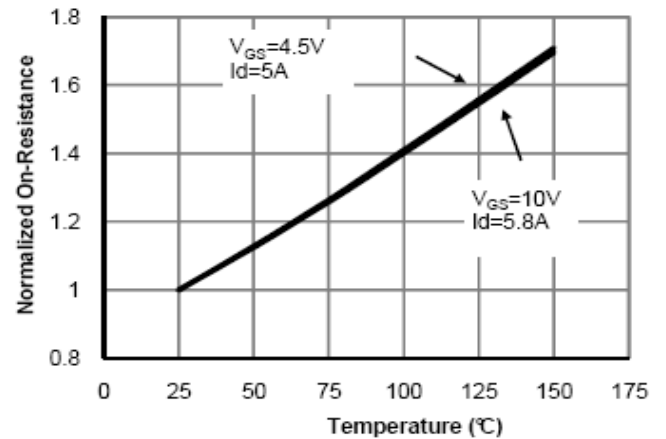


Figure 4: On-Resistance vs. Junction Temperature (Note E)

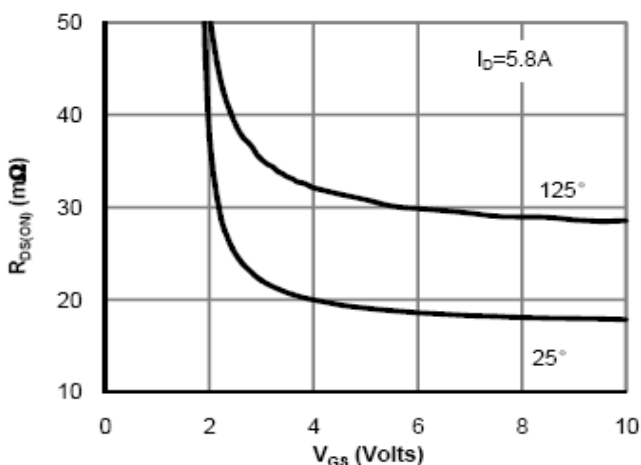


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

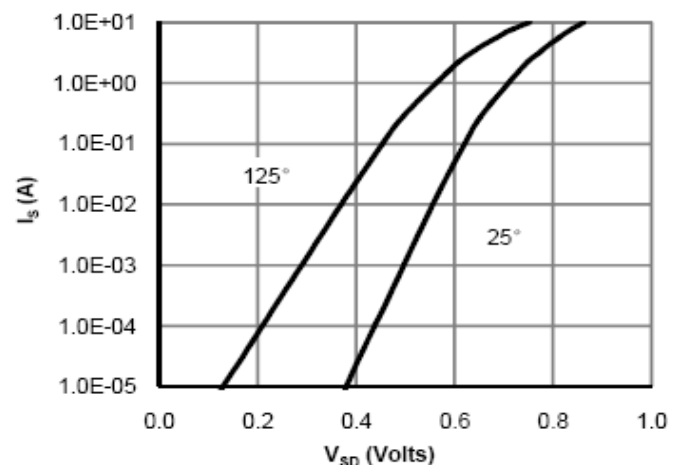


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

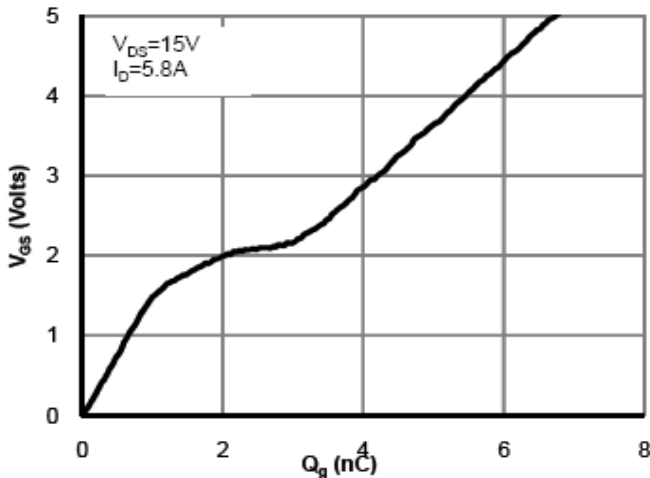


Figure 7: Gate-Charge Characteristics

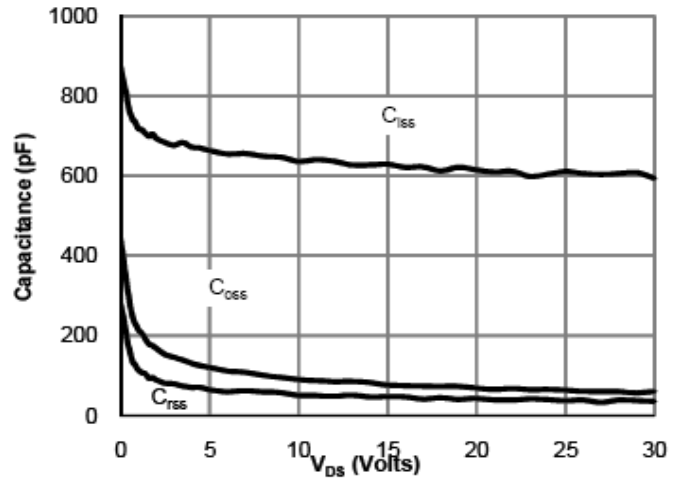


Figure 8: Capacitance Characteristics

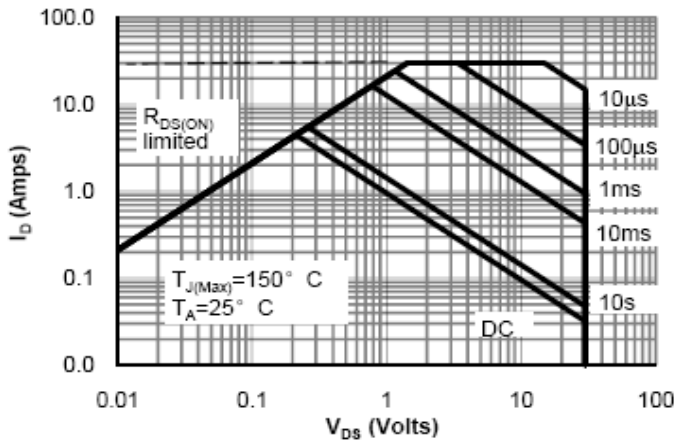


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

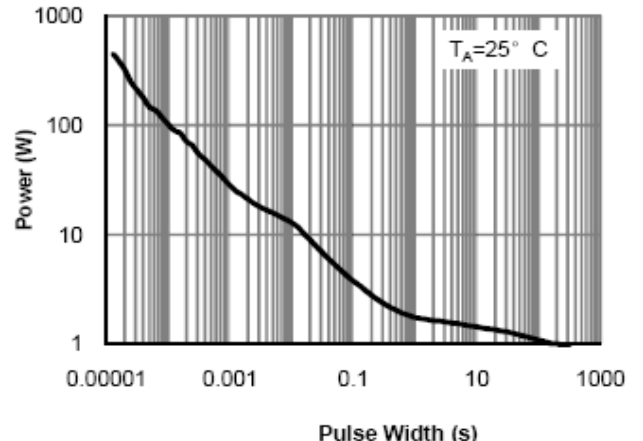


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

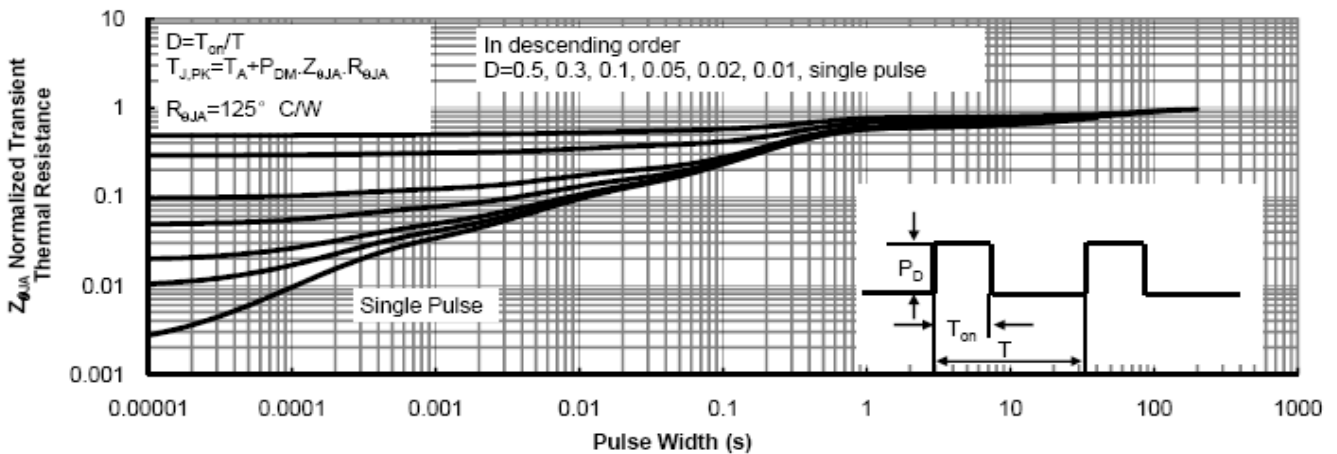
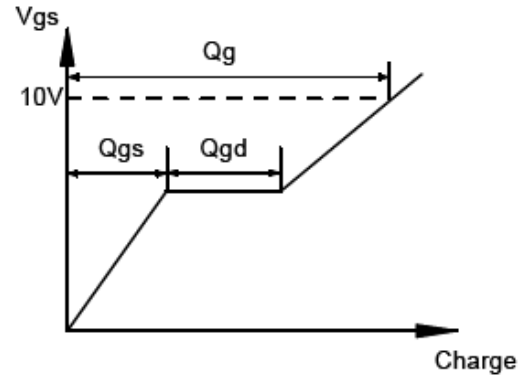
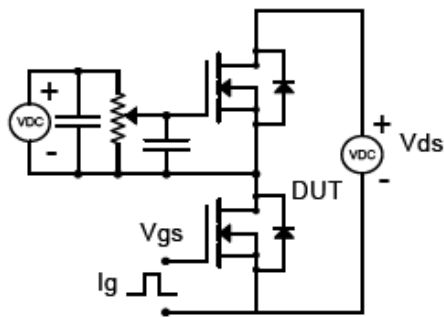
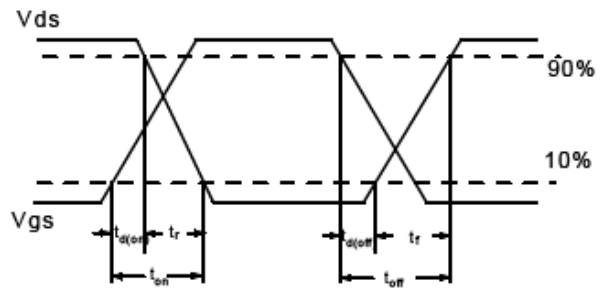
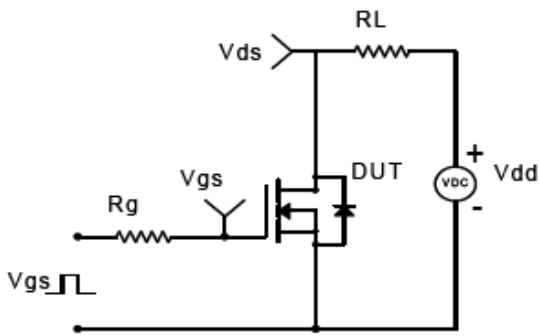


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

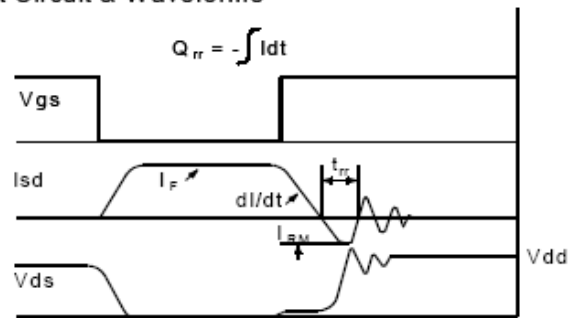
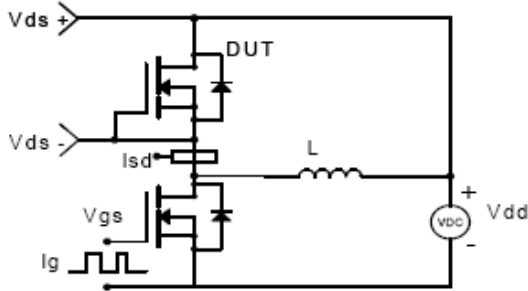
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

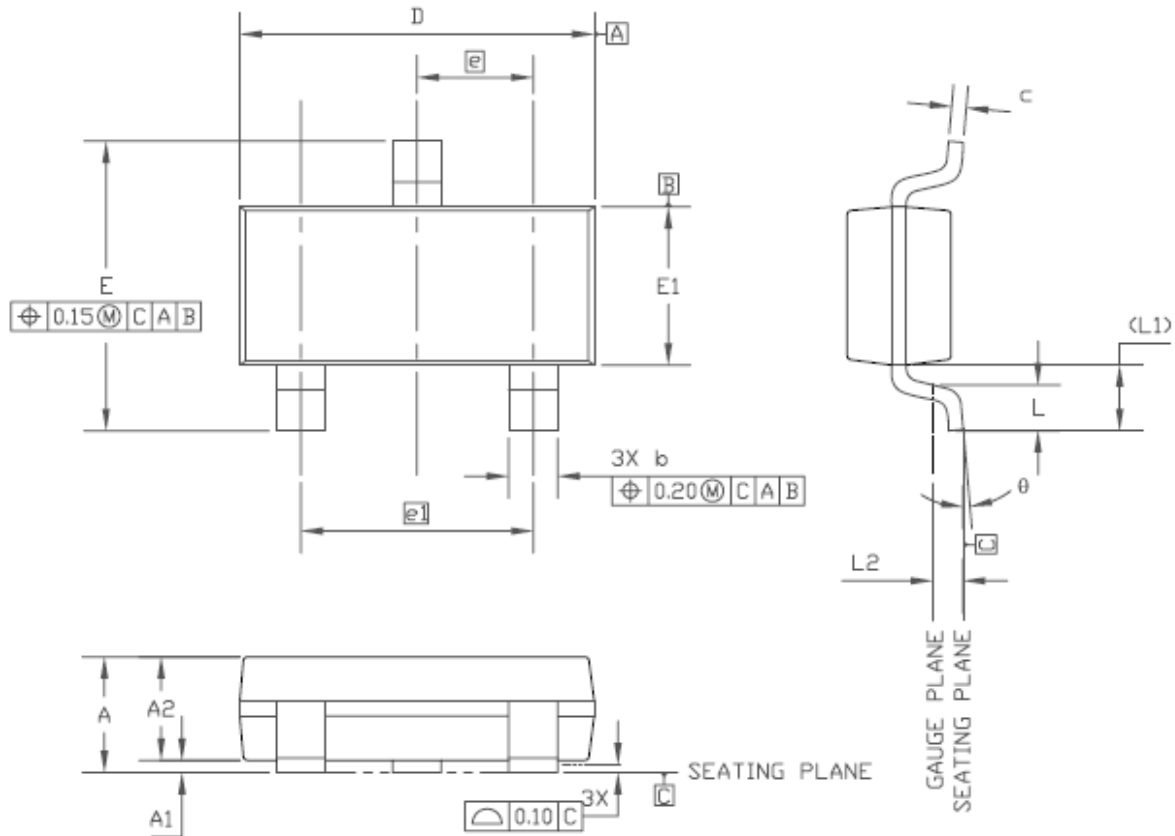


Diode Recovery Test Circuit & Waveforms

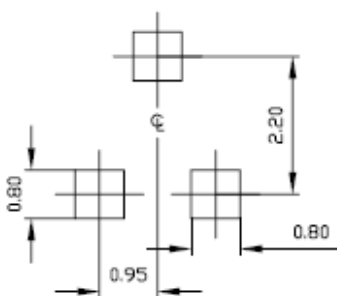


Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°