HM514258A Series

262,144-Word X 4-Bit CMOS Dynamic RAM

■ DESCRIPTION

The Hitachi HM514258A is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514258A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS technology and some new CMOS circuit design technologies. The HM514258A offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM514258A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

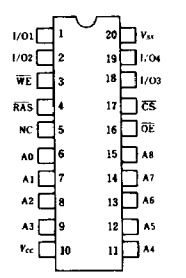
- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
  - Standby .....11 mW (max)
  - Active .....495 mW/440 mW/413 mW/358 mW/303 mW (max)
- Static Column Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CS}$ Before $\overline{RAS}$ Refresh

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514258AP-6	60 ns	300 mil 20-pin Plastic DIP (DP-20NA)
HM514258AP-7	70 ns	
HM514258AP-8	80 ns	
HM514258AP-10	100 ns	
HM514258AP-12	120 ns	
HM514258AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM514258AJP-7	70 ns	
HM514258AJP-8	80 ns	
HM514258AJP-10	100 ns	
HM514258AJP-12	120 ns	
HM514258AZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM514258AZP-7	70 ns	
HM514258AZP-8	80 ns	
HM514258AZP-10	100 ns	
HM514258AZP-12	120 ns	

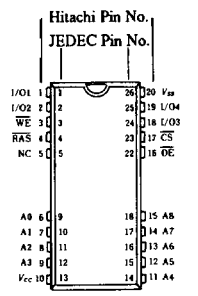
■ PIN OUT

HM514258AP Series



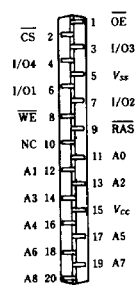
(Top View)

HM514258AJP Series



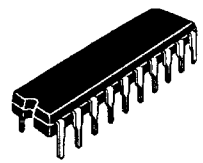
(Top View)

HM514258AZP Series



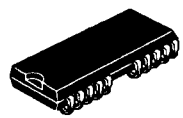
(Bottom View)

HM514258AP Series



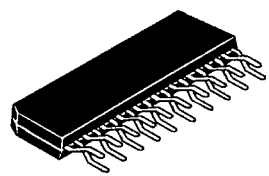
(DP-20NA)

HM514258AJP Series



(CP-20D)

HM514258AZP Series

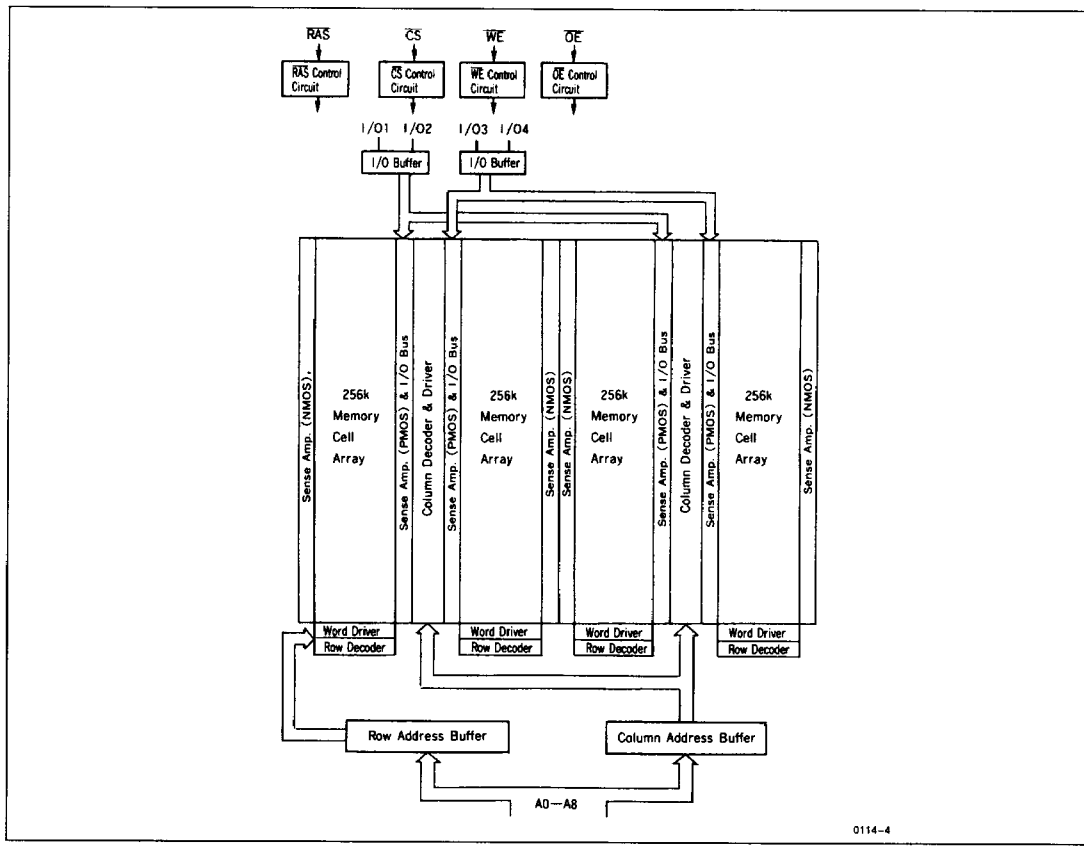


(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
I/O_0–I/O_4	Data Input/Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	I/O Pin	V_{IL}	− 1.0	—	0.8	V	1
	Others	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	75	—	65	—	55	mA	$\overline{RAS}$, $\overline{CS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1	mA	CMOS Interface, $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	75	—	65	—	55	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	80	—	70	—	65	—	55	—	45	mA	t_{RC} = Min	
Static Column Mode Current	I_{CC9}	—	80	—	70	—	65	—	55	—	45	mA	t_{SC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Input/Output Capacitance (Data Input, Data Output)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[17, 18]

Test Conditions

Input Rise and Fall Times: 5 ns
Input timing reference levels: 0.8V, 2.4V
Output load: 2 TTL Gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ Pulse Width	t_{SP}	20	10000	20	10000	25	10000	30	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASW}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{AHW}	15	—	15	—	20	—	25	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	70	25	90	ns	8
$\overline{RAS}$ Hold Time	t_{RSL}	20	—	20	—	25	—	30	—	30	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{SRS}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CS}$ Delay Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	1, 7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CS}$	t_{ACS}	—	20	—	20	—	25	—	30	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	50	—	55	ns	3, 5, 14
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	

Read Cycle (continued)

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to Column Address Hold Time	t_{AHR}	15	—	15	—	15	—	15	—	15	—	ns	16
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	50	20	65	ns	9
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	50	—	55	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	60	—	70	—	80	—	100	—	120	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Hold Time from Address	t_{AOH}	5	—	5	—	5	—	5	—	5	—	ns	
$\overline{CS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{CS}$ Hold Time from $\overline{OE}$	t_{OCH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{OE}$ Hold Time from $\overline{RAS}$	t_{ROH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{OE}$ Hold Time from $\overline{CS}$	t_{COH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{OE}$ Pulse Width	t_{OEP}	20	—	20	—	25	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	25	—	25	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	55	—	65	—	75	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
D_{in} Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
D_{in} Hold Time	t_{DH}	15	—	15	—	20	—	25	—	25	—	ns	11
D_{in} Hold Time to $\overline{RAS}$	t_{DHR}	55	—	65	—	75	—	95	—	115	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AWR}	55	—	65	—	75	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	93	—	110	—	135	—	160	—	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	65	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	85	—	95	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CS}$ Setup Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{ZRH}	10	—	10	—	10	—	10	—	10	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Static Column Mode Cycle Time	t_{SC}	35	—	40	—	45	—	55	—	60	—	ns	
Static Column Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSWD}	70	—	80	—	90	—	110	—	135	—	ns	
Static Column Mode $\overline{CS}$ Precharge Time	t_{SI}	10	—	10	—	10	—	10	—	15	—	ns	
Static Column Mode $\overline{WE}$ Precharge Time	t_{WI}	10	—	10	—	10	—	10	—	15	—	ns	

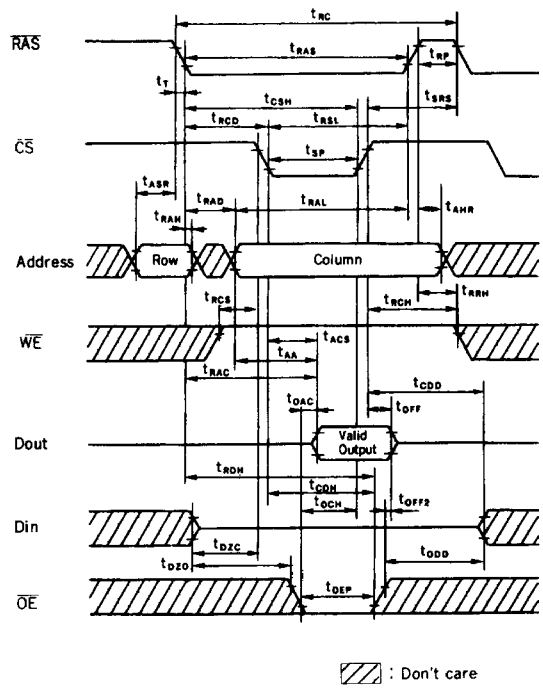
Static Column Mode Read-Modify-Write Cycle and Mixed Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Static Column Mode Cycle Time on Read-Modify-Write	t_{SRW}	90	—	100	—	120	—	140	—	160	—	ns	12
Access Time from First $\overline{WE}$	t_{ALW}	—	65	—	75	—	85	—	100	—	115	ns	3, 13
Last $\overline{WE}$ to Column Address Delay Time	t_{LWAD}	20	35	20	40	25	45	25	50	30	60	ns	15
Last $\overline{WE}$ to Column Address Hold Time	t_{AHLW}	65	—	75	—	85	—	100	—	115	—	ns	

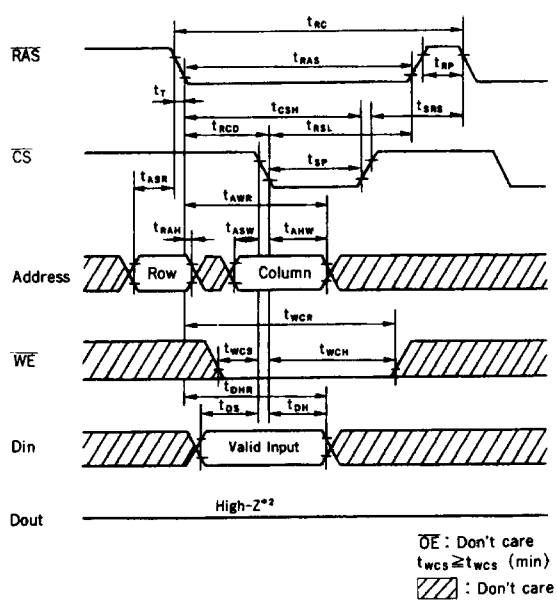
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T
13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} is defined as the time at which the column address hold is set.
17. An initial pause of 100 μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If internal refresh counter is used, eight or more $\overline{CS}$ before $\overline{RAS}$ refresh cycles are required.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

■ TIMING WAVEFORMS

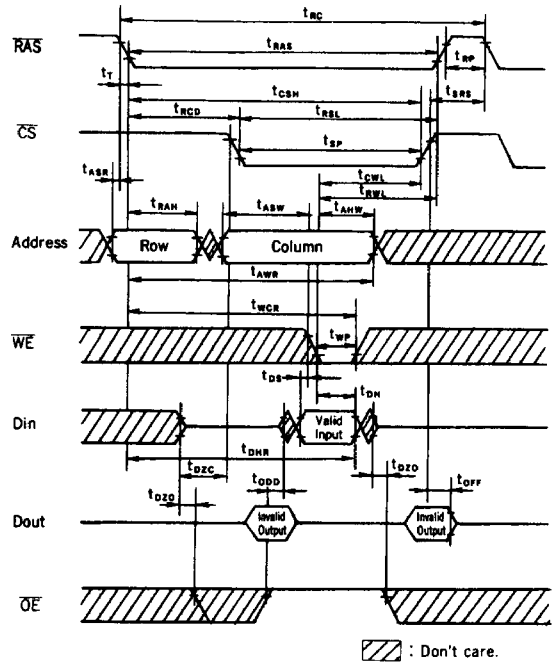
• Read Cycle



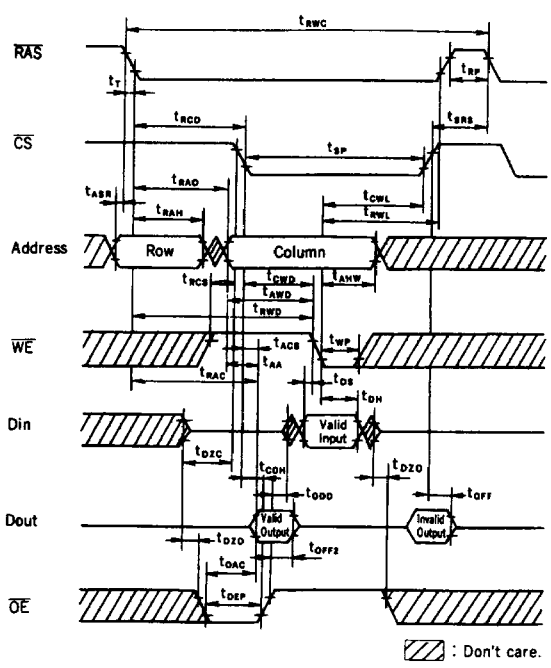
• Early Write Cycle



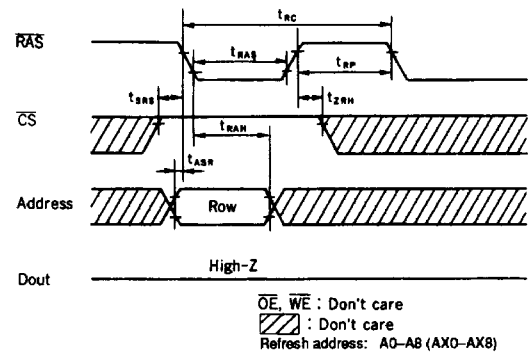
• **Delayed Write Cycle**



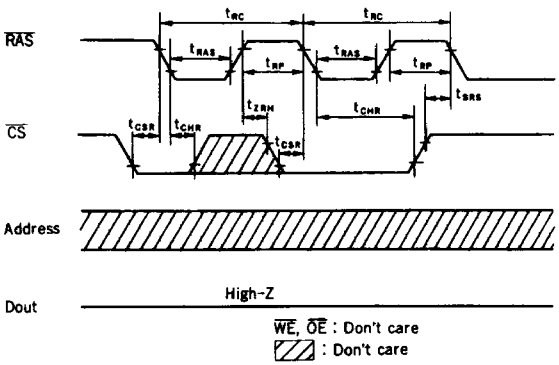
• **Read-Modify-Write Cycle**



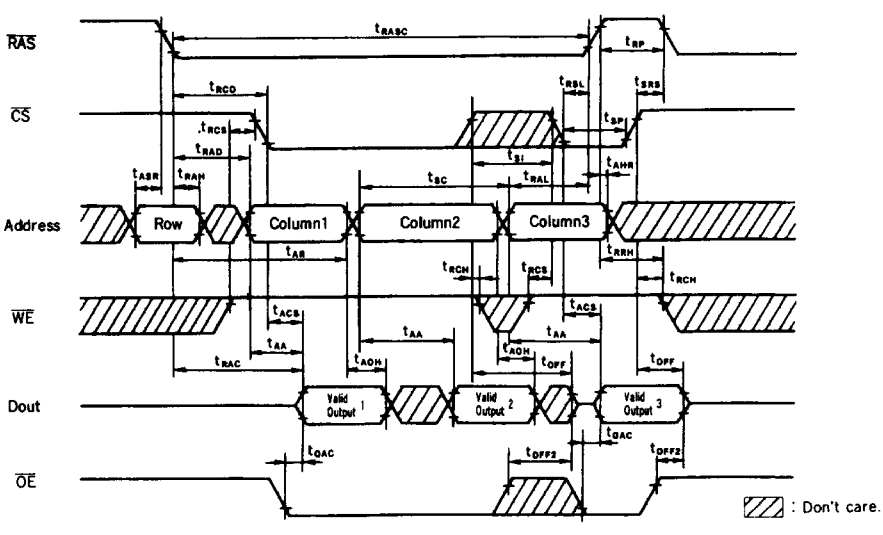
• $\overline{RAS}$ Only Refresh Cycle



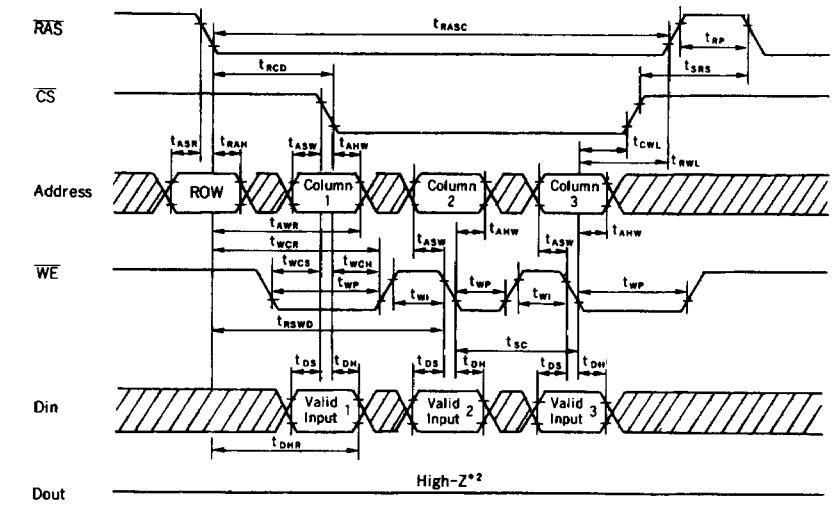
• $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



• Static Column Mode Read Cycle



• **Static Column Mode Write Cycle (1)**



1. ▨ : Don't care
2. $t_{WCS} \geqq t_{WCS}(min)$
3. $\overline{OE}$: Don't care

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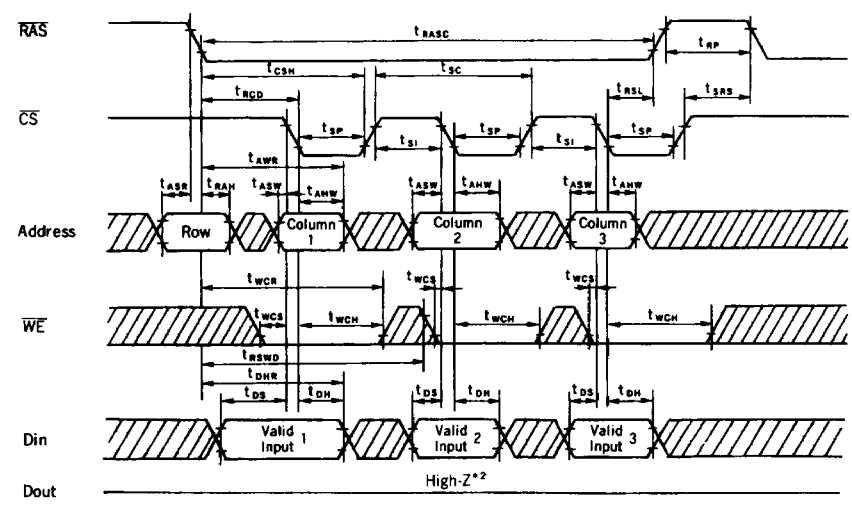
• **Static Column Mode Write Cycle (2)**



1. ▨ : Don't care.
2. $t_{WCS} \geqq t_{WCS}(min)$
3. $\overline{OE}$: Don't care.

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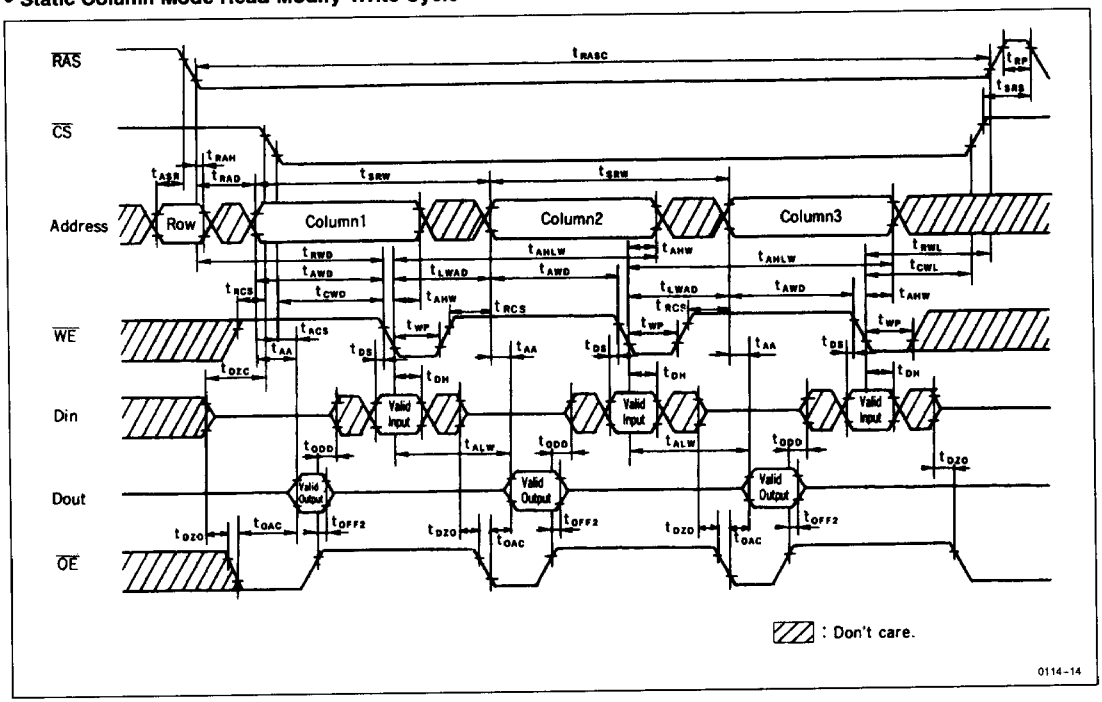
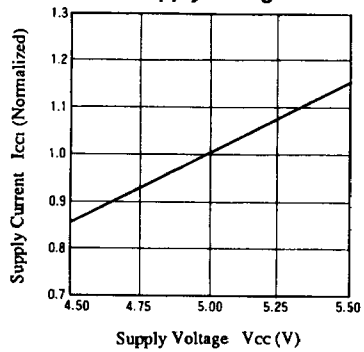
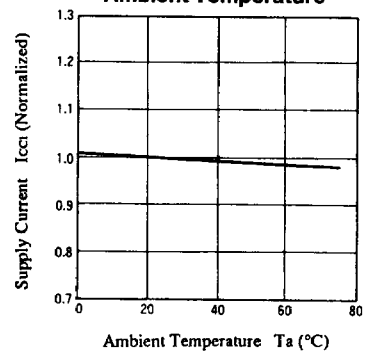
• **Static Column Mode Read-Modify-Write Cycle**



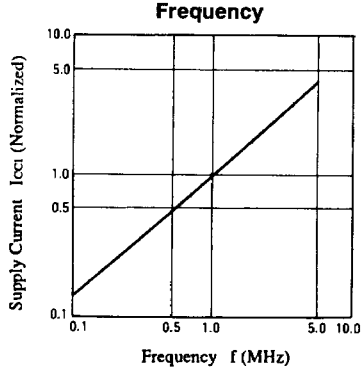
Supply Current (Active) vs Supply Voltage



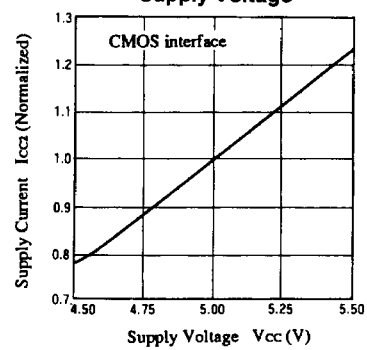
Supply Current (Active) vs Ambient Temperature



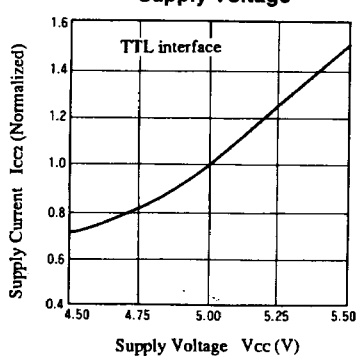
Supply Current (Active) vs Frequency



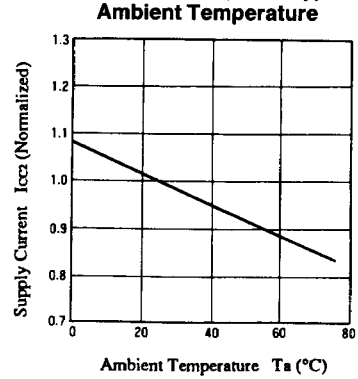
Supply Current (Standby) vs Supply Voltage



Supply Current (Standby) vs Supply Voltage



Supply Current (Standby) vs Ambient Temperature



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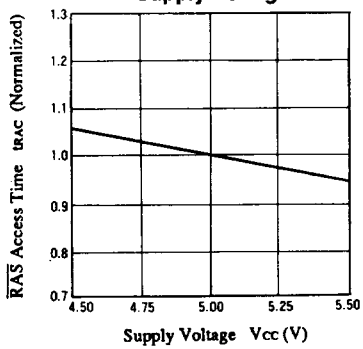
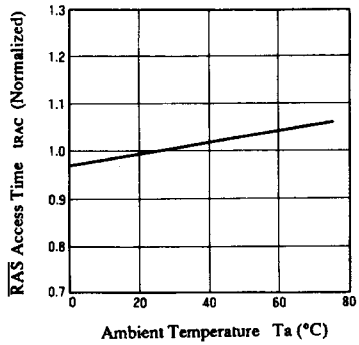
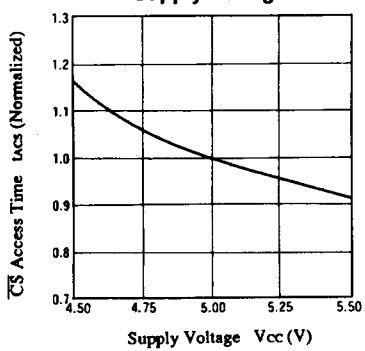
$\overline{RAS}$ Access Time vs Supply Voltage



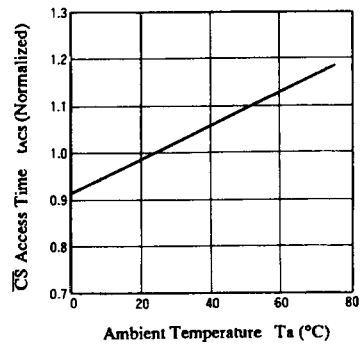
$\overline{RAS}$ Access Time vs Ambient Temperature



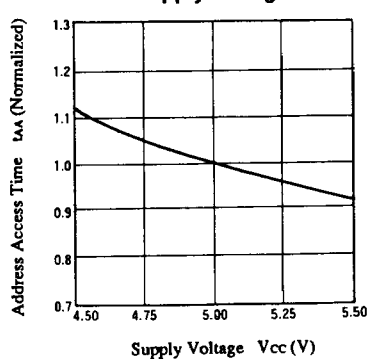
$\overline{CS}$ Access Time vs Supply Voltage



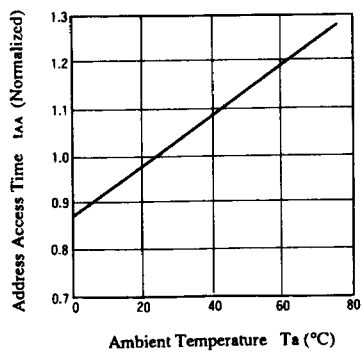
$\overline{CS}$ Access Time vs Ambient Temperature



Address Access Time vs Supply Voltage



Address Access Time vs Ambient Temperature



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