# Ultralow Noise, High Accuracy Voltage References

Data Sheet **ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550**

## FEATURES

- **Maximum temperature coefficient ($TCV_{OUT}$): 2 ppm/°C**
- **Output noise (0.1 Hz to 10 Hz)**
  - **Less than 1 µV p-p at $V_{OUT}$ of 2.048 V typical**
- **Initial output voltage error: ±0.02% (maximum)**
- **Input voltage range: 3 V to 15 V**
- **Operating temperature: −40°C to +125°C**
- **Output current: +10 mA source/−10 mA sink**
- **Low quiescent current: 950 µA (maximum)**
- **Low dropout voltage: 300 mV at 2 mA ($V_{OUT}$ ≥ 3 V)**
- **8-lead SOIC package**

## APPLICATIONS

- **Precision data acquisition systems**
- **High resolution data converters**
- **High precision measurement devices**
- **Industrial instrumentation**
- **Medical devices**
- **Automotive battery monitoring**

## GENERAL DESCRIPTION

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 devices are high precision, low power, low noise voltage references featuring ±0.02% maximum initial error, excellent temperature stability, and low output noise.

This family of voltage references uses an innovative core topology to achieve high accuracy while offering industry-leading temperature stability and noise performance. The low, thermally induced output voltage hysteresis and low long-term output voltage drift of the devices also improve system accuracy over time and temperature variations.

A maximum operating current of 950 µA and a maximum low dropout voltage of 300 mV allow the devices to function very well in portable equipment.

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 series of references is provided in an 8-lead SOIC package and is available in a wide range of output voltages, all of which are specified over the extended industrial temperature range of −40°C to +125°C.

## PIN CONFIGURATION

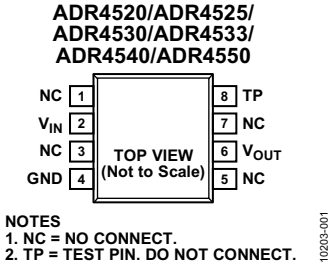


*Figure 1. 8-Lead SOIC*

**Table 1. Selection Guide**

| Model | Output Voltage (V) |
|---|---|
| ADR4520 | 2.048 |
| ADR4525 | 2.5 |
| ADR4530 | 3.0 |
| ADR4533 | 3.3 |
| ADR4540 | 4.096 |
| ADR4550 | 5.0 |

**Table 2. Voltage Reference Choices from Analog Devices**

| $V_{OUT}$ (V) | Low Cost/ Low Power | Micropower | Ultralow Noise | High Voltage, High Performance |
|---|---|---|---|---|
| 2.048 | ADR360<br>ADR3420 | REF191 | ADR430<br>ADR440 | |
| 2.5 | ADR3425<br>AD1582<br>ADR361 | ADR291<br>REF192 | ADR431<br>ADR441 | ADR03<br>AD780 |
| 5.0 | ADR3450<br>AD1585<br>ADR365 | ADR293<br>REF195 | ADR435<br>ADR445 | ADR02<br>AD586 |

**Rev. 0**



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## REVISION HISTORY

**4/12—Revision 0: Initial Version**

# SPECIFICATIONS

## ADR4520 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 3 V to 15 V, $I_L$ = 0 mA, $T_A$ = 25°C.

**Table 3.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | 2.048 | | V |
| INITIAL OUTPUT VOLTAGE ERROR | $V_{OUT\_ERR}$ | B grade | | | ±0.02 | % |
| | | | | | 410 | µV |
| | | A grade | | | ±0.04 | % |
| | | | | | 820 | µV |
| SOLDER HEAT SHIFT | | | | ±0.02 | | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | B grade, −40°C ≤ $T_A$ ≤ +125°C | | | 2 | ppm/°C |
| | | A grade, −40°C ≤ $T_A$ ≤ +125°C | | | 4 | ppm/°C |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 10 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C | | 30 | 80 | ppm/mA |
| | | $I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C | | 100 | 120 | ppm/mA |
| QUIESCENT CURRENT | $I_Q$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | 700 | 950 | µA |
| DROPOUT VOLTAGE | $V_{DO}$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | | 1 | V |
| | | −40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA | | | 1 | V |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | 90 | | dB |
| OUTPUT CURRENT CAPACITY | $I_L$ | | | | | |
| Sinking | | | | | −8 | mA |
| Sourcing | | | | | 10 | mA |
| OUTPUT VOLTAGE NOISE | $e_{Np-p}$ | 0.1 Hz to 10.0 Hz | | 1.0 | | µV p-p |
| OUTPUT VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 35.8 | | nV/√Hz |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{OUT\_HYS}$ | $T_A$ = temperature cycled from +25°C to −40°C to +125°C and back to +25°C | | 50 | | ppm |
| LONG-TERM DRIFT | $\Delta V_{OUT\_LTD}$ | 1000 hours at 60°C | | 25 | | ppm |
| TURN-ON SETTLING TIME | $t_R$ | $I_L$ = 0 mA, $C_L$ = 1 µF, $C_{IN}$ = 0.1 µF, $R_L$ = 1 kΩ | | 90 | | µs |
| LOAD CAPACITANCE | | | 1 | | 100 | µF |

## ADR4525 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 3 V to 15 V, $I_L$ = 0 mA, $T_A$ = 25°C.

**Table 4.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | 2.500 | | V |
| INITIAL OUTPUT VOLTAGE ERROR | $V_{OUT\_ERR}$ | B grade | | | ±0.02 | % |
| | | | | | 500 | µV |
| | | A grade | | | ±0.04 | % |
| | | | | | 1 | mV |
| SOLDER HEAT SHIFT | | | | ±0.02 | | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | B grade, −40°C ≤ $T_A$ ≤ +125°C | | | 2 | ppm/°C |
| | | A grade, −40°C ≤ $T_A$ ≤ +125°C | | | 4 | ppm/°C |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 10 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C | | 30 | 80 | ppm/mA |
| | | $I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C | | 60 | 120 | ppm/mA |
| QUIESCENT CURRENT | $I_Q$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | 700 | 950 | µA |
| DROPOUT VOLTAGE | $V_{DO}$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | | 500 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA | | | 500 | mV |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | 90 | | dB |
| OUTPUT CURRENT CAPACITY | $I_L$ | | | | | |
| Sinking | | | | | −10 | mA |
| Sourcing | | | | | 10 | mA |
| OUTPUT VOLTAGE NOISE | $e_{NP-P}$ | 0.1 Hz to 10.0 Hz | | 1.25 | | µV p-p |
| OUTPUT VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 41.3 | | nV/√Hz |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{OUT\_HYS}$ | $T_A$ = temperature cycled from +25°C to −40°C to +125°C and back to +25°C | | 50 | | ppm |
| LONG-TERM DRIFT | $\Delta V_{OUT\_LTD}$ | 1000 hours at 60°C | | 25 | | ppm |
| TURN-ON SETTLING TIME | $t_R$ | $I_L$ = 0 mA, $C_L$ = 1 µF, $C_{IN}$ = 0.1 µF, $R_L$ = 1 kΩ | | 125 | | µs |
| LOAD CAPACITANCE | | | 1 | | 100 | µF |

## ADR4530 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 3.1 V to 15 V, $I_L$ = 0 mA, $T_A$ = 25°C.

**Table 5.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | 3.000 | | V |
| INITIAL OUTPUT VOLTAGE ERROR | $V_{OUT\_ERR}$ | B grade | | | ±0.02 | % |
| | | | | | 600 | µV |
| | | A grade | | | ±0.04 | % |
| | | | | | 1.2 | mV |
| SOLDER HEAT SHIFT | | | | ±0.02 | | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | B grade, −40°C ≤ $T_A$ ≤ +125°C | | | 2 | ppm/°C |
| | | A grade, −40°C ≤ $T_A$ ≤ +125°C | | | 4 | ppm/°C |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 10 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C | | 30 | 80 | ppm/mA |
| | | $I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C | | 60 | 120 | ppm/mA |
| QUIESCENT CURRENT | $I_Q$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | 700 | 950 | µA |
| DROPOUT VOLTAGE | $V_{DO}$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | | 100 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA | | | 300 | mV |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | 90 | | dB |
| OUTPUT CURRENT CAPACITY | $I_L$ | | | | | |
| Sinking | | | | | −10 | mA |
| Sourcing | | | | | 10 | mA |
| OUTPUT VOLTAGE NOISE | $e_{Np-p}$ | 0.1 Hz to 10.0 Hz | | 1.6 | | µV p-p |
| OUTPUT VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 60 | | nV/√Hz |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{OUT\_HYS}$ | $T_A$ = temperature cycled from +25°C to −40°C to +125°C and back to +25°C | | 50 | | ppm |
| LONG-TERM DRIFT | $\Delta V_{OUT\_LTD}$ | 1000 hours at 60°C | | 25 | | ppm |
| TURN-ON SETTLING TIME | $t_R$ | $I_L$ = 0 mA, $C_L$ = 0.1 µF, $C_{IN}$ = 0.1 µF, $R_L$ = 1 kΩ | | 130 | | µs |
| LOAD CAPACITANCE | | | 0.1 | | 100 | µF |

## ADR4533 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 3.4 V to 15 V, $I_L$ = 0 mA, $T_A$ = 25°C.

**Table 6.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | 3.300 | | V |
| INITIAL OUTPUT VOLTAGE ERROR | $V_{OUT\_ERR}$ | B grade | | | ±0.02 | % |
| | | | | | 660 | µV |
| | | A grade | | | ±0.04 | % |
| | | | | | 1.32 | mV |
| SOLDER HEAT SHIFT | | | | ±0.02 | | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | B grade, −40°C ≤ $T_A$ ≤ +125°C | | | 2 | ppm/°C |
| | | A grade, −40°C ≤ $T_A$ ≤ +125°C | | | 4 | ppm/°C |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 10 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C | | 30 | 80 | ppm/mA |
| | | $I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C | | 60 | 120 | ppm/mA |
| QUIESCENT CURRENT | $I_Q$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | 700 | 950 | µA |
| DROPOUT VOLTAGE | $V_{DO}$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | | 100 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA | | | 300 | mV |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ =1 kHz | | 90 | | dB |
| OUTPUT CURRENT CAPACITY | $I_L$ | | | | | |
| Sinking | | | | | −10 | mA |
| Sourcing | | | | | 10 | mA |
| OUTPUT VOLTAGE NOISE | $e_{NP-P}$ | 0.1 Hz to 10.0 Hz | | 2.1 | | µV p-p |
| OUTPUT VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 64.2 | | nV/√Hz |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{OUT\_HYS}$ | $T_A$ = temperature cycled from +25°C to −40°C to +125°C and back to +25°C | | 50 | | ppm |
| LONG-TERM DRIFT | $\Delta V_{OUT\_LTD}$ | 1000 hours at 60°C | | 25 | | ppm |
| TURN-ON SETTLING TIME | $t_R$ | $I_L$ = 0 mA, $C_L$ = 0.1 µF, $C_{IN}$ = 0.1 µF, $R_L$ = 1 kΩ | | 135 | | µs |
| LOAD CAPACITANCE | | | 0.1 | | 100 | µF |

## ADR4540 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 4.2 V to 15 V, $I_L$ = 0 mA, $T_A$ = 25°C.

**Table 7.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | 4.096 | | V |
| INITIAL OUTPUT VOLTAGE ERROR | $V_{OUT\_ERR}$ | B grade | | | ±0.02 | % |
| | | | | | 820 | µV |
| | | A grade | | | ±0.04 | % |
| | | | | | 1.64 | mV |
| SOLDER HEAT SHIFT | | | | ±0.02 | | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | B grade, −40°C ≤ $T_A$ ≤ +125°C | | | 2 | ppm/°C |
| | | A grade, −40°C ≤ $T_A$ ≤ +125°C | | | 4 | ppm/°C |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 10 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C | | 25 | 80 | ppm/mA |
| | | $I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C | | 50 | 120 | ppm/mA |
| QUIESCENT CURRENT | $I_Q$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | 700 | 950 | µA |
| DROPOUT VOLTAGE | $V_{DO}$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | | 100 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA | | | 300 | mV |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | 90 | | dB |
| OUTPUT CURRENT CAPACITY | $I_L$ | | | | | |
| Sinking | | | | | −10 | mA |
| Sourcing | | | | | 10 | mA |
| OUTPUT VOLTAGE NOISE | $e_{Np-p}$ | 0.1 Hz to 10.0 Hz | | 2.7 | | µV p-p |
| OUTPUT VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 83.5 | | nV/√Hz |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{OUT\_HYS}$ | $T_A$ = temperature cycled from +25°C to −40°C to +125°C and back to +25°C | | 50 | | ppm |
| LONG-TERM DRIFT | $\Delta V_{OUT\_LTD}$ | 1000 hours at 60°C | | 25 | | ppm |
| TURN-ON SETTLING TIME | $t_R$ | $I_L$ = 0 mA, $C_L$ = 0.1 µF, $C_{IN}$ = 0.1 µF, $R_L$ = 1 kΩ | | 155 | | µs |
| LOAD CAPACITANCE | | | 0.1 | | 100 | µF |

## ADR4550 ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $V_{IN}$ = 5.1 V to 15 V, $I_L$ = 0 mA, $T_A$ = 25°C.

**Table 8.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | $V_{OUT}$ | | | 5.000 | | V |
| INITIAL OUTPUT VOLTAGE ERROR | $V_{OUT\_ERR}$ | B grade | | | ±0.02 | % |
| | | | | | 1 | mV |
| | | A grade | | | ±0.04 | % |
| | | | | | 2 | mV |
| SOLDER HEAT SHIFT | | | | ±0.02 | | % |
| TEMPERATURE COEFFICIENT | $TCV_{OUT}$ | B grade, −40°C ≤ $T_A$ ≤ +125°C | | | 2 | ppm/°C |
| | | A grade, −40°C ≤ $T_A$ ≤ +125°C | | | 4 | ppm/°C |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 10 | ppm/V |
| LOAD REGULATION | $\Delta V_{OUT}/\Delta I_L$ | $I_L$ = 0 mA to +10 mA source, −40°C ≤ $T_A$ ≤ +125°C | | 25 | 80 | ppm/mA |
| | | $I_L$ = 0 mA to −10 mA sink, −40°C ≤ $T_A$ ≤ +125°C | | 35 | 120 | ppm/mA |
| QUIESCENT CURRENT | $I_Q$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | 700 | 950 | µA |
| DROPOUT VOLTAGE | $V_{DO}$ | −40°C ≤ $T_A$ ≤ +125°C, no load | | | 100 | mV |
| | | −40°C ≤ $T_A$ ≤ +125°C, $I_L$ = 2 mA | | | 300 | mV |
| RIPPLE REJECTION RATIO | RRR | $f_{IN}$ = 1 kHz | | 90 | | dB |
| OUTPUT CURRENT CAPACITY | $I_L$ | | | | | |
| Sinking | | | | | −10 | mA |
| Sourcing | | | | | 10 | mA |
| OUTPUT VOLTAGE NOISE | $e_{NP-P}$ | 0.1 Hz to 10.0 Hz | | 2.8 | | µV p-p |
| OUTPUT VOLTAGE NOISE DENSITY | $e_N$ | 1 kHz | | 95.3 | | nV/√Hz |
| OUTPUT VOLTAGE HYSTERESIS | $\Delta V_{OUT\_HYS}$ | $T_A$ = temperature cycled from +25°C to −40°C to +125°C and back to +25°C | | 50 | | ppm |
| LONG-TERM DRIFT | $\Delta V_{OUT\_LTD}$ | 1000 hours at 60°C | | 25 | | ppm |
| TURN-ON SETTLING TIME | $t_R$ | $I_L$ = 0 mA, $C_L$ = 0.1 µF, $C_{IN}$ = 0.1 µF, $R_L$ = 1 kΩ | | 160 | | µs |
| LOAD CAPACITANCE | | | 0.1 | | 100 | µF |

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 9.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 16 V |
| Operating Temperature Range | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature Range | −65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions; that is, a device soldered in a circuit board for surface-mount packages.

**Table 10. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead SOIC | 120 | 42 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

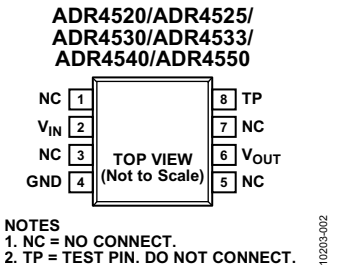



*Figure 2. Pin Configuration*

**Table 11. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | NC | No Connect. This pin is not connected internally. |
| 2 | $V_{IN}$ | Input Voltage Connection. |
| 3 | NC | No Connect. This pin is not connected internally. |
| 4 | GND | Ground. |
| 5 | NC | No Connect. This pin is not connected internally. |
| 6 | $V_{OUT}$ | Output Voltage. |
| 7 | NC | No Connect. This pin is not connected internally. |
| 8 | TP | Test Pin. Do not connect. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

## ADR4520

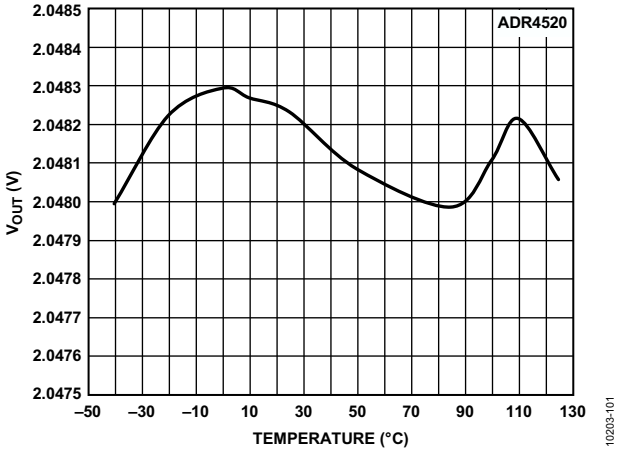



Figure 3. ADR4520 Output Voltage vs. Temperature

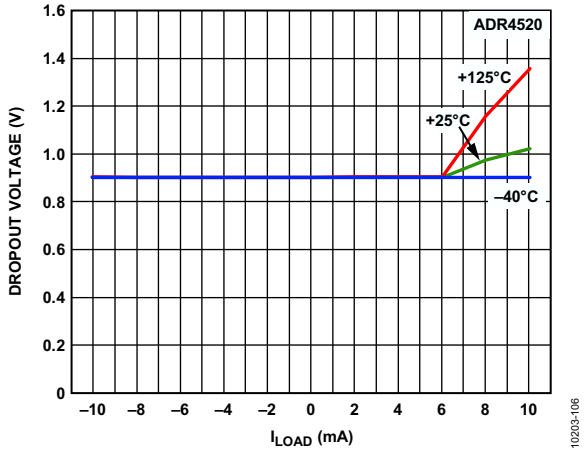



Figure 6. ADR4520 Dropout Voltage vs. Load Current

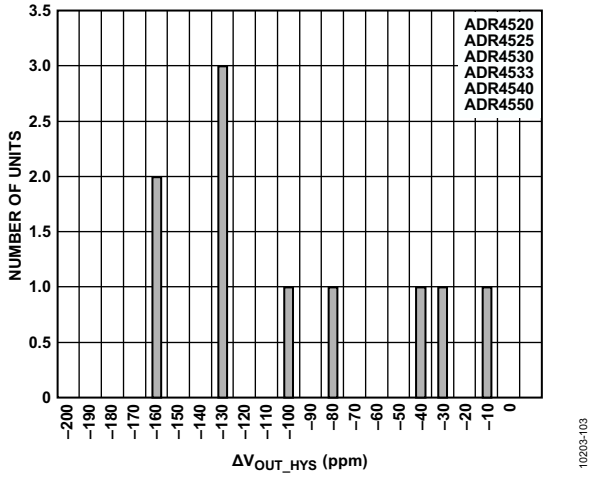



Figure 4. ADR4520 Thermally Induced Output Voltage Hysteresis Distribution

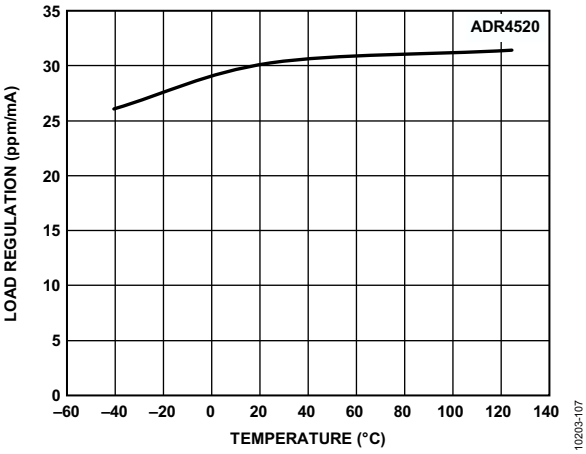



Figure 7. ADR4520 Load Regulation vs. Temperature (Sourcing)

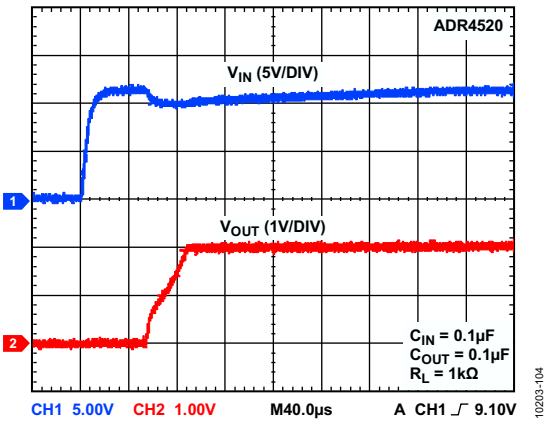



Figure 5. ADR4520 Output Voltage Start-Up Response

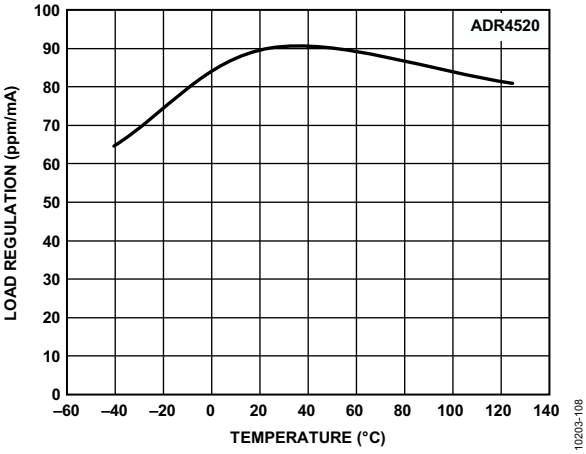



Figure 8. ADR4520 Load Regulation vs. Temperature (Sinking)

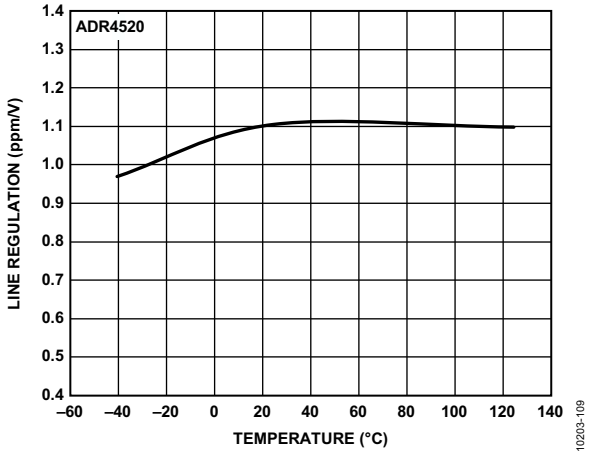



Figure 9. ADR4520 Line Regulation vs. Temperature

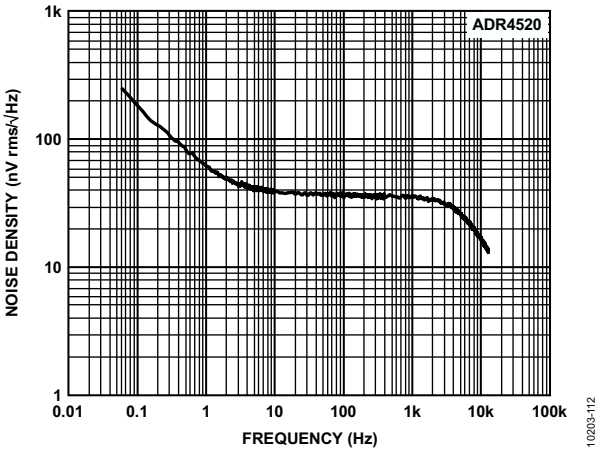



Figure 12. ADR4520 Output Noise Spectral Density

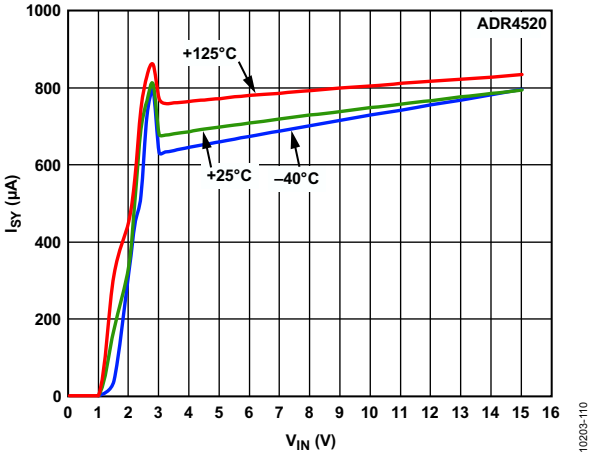



Figure 10. ADR4520 Supply Current vs. Supply Voltage

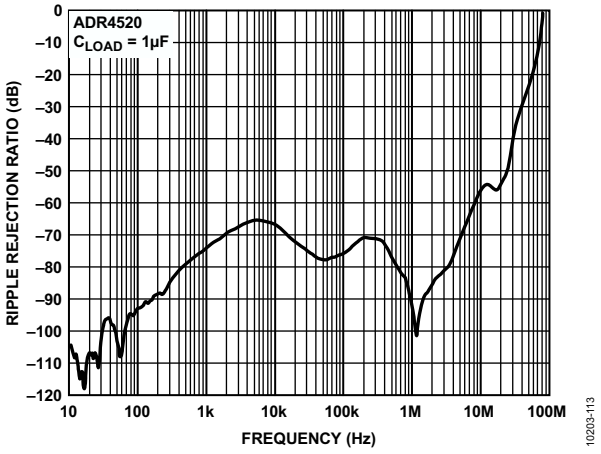



Figure 13. ADR4520 Ripple Rejection Ratio vs. Frequency

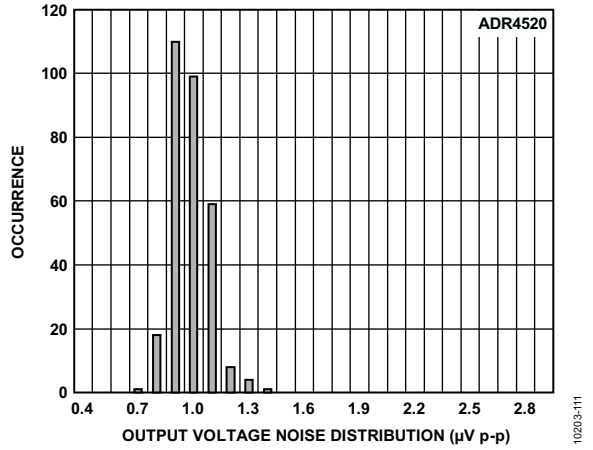



Figure 11. ADR4520 Output Voltage Noise
(Maximum Amplitude from 0.1 Hz to 10 Hz)

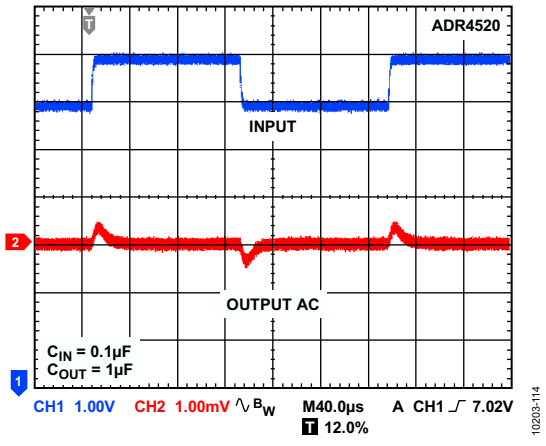



Figure 14. ADR4520 Line Transient Response

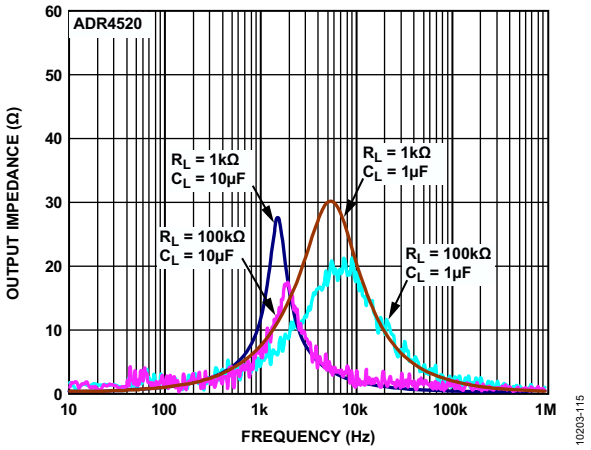



Figure 15. ADR4520 Output Impedance vs. Frequency

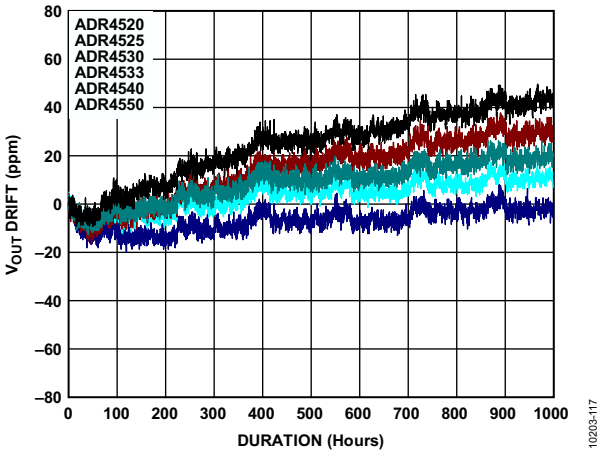



Figure 17. ADR4520 Typical Long-Term Output Voltage Drift (1000 Hours)

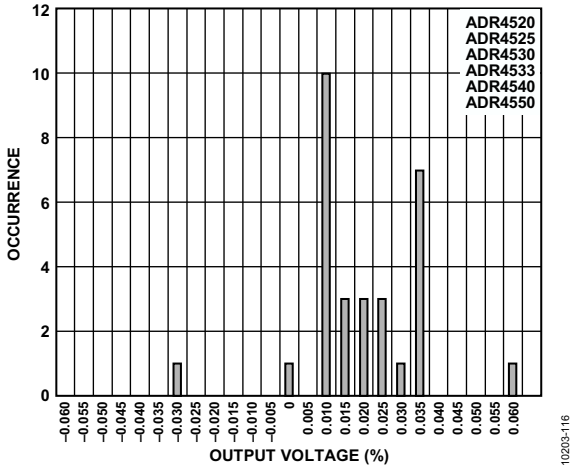



Figure 16. ADR4520 Output Voltage Drift Distribution After Reflow (SHR Drift)

## ADR4525

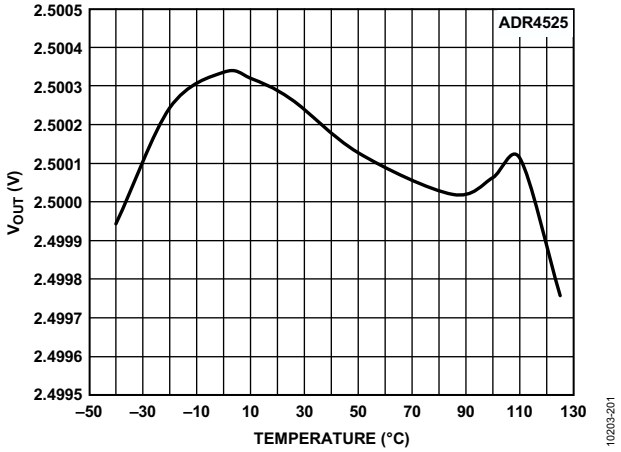



Figure 18. ADR4525 Output Voltage vs. Temperature

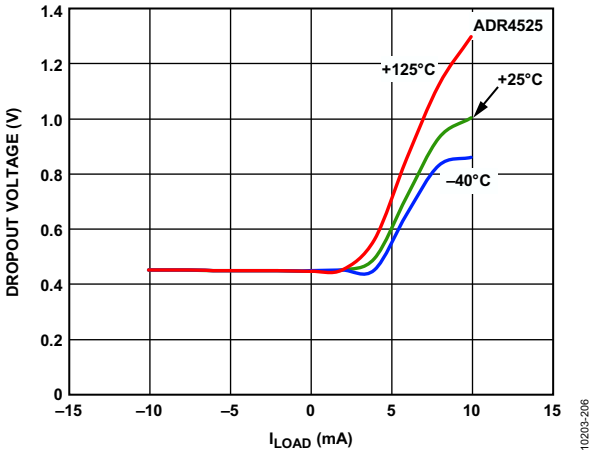



Figure 21. ADR4525 Dropout Voltage vs. Load Current

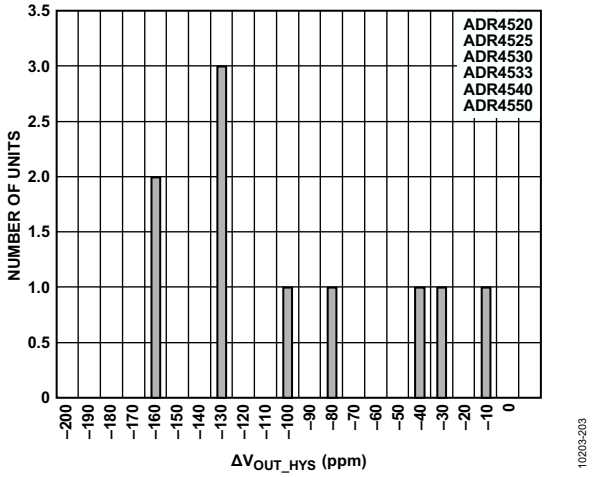



Figure 19. ADR4525 Thermally Induced Output Voltage Hysteresis Distribution

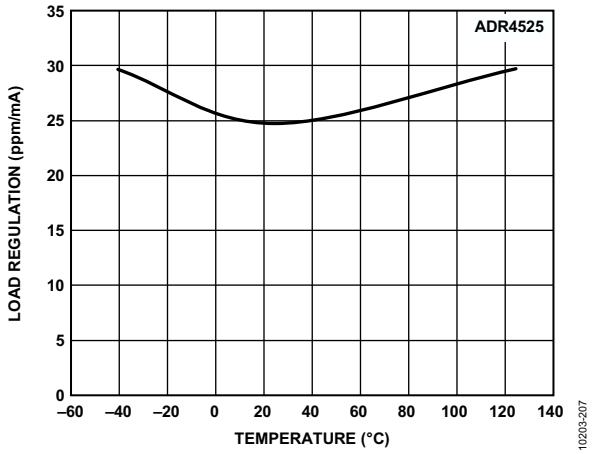



Figure 22. ADR4525 Load Regulation vs. Temperature (Sourcing)

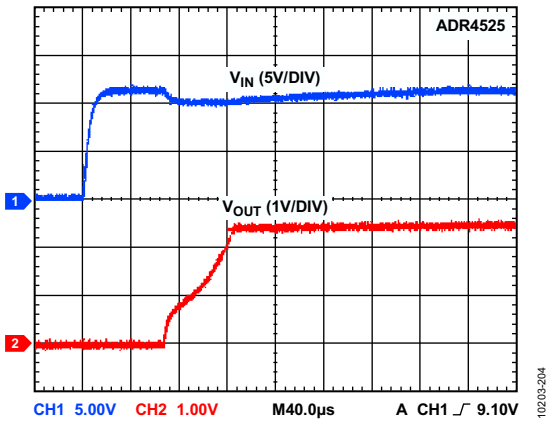



Figure 20. ADR4525 Output Voltage Start-Up Response

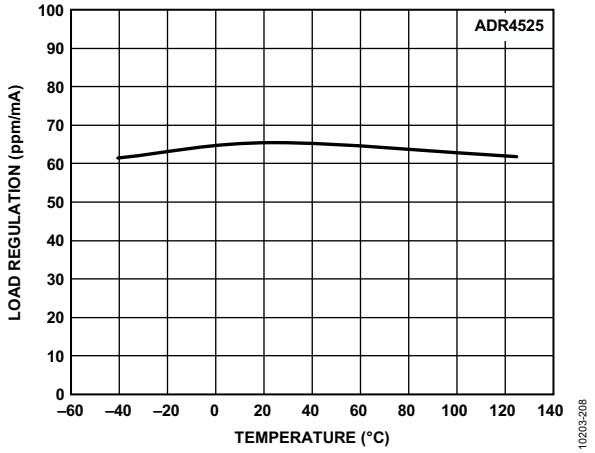



Figure 23. ADR4525 Load Regulation vs. Temperature (Sinking)

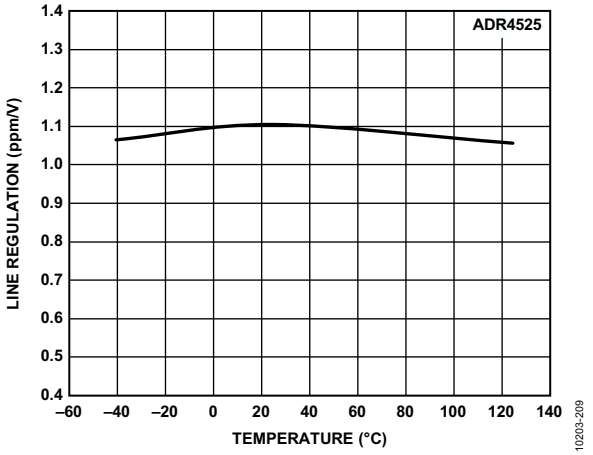



Figure 24. ADR4525 Line Regulation vs. Temperature

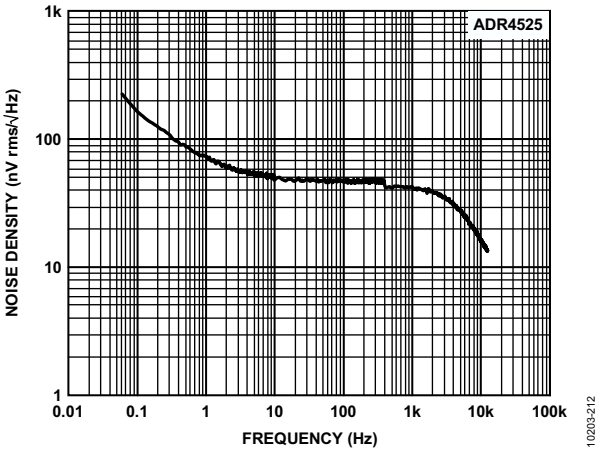



Figure 27. ADR4525 Output Noise Spectral Density

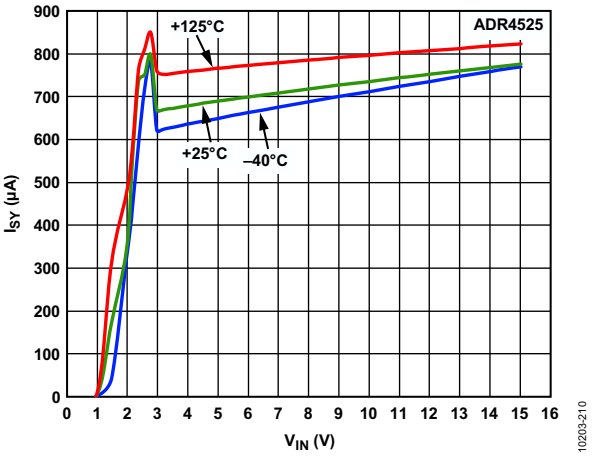



Figure 25. ADR4525 Supply Current vs. Supply Voltage

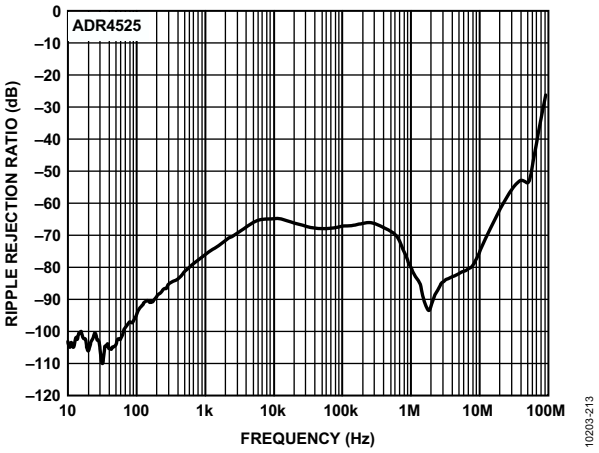



Figure 28. ADR4525 Ripple Rejection Ratio vs. Frequency

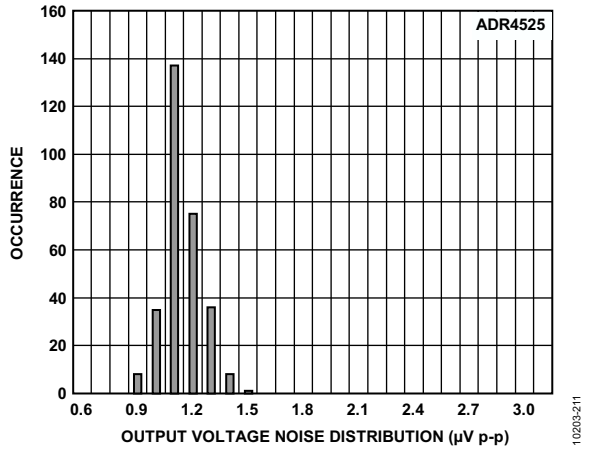



Figure 26. ADR4525 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

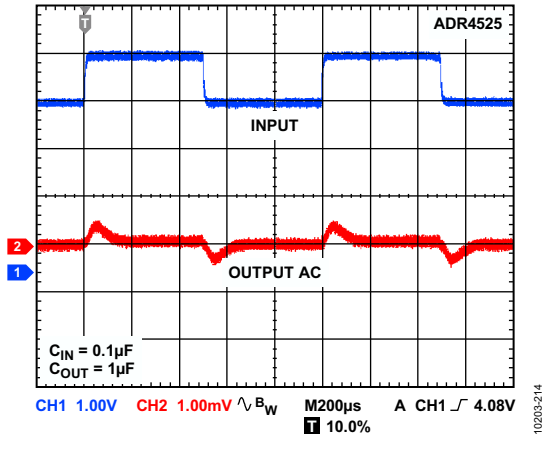



Figure 29. ADR4525 Line Transient Response

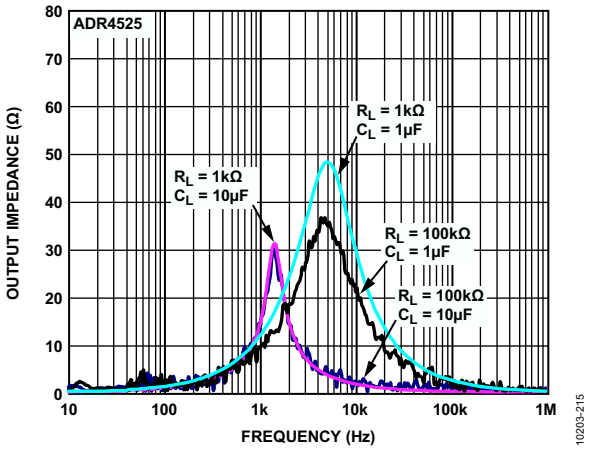



Figure 30. ADR4525 Output Impedance vs. Frequency

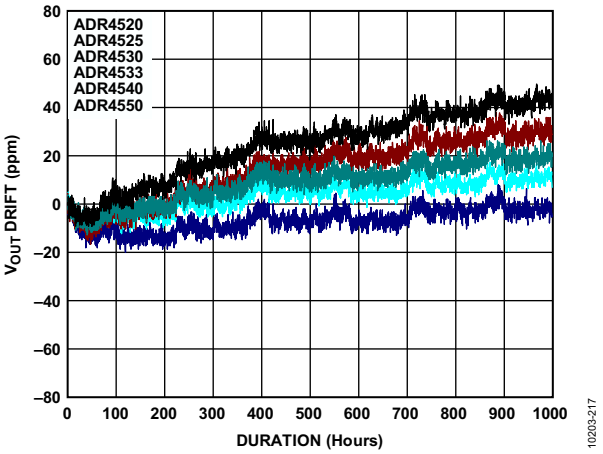



Figure 32. ADR4525 Typical Long-Term Output Voltage Drift (1000 Hours)

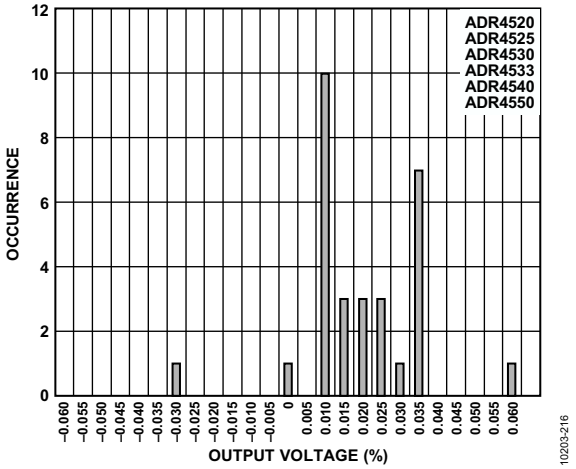



Figure 31. ADR4525 Output Voltage Drift Distribution After Reflow (SHR Drift)

## ADR4530

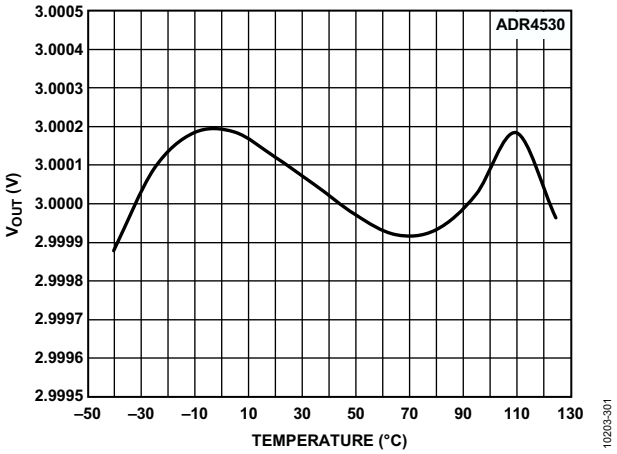



Figure 33. ADR4530 Output Voltage vs. Temperature

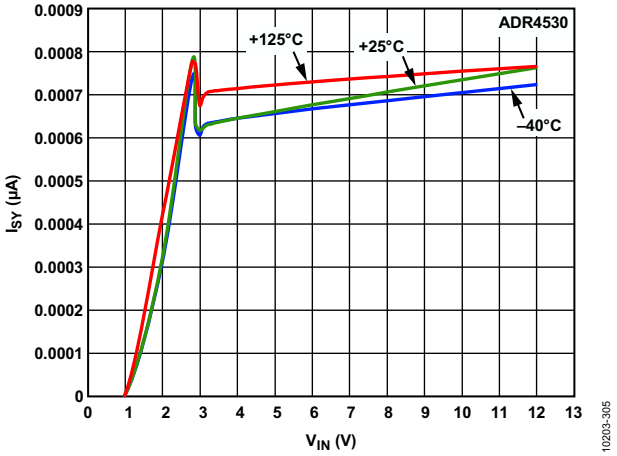



Figure 36. ADR4530 Supply Current vs. Supply Voltage

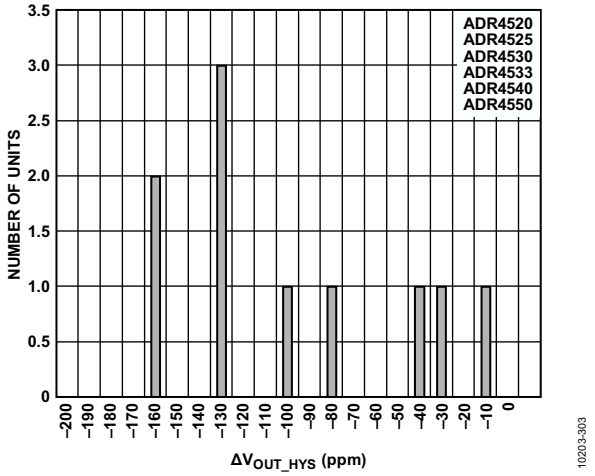



Figure 34. ADR4530 Thermally Induced Output Voltage Hysteresis Distribution

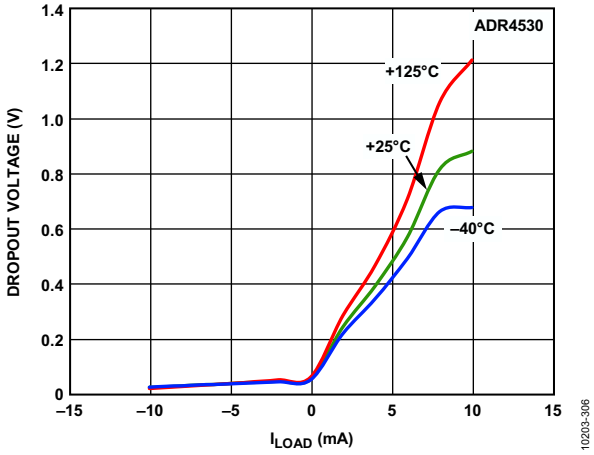



Figure 37. ADR4530 Dropout Voltage vs. Load Current

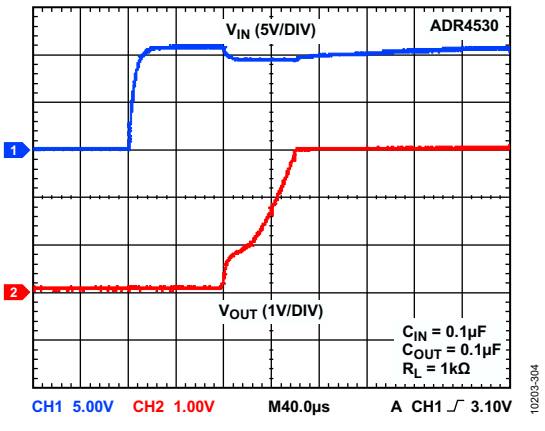



Figure 35. ADR4530 Output Voltage Start-Up Response

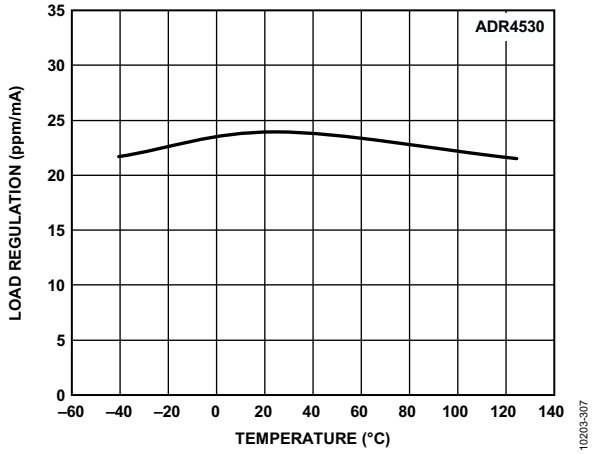



Figure 38. ADR4530 Load Regulation vs. Temperature (Sourcing)

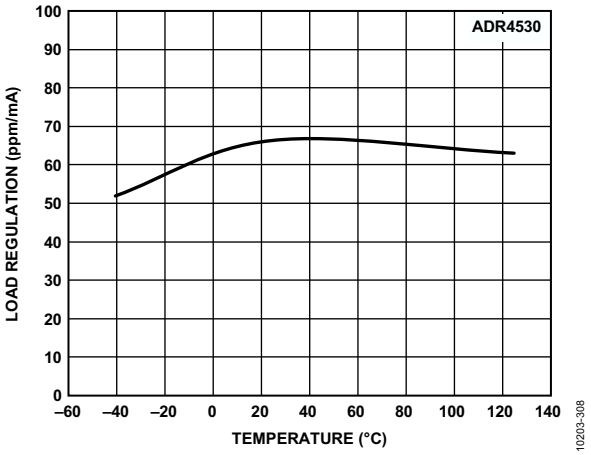



Figure 39. ADR4530 Load Regulation vs. Temperature (Sinking)

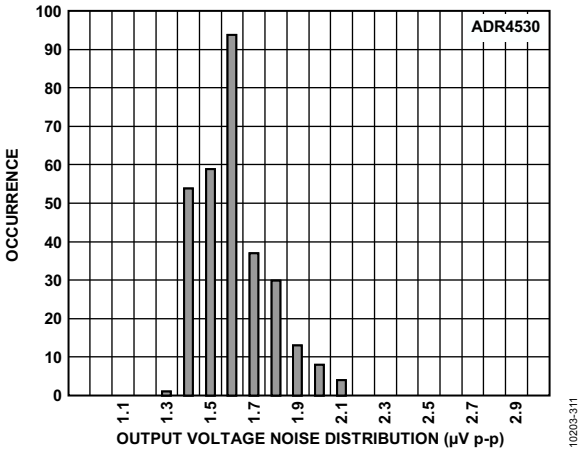



Figure 42. ADR4530 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

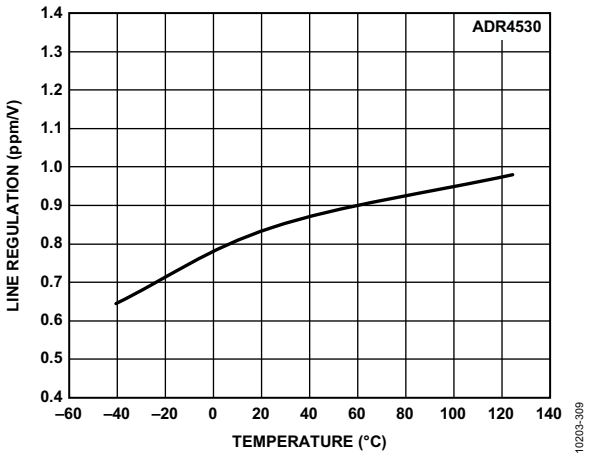



Figure 40. ADR4530 Line Regulation vs. Temperature

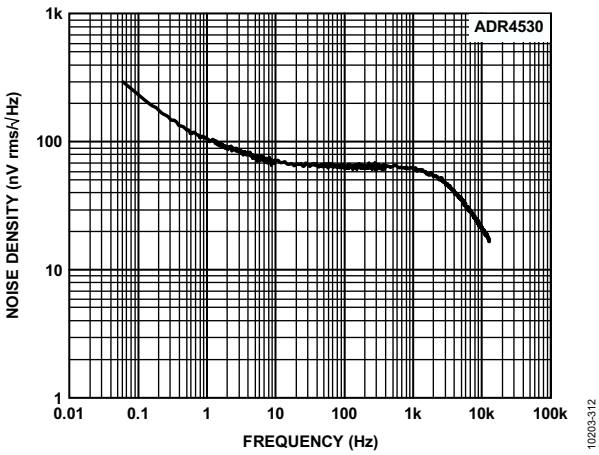



Figure 43. ADR4530 Output Noise Spectral Density

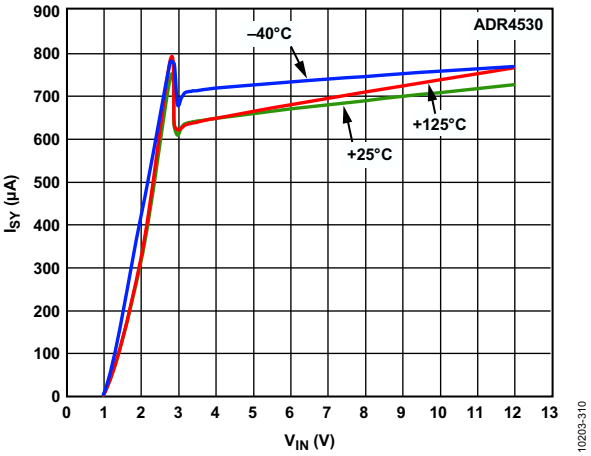



Figure 41. ADR4530 Supply Current vs. Supply Voltage

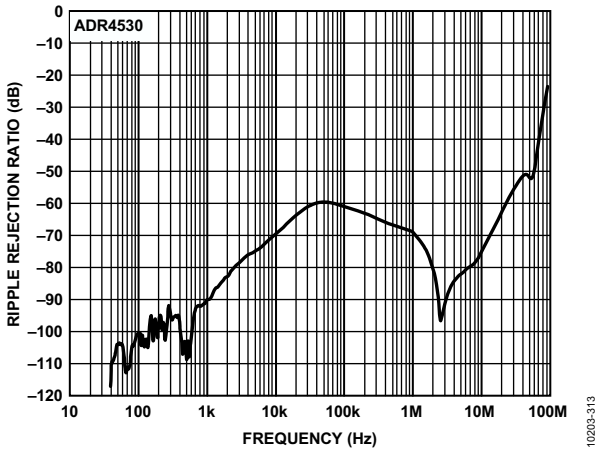



Figure 44. ADR4530 Ripple Rejection Ratio vs. Frequency

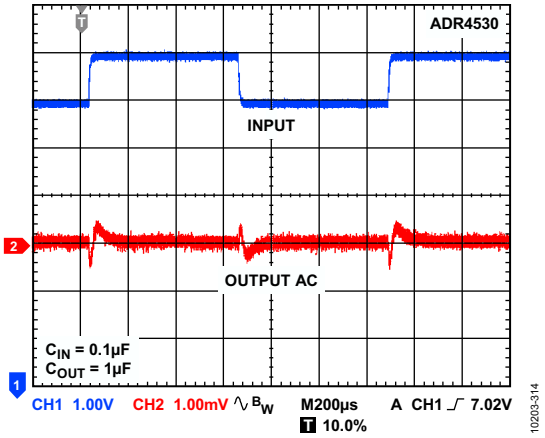



Figure 45. ADR4530 Line Transient Response

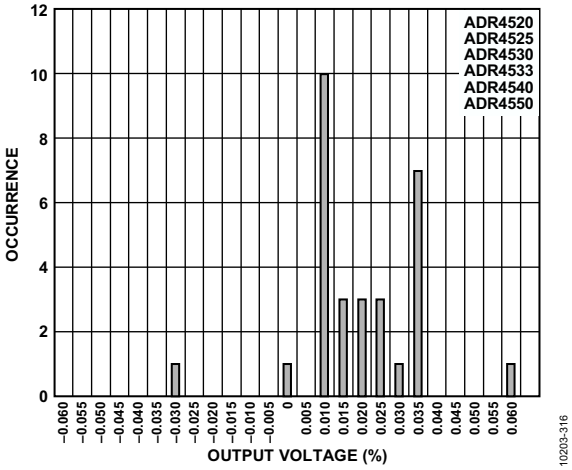



Figure 47. ADR4530 Output Voltage Drift Distribution After Reflow (SHR Drift)

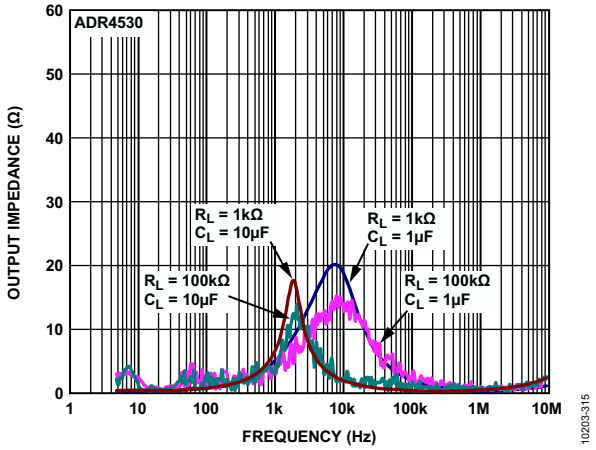



Figure 46. ADR4530 Output Impedance vs. Frequency

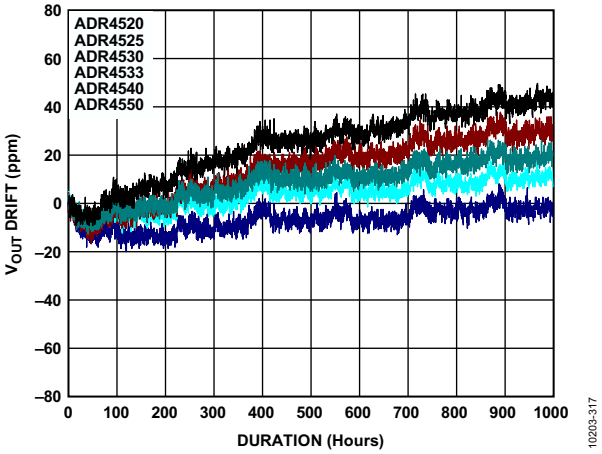



Figure 48. ADR4530 Typical Long-Term Output Voltage Drift (1000 Hours)

## ADR4533

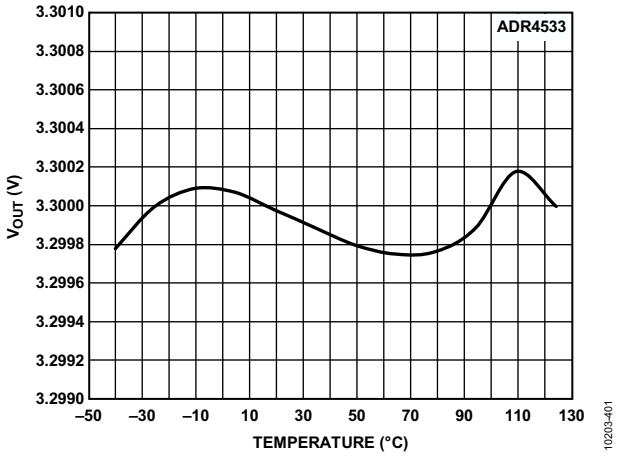



Figure 49. ADR4533 Output Voltage vs. Temperature

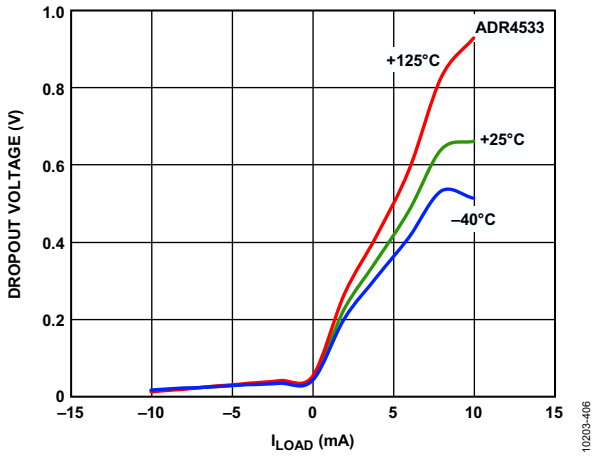



Figure 52. ADR4533 Dropout Voltage vs. Load Current

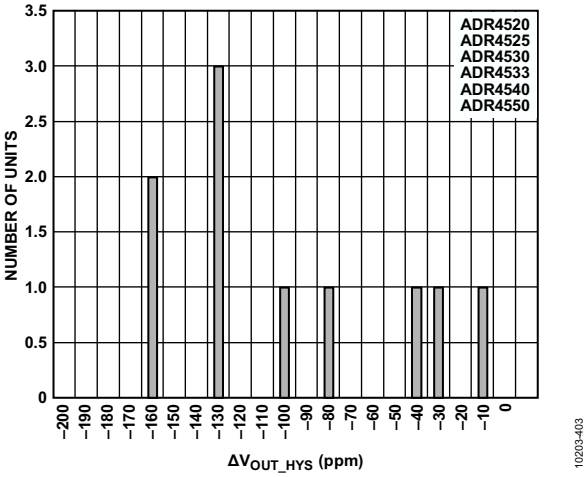



Figure 50. ADR4533 Thermally Induced Output Voltage Hysteresis Distribution

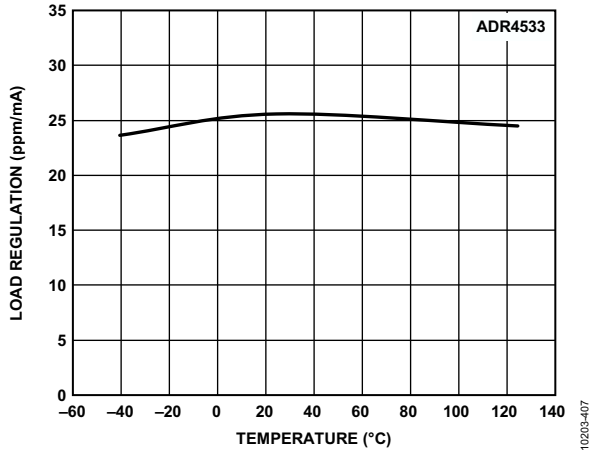



Figure 53. ADR4533 Load Regulation vs. Temperature (Sourcing)

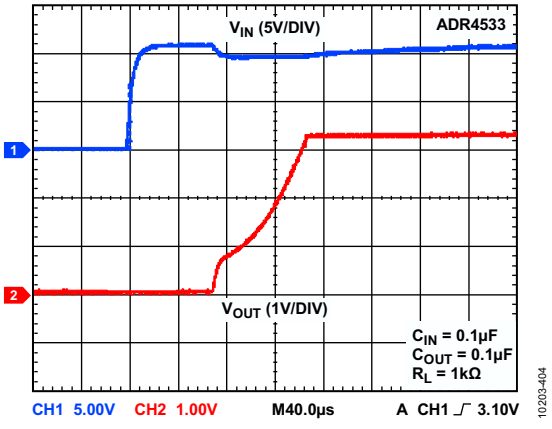



Figure 51. ADR4533 Output Voltage Start-Up Response

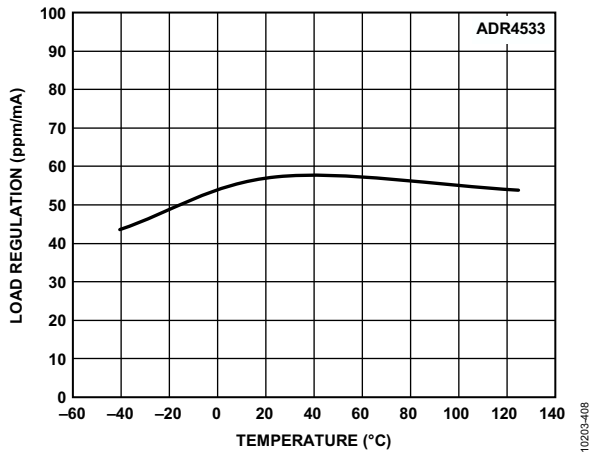



Figure 54. ADR4533 Load Regulation vs. Temperature (Sinking)

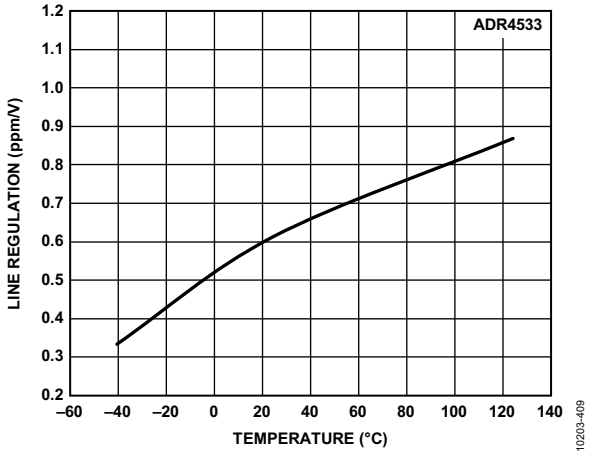



Figure 55. ADR4533 Line Regulation vs. Temperature

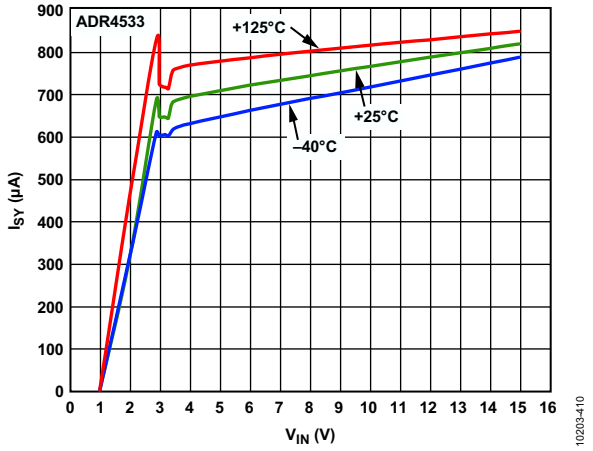



Figure 56. ADR4533 Supply Current vs. Supply Voltage

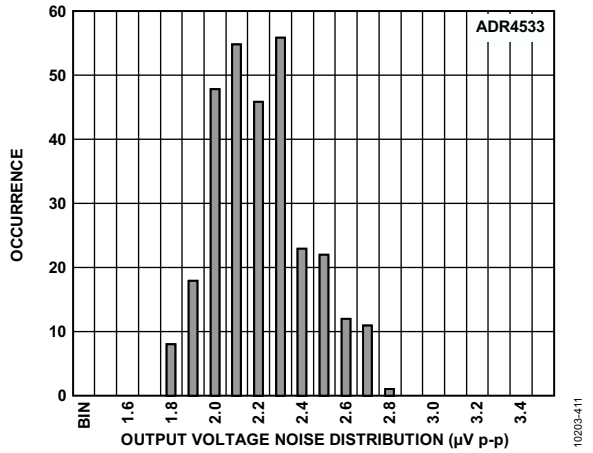



Figure 57. ADR4533 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

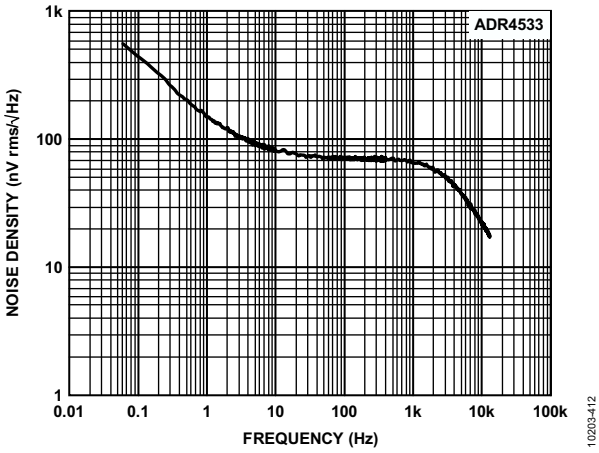



Figure 58. ADR4533 Output Noise Spectral Density

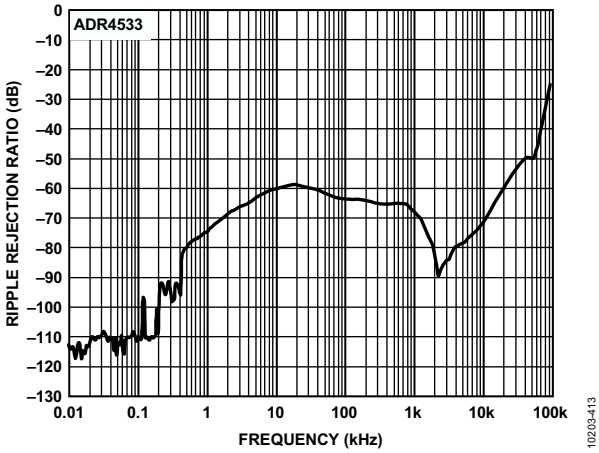



Figure 59. ADR4533 Ripple Rejection Ratio vs. Frequency

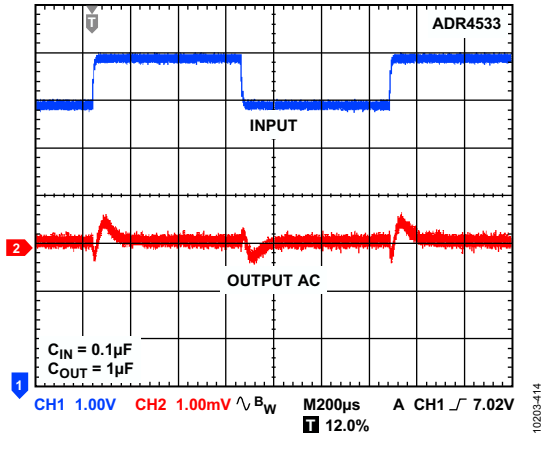



Figure 60. ADR4533 Line Transient Response

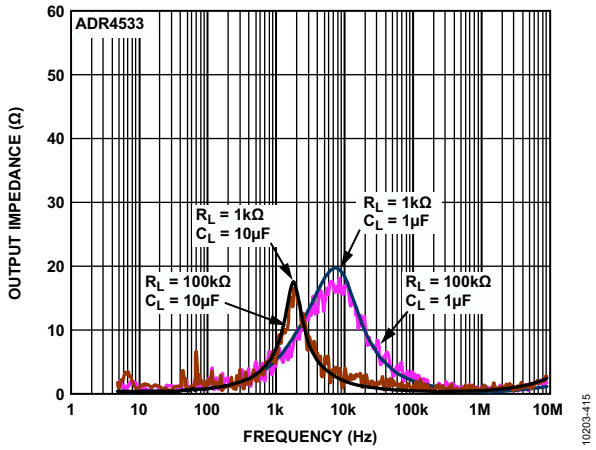



Figure 61. ADR4533 Output Impedance vs. Frequency

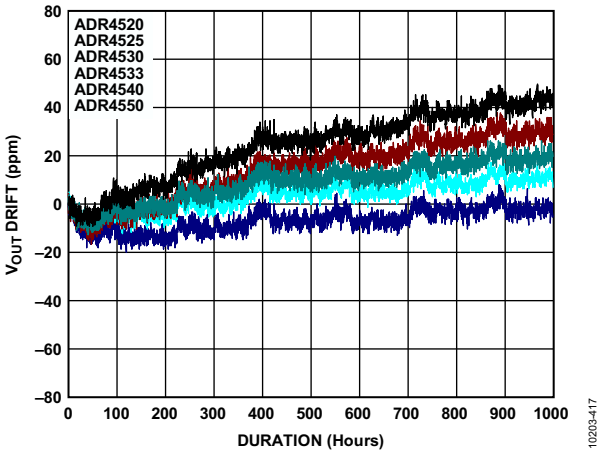



Figure 63. ADR4533 Typical Long-Term Output Voltage Drift (1000 Hours)

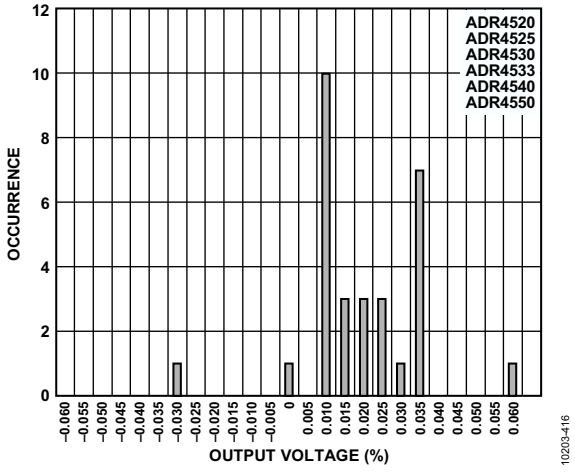



Figure 62. ADR4533 Output Voltage Drift Distribution After Reflow (SHR Drift)

## ADR4540

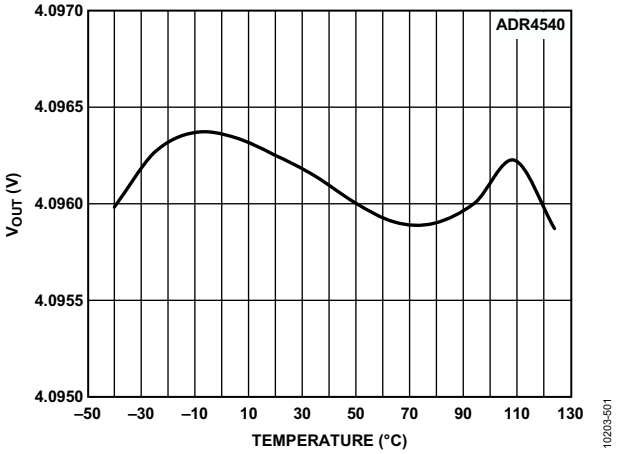



Figure 64. ADR4540 Output Voltage vs. Temperature

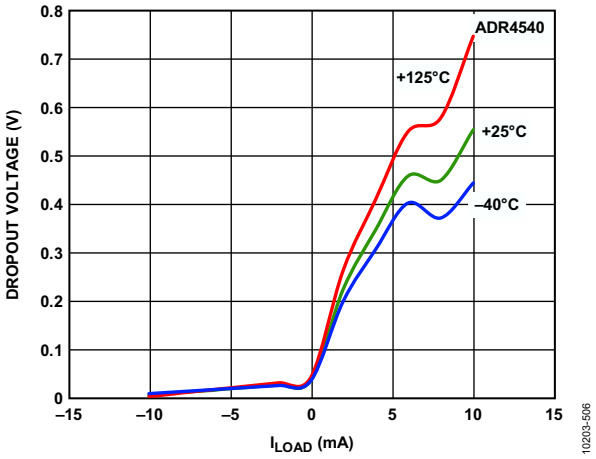



Figure 67. ADR4540 Dropout Voltage vs. Load Current

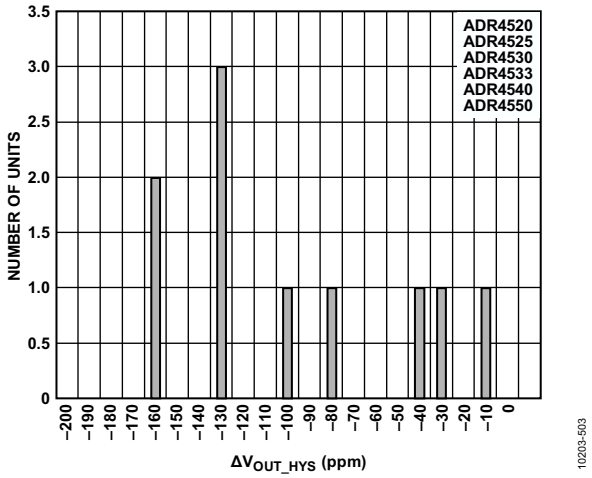



Figure 65. ADR4540 Thermally Induced Output Voltage Hysteresis Distribution

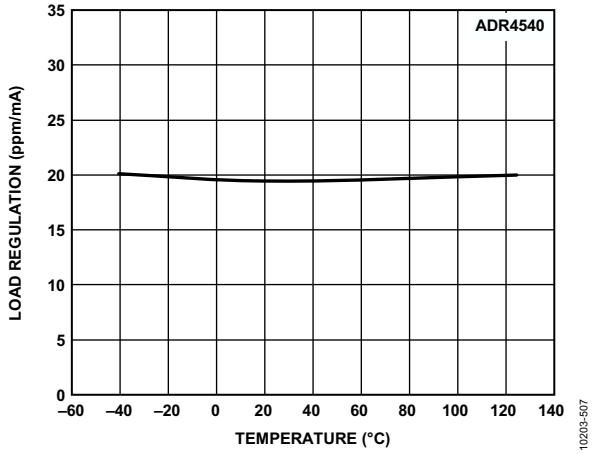



Figure 68. ADR4540 Load Regulation vs. Temperature (Sourcing)

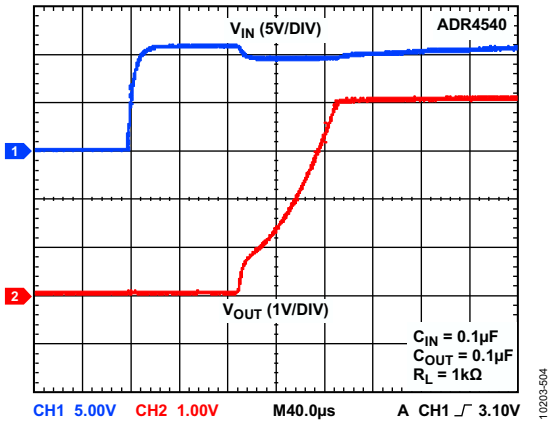



Figure 66. ADR4540 Output Voltage Start-Up Response

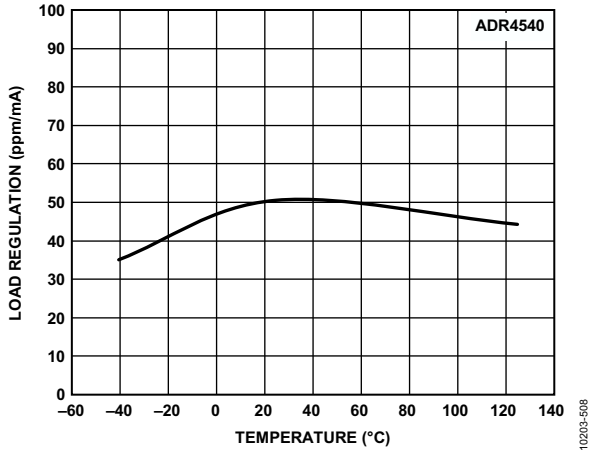



Figure 69. ADR4540 Load Regulation vs. Temperature (Sinking)

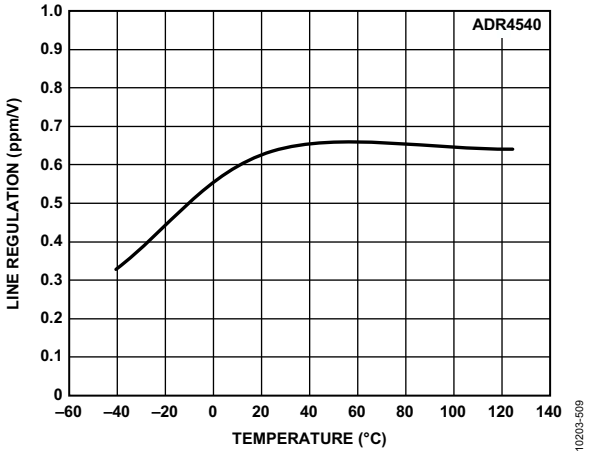



Figure 70. ADR4540 Line Regulation vs. Temperature

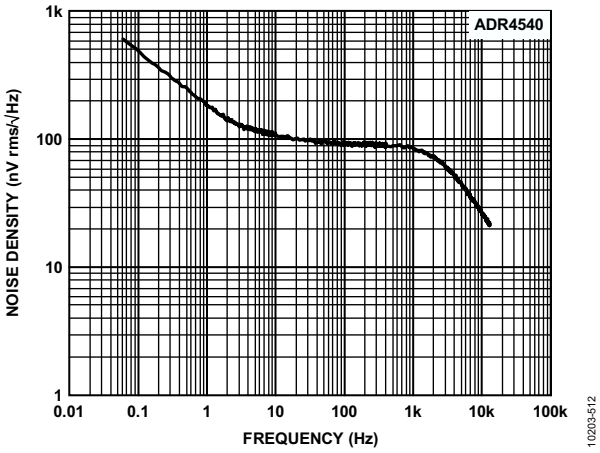



Figure 73. ADR4540 Output Noise Spectral Density

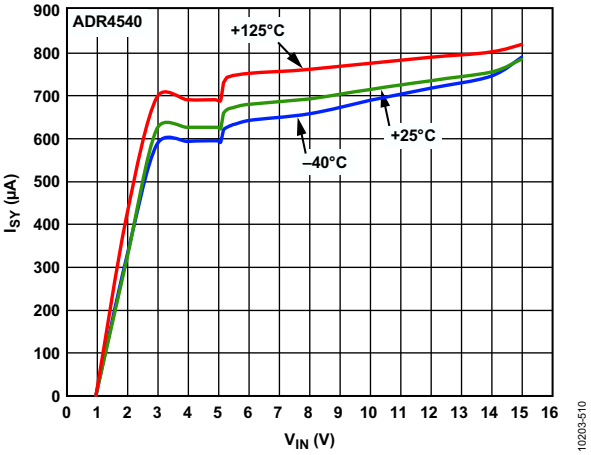



Figure 71. ADR4540 Supply Current vs. Supply Voltage

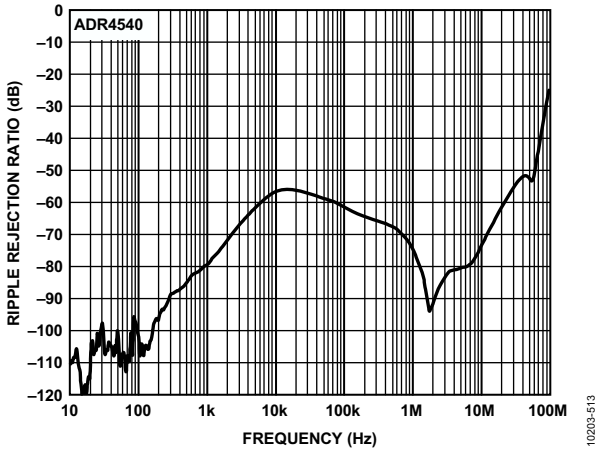



Figure 74. ADR4540 Ripple Rejection Ratio vs. Frequency

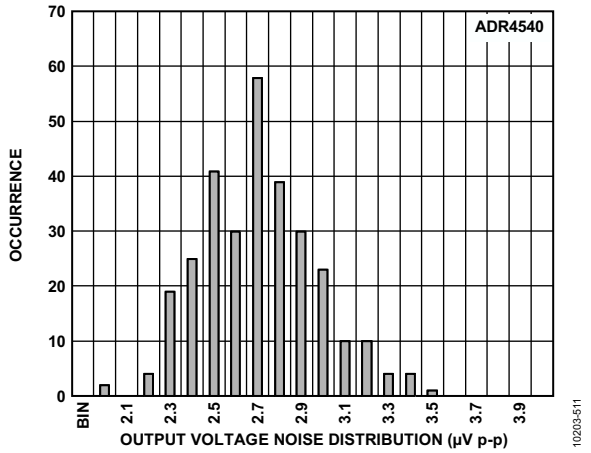



Figure 72. ADR4540 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

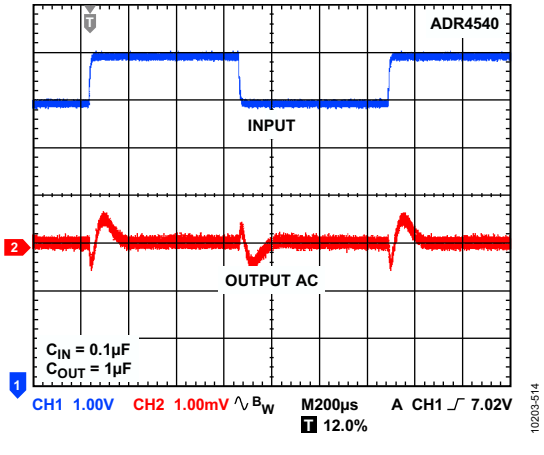



Figure 75. ADR4540 Line Transient Response

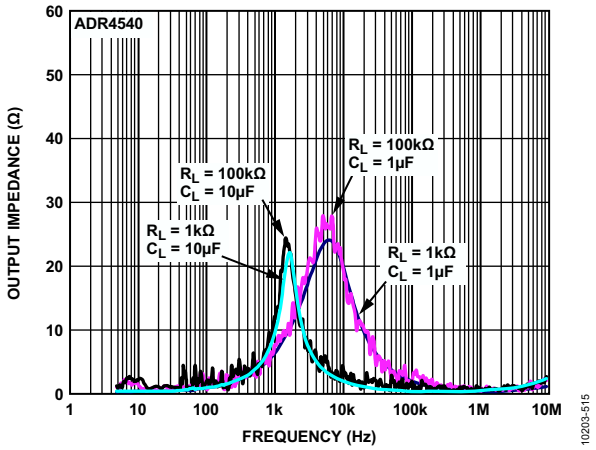



Figure 76. ADR4540 Output Impedance vs. Frequency

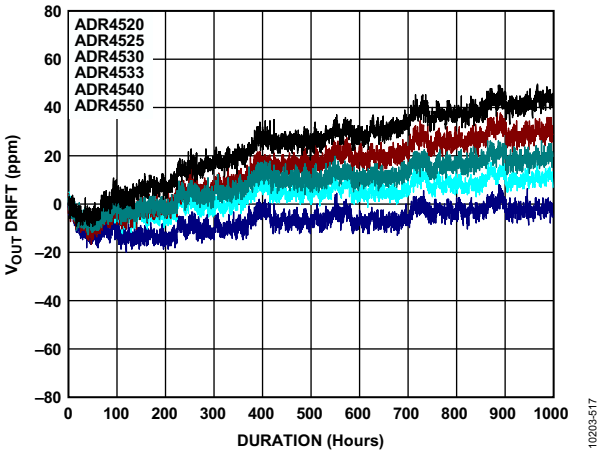



Figure 78. ADR4540 Typical Long-Term Output Voltage Drift (1000 Hours)

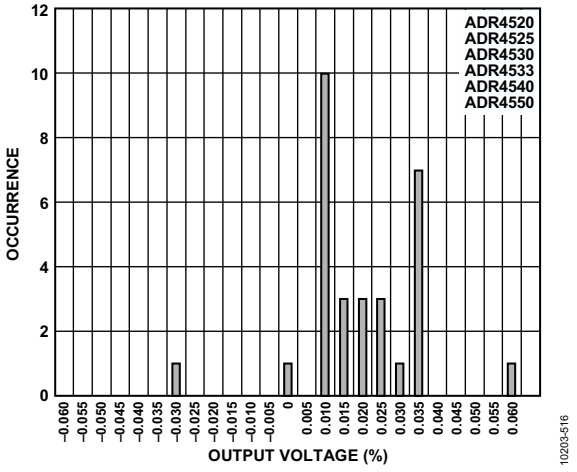



Figure 77. ADR4540 Output Voltage Drift Distribution After Reflow (SHR Drift)

## ADR4550

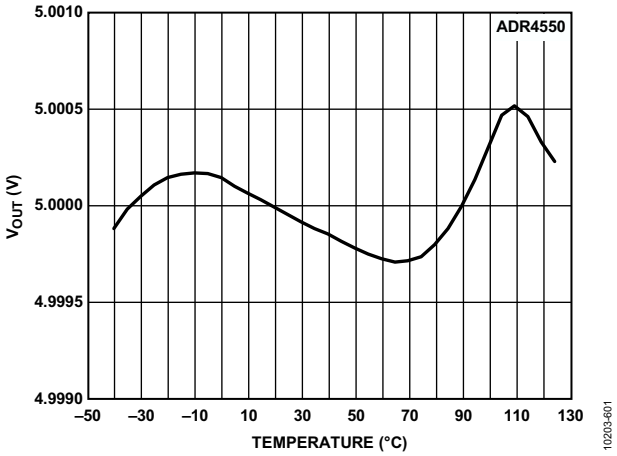



Figure 79. ADR4550 Output Voltage vs. Temperature

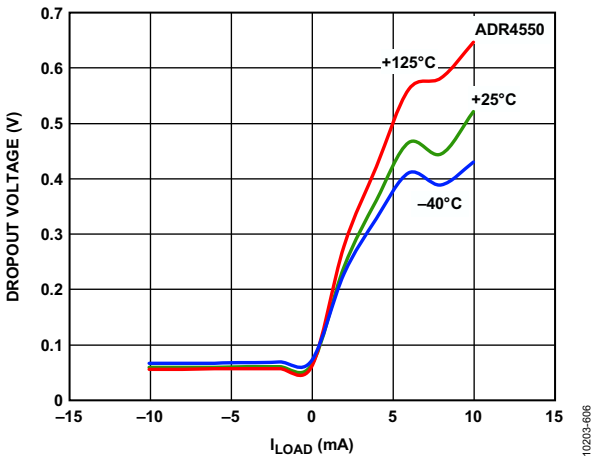



Figure 82. ADR4550 Dropout Voltage vs. Load Current

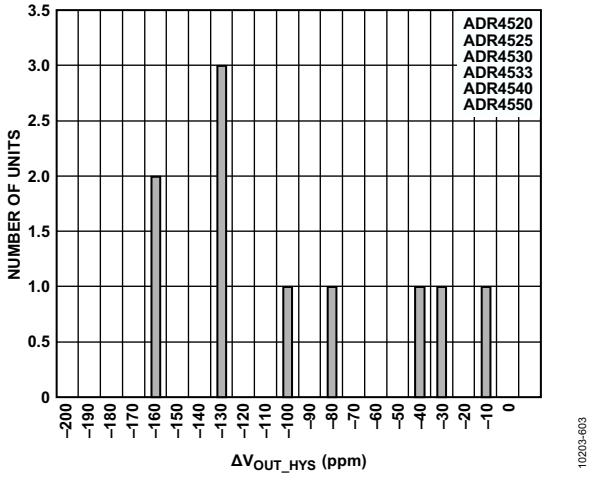



Figure 80. ADR4550 Thermally Induced Output Voltage Hysteresis Distribution

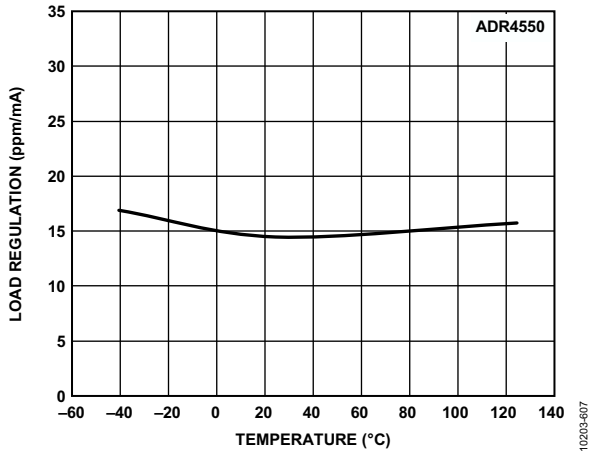



Figure 83. ADR4550 Load Regulation vs. Temperature (Sourcing)

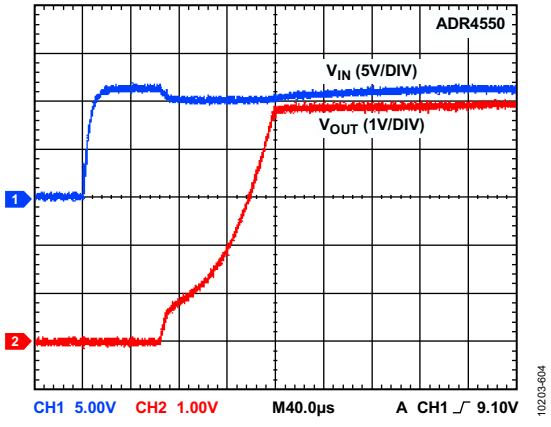



Figure 81. ADR4550 Output Voltage Start-Up Response

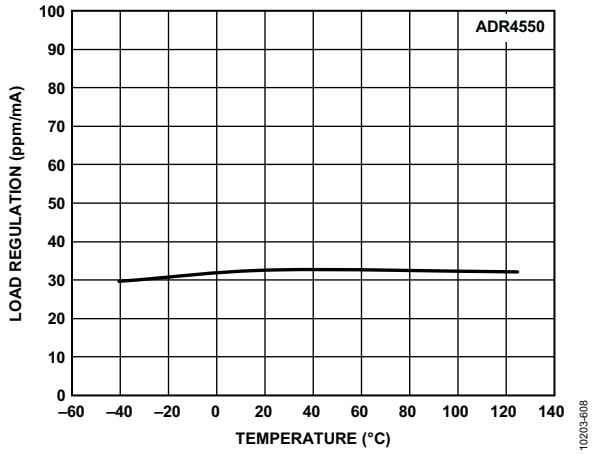



Figure 84. ADR4550 Load Regulation vs. Temperature (Sinking)

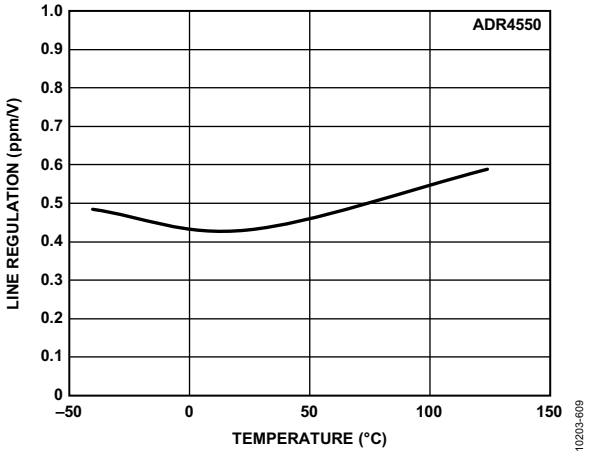



Figure 85. ADR4550 Line Regulation vs. Temperature

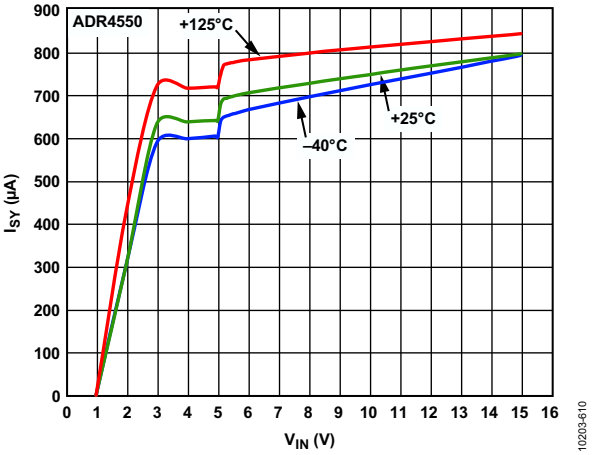



Figure 86. ADR4550 Supply Current vs. Supply Voltage

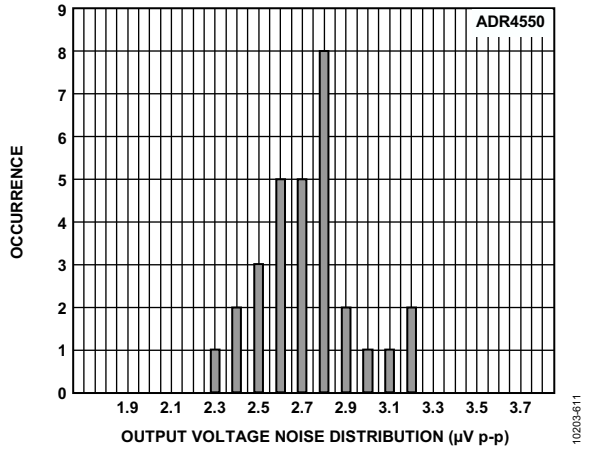



Figure 87. ADR4550 Output Voltage Noise (Maximum Amplitude from 0.1 Hz to 10 Hz)

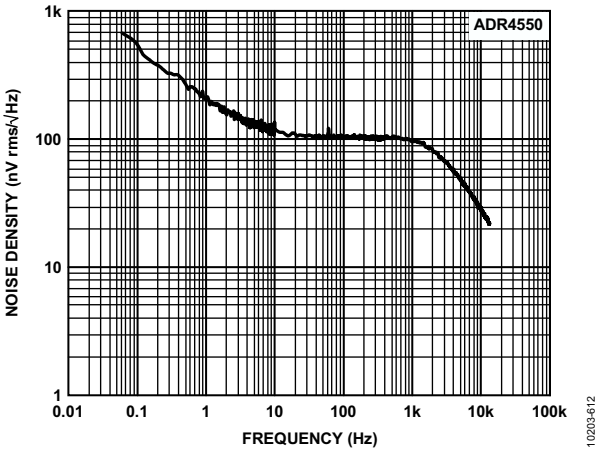



Figure 88. ADR4550 Output Noise Spectral Density

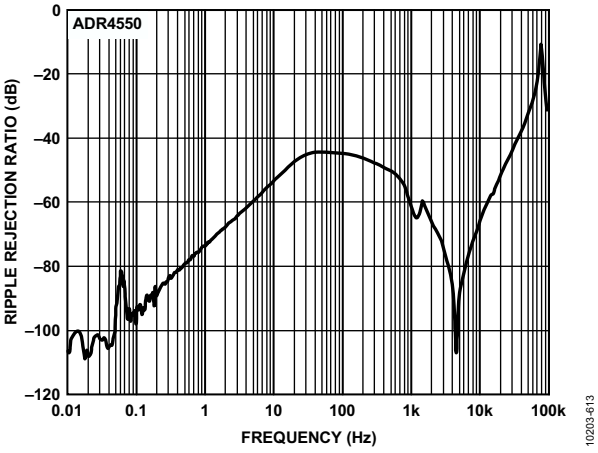



Figure 89. ADR4550 Ripple Rejection Ratio vs. Frequency

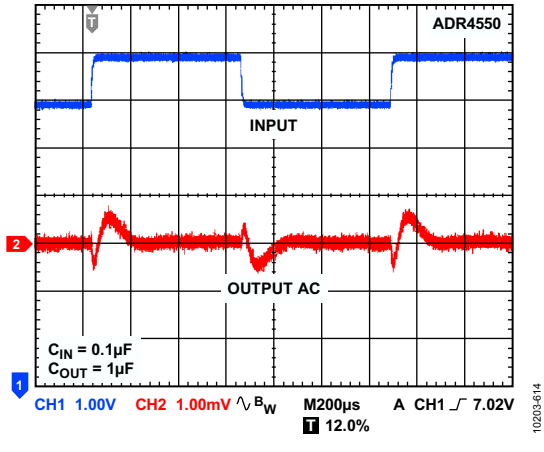



Figure 90. ADR4550 Line Transient Response

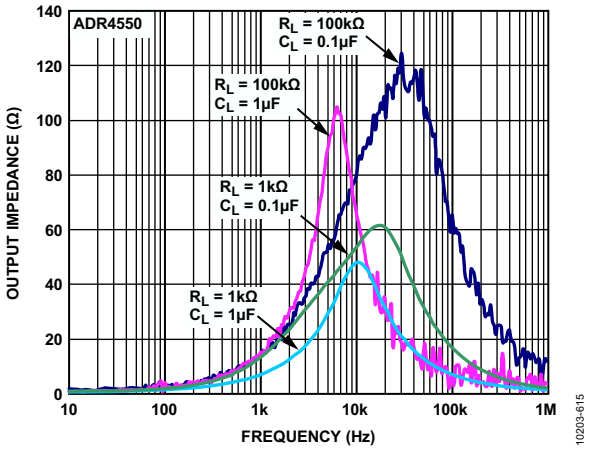



Figure 91. ADR4550 Output Impedance vs. Frequency

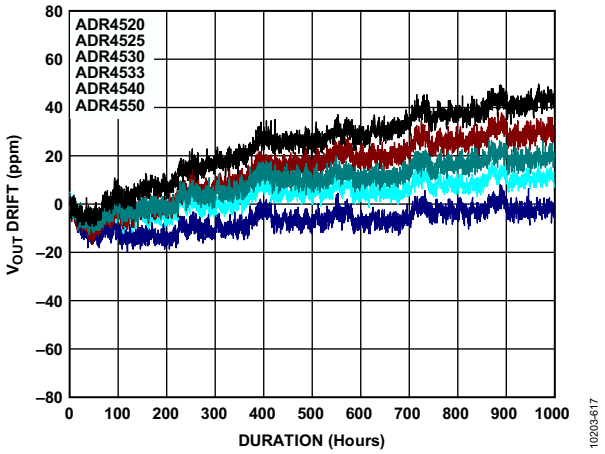



Figure 93. ADR4550 Typical Long-Term Output Voltage Drift (1000 Hours)

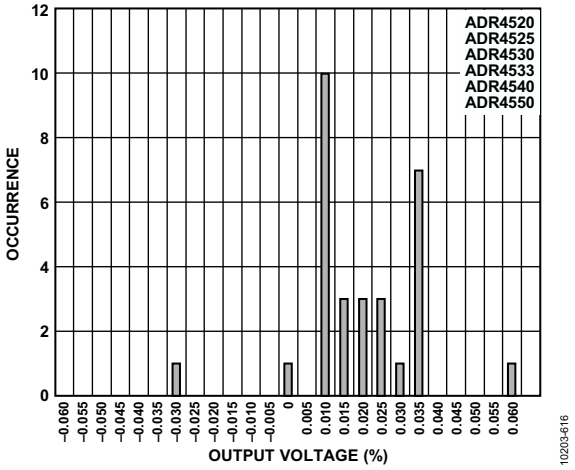



Figure 92. ADR4550 Output Voltage Drift Distribution After Reflow (SHR Drift)

# TERMINOLOGY

**Dropout Voltage ($V_{DO}$)**
Dropout voltage, sometimes referred to as supply voltage headroom or supply output voltage differential, is defined as the minimum voltage differential between the input and output such that the output voltage is maintained to within 0.1% accuracy.

$$V_{DO} = (V_{IN} - V_{OUT})_{min} | I_L = constant$$

Because the dropout voltage depends on the current passing through the device, it is always specified for a given load current. In series mode devices, the dropout voltage typically increases proportionally to the load current (see Figure 6, Figure 21, Figure 37, Figure 52, Figure 67, and Figure 82).

**Temperature Coefficient ($TCV_{OUT}$)**
The temperature coefficient relates the change in the output voltage to the change in the ambient temperature of the device, as normalized by the output voltage at 25°C. This parameter is determined by the box method, which is represented by the following equation:

$$TCV_{OUT} = \left| \frac{max\{V_{OUT}(T_1, T_2, T_3)\} - min\{V_{OUT}(T_1, T_2, T_3)\}}{V_{OUT}(T_2) \times (T_3 - T_1)} \right| \times 10^6$$

where:
$TCV_{OUT}$ is expressed in ppm/°C.
$V_{OUT}(T_x)$ is the output voltage at Temperature $T_x$.
$T_1$ = −40°C.
$T_2$ = +25°C.
$T_3$ = +125°C.

This three-point method ensures that $TCV_{OUT}$ accurately portrays the maximum difference between any of the three temperatures at which the output voltage of the part is measured.

The $TCV_{OUT}$ for the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 is fully tested over three temperatures: −40°C, +25°C, and +125°C.

**Thermally Induced Output Voltage Hysteresis ($\Delta V_{OUT\_HYS}$)**
Thermally induced output voltage hysteresis represents the change in the output voltage after the device is exposed to a specified temperature cycle. This is expressed as either a shift in voltage or a difference in ppm from the nominal output.

$$\Delta V_{OUT\_HYS} = \frac{V_{OUT\_25°C} - V_{OUT\_TC}}{V_{OUT\_25°C}} \times 10^6 \quad [ppm]$$

where:
$V_{OUT\_25°C}$ is the output voltage at 25°C.
$V_{OUT\_TC}$ is the output voltage after temperature cycling.

**Long-Term Stability ($\Delta V_{OUT\_LTD}$)**
Long-term stability refers to the shift in the output voltage at 60°C after 1000 hours of operation in a 60°C environment. The ambient temperature is kept at 60°C to ensure that the temperature chamber does not switch randomly between heating and cooling, which can cause instability over the 1000 hour measurement. This is also expressed as either a shift in voltage or a difference in ppm from the nominal output.

$$\Delta V_{OUT\_LTD} = \left| \frac{V_{OUT}(t_1) - V_{OUT}(t_0)}{V_{OUT}(t_0)} \right| \times 10^6 \quad [ppm]$$

where:
$V_{OUT}(t_0)$ is the $V_{OUT}$ at 60°C at Time 0.
$V_{OUT}(t_1)$ is the $V_{OUT}$ at 60°C after 1000 hours of operation at 60°C.

**Line Regulation**
Line regulation refers to the change in output voltage in response to a given change in input voltage and is expressed in percent per volt, ppm per volt, or µV per volt change in input voltage. This parameter accounts for the effects of self-heating.

**Load Regulation**
Load regulation refers to the change in output voltage in response to a given change in load current and is expressed in µV per mA, ppm per mA, or ohms of dc output resistance. This parameter accounts for the effects of self-heating.

**Solder Heat Resistance (SHR) Shift**
SHR shift refers to the permanent shift in output voltage that is induced by exposure to reflow soldering and is expressed in units of ppm. This shift is caused by changes in the stress exhibited on the die by the package materials when these materials are exposed to high temperatures. This effect is more pronounced in lead-free soldering processes due to higher reflow temperatures.

# THEORY OF OPERATION

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 series of references uses a unique core topology for extremely high accuracy, stability, and noise performance.

Three parameters contribute to the accuracy of the dc output of a voltage reference: initial accuracy, temperature coefficient, and long-term drift. With an outstanding guaranteed initial error of 0.02% and a low temperature coefficient of 2 ppm/°C maximum, this series of voltage references is perfect for high precision applications. The industry-leading long-term stability of the devices means that systems need less frequent field calibration and that there is a reduction in the costly preshipment system burn-in time.

## LONG-TERM DRIFT

One of the key parameters of the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 references is long-term stability—the output drift over time that the device is powered up. Regardless of output voltage, internal testing during development showed a typical drift of approximately 25 ppm after 1000 hours of continuous, nonloaded operation in a 60°C extremely stable temperature controlled environment.

Note that the majority of the long-term drift typically occurs in the first 200 hours to 300 hours of operation. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time. See the AN-713 Application Note, *The Effect of Long-Term Drift on Voltage References*, at www.analog.com for more information regarding the effects of long-term drift and how it can be minimized.

## POWER DISSIPATION

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 voltage references are capable of sourcing and sinking up to 10 mA of load current at room temperature across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current should be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated via the following equation:

$$P_D = \frac{T_J - T_A}{\theta_{JA}}$$

where:
$P_D$ is the device power dissipation.
$T_J$ is the device junction temperature.
$T_A$ is the ambient temperature.
$\theta_{JA}$ is the package (junction-to-air) thermal resistance.

Due to this relationship, acceptable load current in high temperature conditions may be less than the maximum current sourcing capability of the device. In no case should the part be operated outside of its maximum power rating because doing so may result in premature failure or permanent damage to the device.

# APPLICATIONS INFORMATION

## BASIC VOLTAGE REFERENCE CONNECTION

The circuit shown in Figure 94 illustrates the basic configuration for the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 family of voltage references.

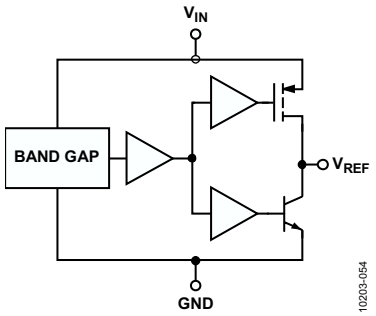



*Figure 94. ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 Simplified Schematic*

## INPUT AND OUTPUT CAPACITORS

### *Input Capacitors*

A 1 µF to 10 µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. An additional 0.1 µF ceramic capacitor should be connected in parallel to reduce supply noise.

### *Output Capacitors*

An output capacitor is required for stability and to filter out low level voltage noise. The minimum value of the output capacitor is shown in Table 12.

**Table 12. Minimum $C_{OUT}$ Value**

| Part Number | Minimum $C_{OUT}$ Value |
|---|---|
| ADR4520, ADR4525 | 1.0 µF |
| ADR4530, ADR4533, ADR4540, ADR4550 | 0.1 µF |

An additional 1 µF to 10 µF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, the designer should keep in mind that doing so will increase the turn-on time of the device.

## LOCATION OF REFERENCE IN SYSTEM

The ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 reference should be placed as close to the load as possible to minimize the length of the output traces and, therefore, the error introduced by the voltage drop. Current flowing through a PCB trace produces an IR voltage drop; with longer traces, this drop can reach several millivolts or more, introducing considerable error into the output voltage of the reference. A 1 inch long, 5 mm wide trace of 1 ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error.

## SAMPLE APPLICATIONS

### *Bipolar Output Reference*

Figure 95 shows a bipolar reference configuration. By connecting the output of the ADR4550 to the inverting terminal of an operational amplifier, it is possible to obtain both positive and negative reference voltages. R1 and R2 must be matched as closely as possible to ensure minimal difference between the negative and positive outputs. Resistors with low temperature coefficients must also be used if the circuit is used in environments with large temperature swings; otherwise, a voltage difference develops between the two outputs as the ambient temperature changes.

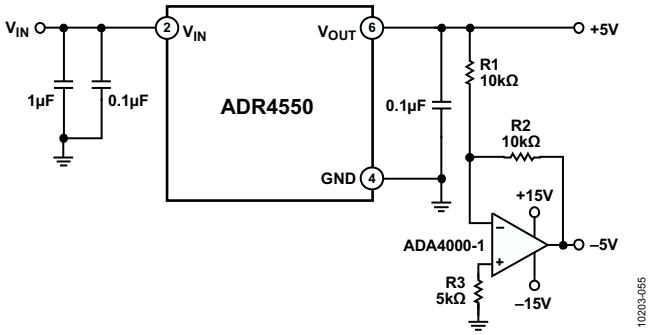



*Figure 95. ADR4550 Bipolar Output Reference*

### *Boosted Output Current Reference*

Figure 96 shows a configuration for obtaining higher current drive capability from the ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550 references without sacrificing accuracy. The op amp regulates the current flow through the MOSFET until $V_{OUT}$ equals the output voltage of the reference; current is then drawn directly from $V_{IN}$ instead of from the reference itself, allowing increased current drive capability.

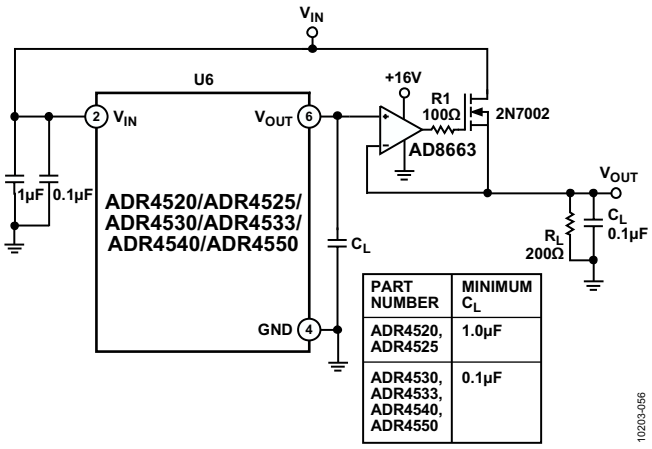
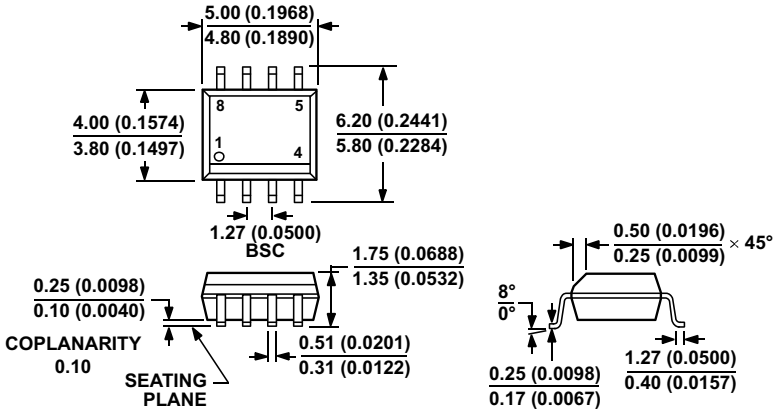



*Figure 96. Boosted Output Current Reference*

Because the current-sourcing capability of this circuit depends only on the $I_D$ rating of the MOSFET, the output drive capability can be adjusted to the application simply by choosing an appropriate MOSFET. In all cases, the $V_{OUT}$ pin should be tied directly to the load device to maintain maximum output voltage accuracy.

# OUTLINE DIMENSIONS




**COMPLIANT TO JEDEC STANDARDS MS-012-AA**
**CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.**

012407-A

*Figure 97. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity |
|---|---|---|---|---|
| ADR4520ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4520ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4520BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4520BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4525ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4525ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4525BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4525BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4530ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4530ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4530BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4530BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4533ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4533ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4533BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4533BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4540ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4540ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4540BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4540BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4550ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4550ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |
| ADR4550BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 98 |
| ADR4550BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | 1,000 |

[1] Z = RoHS Compliant Part.