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Status	Product Specification
ACL Products	

AC11979: Preliminary Specification
ACT11979: Product Specification
8-bit multiplexed I/O read-back register

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11979 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11979 device is an 8-bit multiplexed I/O read-back register. When the Output Enable ($\overline{OE}$) input is held High, it loads data on the rising edge of the Clock (CP). When the Clock is held High or Low, the data is held in the registers. When the Output Enable is Low, the data held in the register is visible on the I/O pins (I/O_n).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PZH}/ t_{PZL}	Propagation delay $\overline{OE}$ to I/O_n	C_L = 50pF	6.2	6.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; Disabled	12	15	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled	8.5	8.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

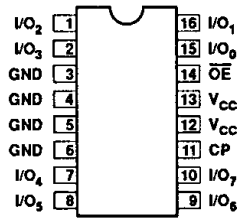
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

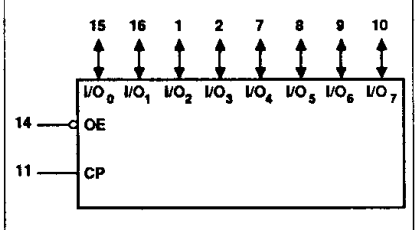
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11979N 74ACT11979N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11979D 74ACT11979D

PIN CONFIGURATION

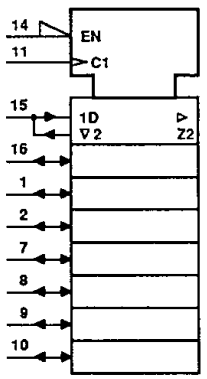
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14	$\overline{OE}$	Output enable input (active Low)
11	CP	Clock input
15, 16, 1, 2 7, 8, 9, 10	I/O_0 - I/O_7	Data inputs/outputs (3-state)
3, 4, 5, 6	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

$\overline{OE}$	CP	I/O_n	OPERATION
L	X*	Data out	Output data
H	↑	l h	Load data
H	H L	Z	Hold data

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low volatge level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Z = High-impedance (OFF) state
* The register is loaded on any Low-to-High transition

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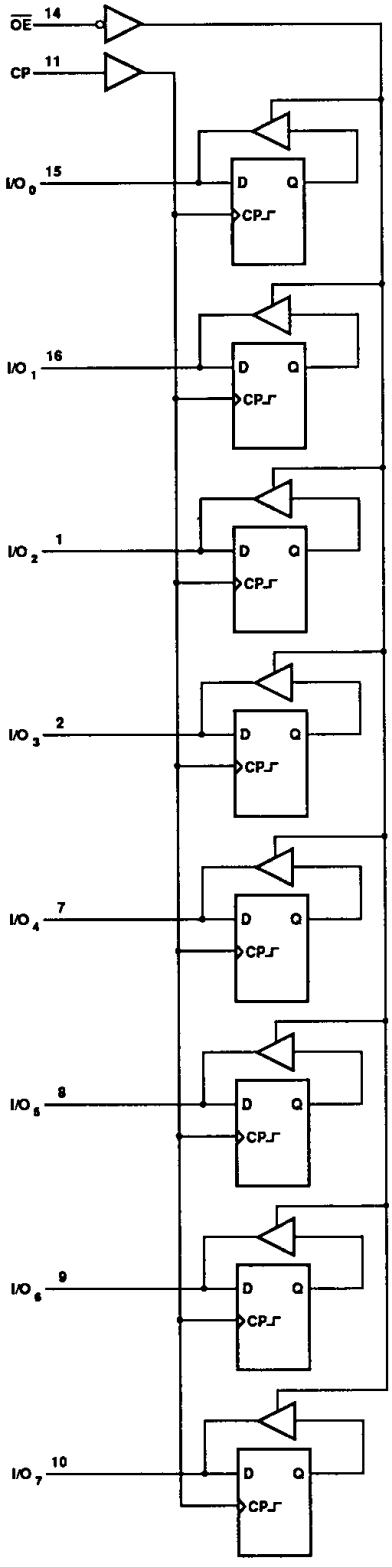
LOGIC DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11979			74ACT11979			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11979				74ACT11979				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.0V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11979					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output enable time to High and Low level	1	3.6 5.0	7.9 9.2	9.9 11.1	3.6 5.0	10.9 12.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	1	4.1 3.7	7.2 6.6	8.7 8.2	4.1 3.7	9.1 8.5	ns
t_W	CP pulse width High or Low	2	4.0			4.0		ns
t_S	Setup time I/O_n to CP	2	6.0			6.0		ns
t_H	Hold time CP to I/O_n	2	0.0			0.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11979					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output enable time to High and Low level	1	3.1 4.4	5.4 7.0	7.3 9.2	3.1 4.4	7.9 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	1	3.8 3.4	5.8 5.5	7.8 7.5	3.8 3.4	8.2 7.8	ns
t_W	CP pulse width High or Low	2	3.0			3.0		ns
t_S	Setup time I/O_n to CP	2	5.0			5.0		ns
t_H	Hold time CP to I/O_n	2	0.5			0.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11979					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output enable time to High and Low level	1	2.4 3.0	5.8 7.5	9.1 11.3	2.4 3.0	9.9 12.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	1	4.5 4.2	6.8 6.7	9.4 9.3	4.5 4.2	10.0 9.8	ns
t_W	CP pulse width High or Low	2	4.0			4.0		ns
t_S	Setup time I/O_n to CP	2	4.5			4.5		ns
t_H	Hold time CP to I/O_n	2	1.5			1.5		ns

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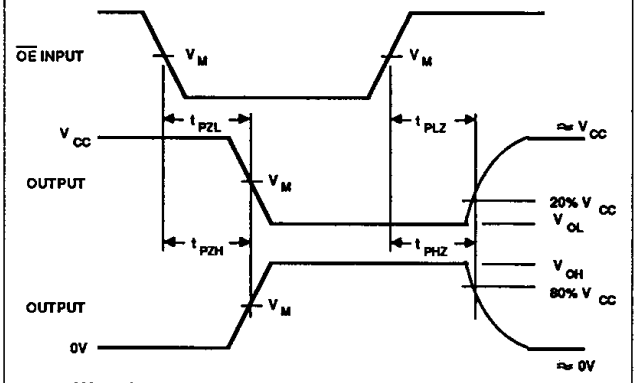
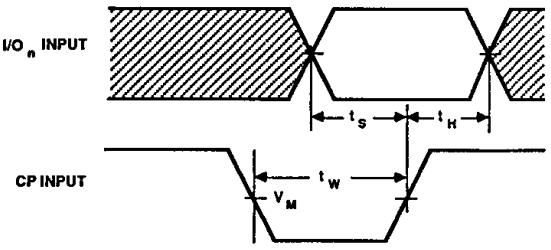
AC WAVEFORMS



Waveform 1. Waveforms Showing the 3-State Output Enable and Disable Times

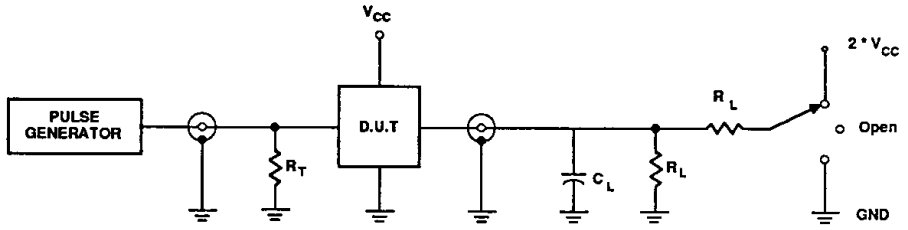


Waveform 2. Waveforms Showing the Data Setup and Hold Times for I/O_n Input to CP Input

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns