HI-6011
ARINC 429
Transmitter / Dual Receiver for 8-Bit Bus

HOLT INC.
INTEGRATED CIRCUITS

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GENERAL DESCRIPTION

The HI-6011 is a CMOS integrated circuit designed to interface the avionics ARINC 429 data bus to an 8-bit port. It contains two receivers and one transmitter. They operate independently except for the parity option and the selected clock rate. The receiver demands that the incoming data meet the standard protocol and the transmitter outputs a standard protocol stream.

The HI-6011 provides flexible options for interfacing to the user system. The controlling processor can operate both the receiver and transmitter either by using hard wired flags and gates at the pins or by using software reads and writes of internal registers or a combination thereof.

The chip is programmable to operate with single 8-bit bytes where successive writes and reads are used to receive or transmit complete 32 bit words.

The receiver allows two operational modes: Mode 0 to allow receiving data words irrespective of the word's address label (first 8 Bits); Mode 1 to permit receiving only words with matching address labels.

A Master clock signal of 1, 6 or 12 MHz is supplied to the HI-6011. Two bits of the control word define the frequency.

Interrupt error flags are generated for received parity errors or premature (before 32 bits are received) idle line conditions.

The HI-6011 is a 5 volt chip that will require data translation from and to the ARINC bus using external line drivers and line receivers. The HI-8591 line receiver is available for the receiver side and the single supply HI-8592 line driver is available for the transmitter side.
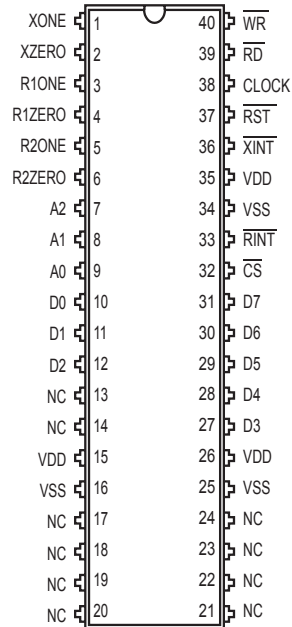
APPLICATIONS

- Avionics Data Communication
- Serial to Parallel Conversion
- Parallel to Serial Conversion

FEATURES

- Single +5V supply
- ARINC 429 protocol controller with 8-bit parallel host interface
- Automatic label recognition option
- Programmable parity option
- Transmit FIFO for up to five ARINC 429 messages
- CMOS / TTL logic pins
- Industrial and Extended temperature ranges
- Burn-in available

PIN CONFIGURATION (TOP VIEW)

XONE	1	40	$\overline{WR}$
XZERO	2	39	$\overline{RD}$
R1ONE	3	38	CLOCK
R1ZERO	4	37	$\overline{RST}$
R2ONE	5	36	$\overline{XINT}$
R2ZERO	6	35	VDD
A2	7	34	VSS
A1	8	33	$\overline{RINT}$
A0	9	32	$\overline{CS}$
D0	10	31	D7
D1	11	30	D6
D2	12	29	D5
NC	13	28	D4
NC	14	27	D3
VDD	15	26	VDD
VSS	16	25	VSS
NC	17	24	NC
NC	18	23	NC
NC	19	22	NC
NC	20	21	NC

40-pin ceramic side-braised DIP

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin	Symbol	Function	Description
1	XONE	OUTPUT	Bipolar modulated serial output data
2	XZERO	OUTPUT	Bipolar modulated serial output data
3	R1ONE	INPUT	Receiver 1 input data
4	R1ZERO	INPUT	Receiver 1 input data
5	R2ONE	INPUT	Receiver 2 input data
6	R2ZERO	INPUT	Receiver 2 input data
7	A2	INPUT	Address Line Bit 2
8	A1	INPUT	Address Line Bit 1
9	A0	INPUT	Address Line Bit 0
10	D0	I/O	Data Line Bit 0
11	D1	I/O	Data Line Bit 1
12	D2	I/O	Data Line Bit 2
13	NC	-	No Connect
14	NC	-	No Connect
15	V_{DD}	POWER	5 Volts ±10%
16	V_{SS}	GROUND	Ground – Reference for all signals
17	NC	-	No Connect
18	NC	-	No Connect
19	NC	-	No Connect
20	NC	-	No Connect
21	NC	-	No Connect
22	NC	-	No Connect
23	NC	-	No Connect
24	NC	-	No Connect
25	V_{SS}	GROUND	Ground – Reference for all signals
26	V_{DD}	POWER	5 Volts ±10%
27	D3	I/O	Data Line Bit 3
28	D4	I/O	Data Line Bit 4
29	D5	I/O	Data Line Bit 5

Pin	Symbol	Function	Description
30	D6	I/O	Data Line Bit 6
31	D7	I/O	Data Line Bit 7
32	$\overline{CS}$	INPUT	Chip Select (Low True)
33	$\overline{RINT}$	OUTPUT	Receiver Interrupt
34	V_{SS}	GROUND	Ground – Reference for all signals
35	V_{DD}	POWER	5 Volts ±10%
36	$\overline{XINT}$	OUTPUT	Transmitter Interrupt
37	$\overline{RST}$	INPUT	Reset (Low True)
38	CLOCK	INPUT	1, 6, or 12 MHz input clock
39	$\overline{RD}$	INPUT	Read Strobe (Low True) (Data clocked on trailing edge)
40	$\overline{WR}$	INPUT	Write Strobe (Low True) (Data clocked on trailing edge)

ARINC 429 DATA FORMAT AND READ/WRITE CYCLES

The ARINC 429 specification defines the 32-bit word as shown in Figure 1, indicating the order in which bits appear on the ARINC 429 data bus. ARINC bit 1 is defined as the label MSB, whereas the data field MSB is bit 31 as shown below.
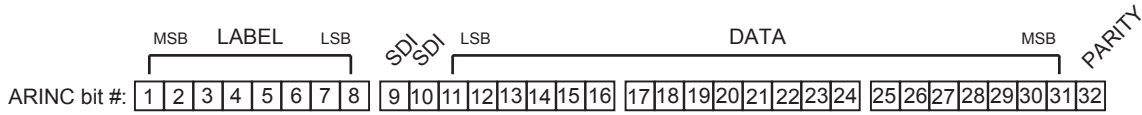

Figure 1. ARINC 429 Data Format.

Read/write operations to the HI-6011 are performed via 3 address pins, A2:0, and 8 data pins, D7:0. The address pins A2:0 specify the possible read/write operations (see Section "Read/Write Operations"). The 32-bit ARINC word is communicated using 4 successive reads or writes over the 8-bit data bus as follows:

Table 2. Order of ARINC 429 word bits during read/write cycles.

Read/Write Cycle	ARINC 429 bits	Data Pins D7:0
1	Bits 1-8 (Label)	Bit 1 = D0, Bit 8 = D7
2	Bits 9-16	Bit 9 = D0, Bit 16 = D7
3	Bits 17-24	Bit 17 = D0, Bit 24 = D7
4	Bits 25-32	Bit 25 = D0, Bit 32 = D7

READ/WRITE OPERATIONS

Read/write operations to the HI-6011 are performed via 3 address pins, A2:0, and 8 data pins, D7:0. The chip select pin, $\overline{CS}$, must be held low during all read/write operations. A single byte read is enabled by pulling the $\overline{RD}$ pin low. Subsequent byte reads are performed by cycling $\overline{RD}$ high and then low for each additional byte read. Similarly, byte writes are enabled in the same way by pulling the $\overline{WR}$ pin low and cycling high and then low for each additional byte write. Table 3 and Table 4 summarize the address pins state for each permissible read and write operation respectively.

Table 3. Address pins A2:0 state for permissible read operations

Read to HI-6011: ($\overline{CS}$ = 0, $\overline{RD}$ = 0)	
A2:0	**Description**
000	Read Interrupt Status Register. See Section "Interrupt Status Register".
001	Read Receiver 1 data. The 32-bit ARINC word is read using 4 successive reads over the 8-bit parallel bus, as outlined in Table 2. $\overline{RD}$ must be pulled low for the first byte read and then cycled high and low for subsequent byte reads. $\overline{CS}$ should be held low during the entire 4-byte cycle. If more than four reads are issued, the fifth re-reads the data originally read on the first read, etc.).
010	Read Receiver 2 data. Same operation as Receiver 1 above.
011	Read Transmitter/General Status Register. See Section "Transmitter/General Status Register".
1xx	No function. Returns all zeros.

Table 4. Address pins A2:0 state for permissible write operations

Write to HI-6011: ($\overline{CS}$ = 0, $\overline{WR}$ = 0)	
A2:0	**Description**
000	Write Transmit FIFO. The 32-bit ARINC word is written to the transmit FIFO using 4 successive writes over the 8-bit parallel bus, as outlined in Table 2. $\overline{WR}$ must be pulled low for the first byte write and then cycled high and low for subsequent byte writes. $\overline{CS}$ should be held low during the entire 4-byte cycle. Bit 32 will be automatically overwritten with the correct parity. Up to 5 32-bit words may be queued in the transmit FIFO. A minimum of 8µs must be allowed between the last byte of each word (write cycle 4) and the first byte of the next word (write cycle 1). See Section "Transmit FIFO Operation".

HI-6011

	Write to HI-6011: ($\overline{CS}$ = 0, $\overline{WR}$ = 0)
001	Write Receiver 1 ID Label Register. The Receiver ID Label Register bits are written in the same way as outlined in Table 2 for read/write cycle 1. Two modes of operation are possible for the label ID. **Mode 0:** Mode 0 is enabled by writing all zeros to the Receiver ID Label Register. In this mode, any ID label is accepted and the most recent word overwrites unread previously received word. **Mode 1:** Mode 1 is enabled when any non-zero value is written to the Receiver ID Label Register. In this mode, only received labels matching the written ID label are responded to. The first word in is retained forever until read or until receiver 2 is reset. Any ID label write (same data or different) causes receiver 1 to reset. See Section "Receiver Operation" for further information.
010	Write Receiver 2 ID Label Register. Same operation as Receiver 1 above.
011	Write Control Word Register. See Section "Control Word Register".
1xx	Master Reset. Resets the chip, irrespective of data. Ceases all transmission; re-initializes receivers. Does not change setup parameters. **Note:** A reset to the receivers or a master reset should be given following a change to data rate, parity or input clock specification. A hardware function $\overline{RST}$ is provided which performs the same functions as the software controlled reset.

REGISTER DESCRIPTIONS

Control Word Register

Bits	Description
0	Reset Receiver 1. Used to reset Receiver 1 at any time. Assert and remove a "1" to reset Receiver 1. **Note:** Reset will destroy any word being received at the time of the reset. "1" = reset. Reset must be removed to enable receiver. Receiver function inhibited by a high level on reset.
1	Reset Receiver 2 – Same as for receiver 1.
2	Establish parity. 1 = ODD; 0 = EVEN. Both receivers and the transmitter must use the same parity.
3	Set Receiver 1 Data Rate: 0 = LOW (12-14.5 kbps); 1 = HIGH (100 kbps).
4	Set Receiver 2 Data Rate: Save as for Receiver 1.
5	Set Transmitter Data Rate. Same as for Receiver 1. **Note:** Data rates for the transmitter and individual receivers are independent.
7:6	Specifies Input Clock. <table><tr><td>00</td><td>12 MHz</td><td></td></tr><tr><td>01</td><td>6 MHz</td><td></td></tr><tr><td>1x</td><td>1 MHz</td><td></td></tr></table>

Interrupt Status Register

Bits	Description
0	"1" = Receiver 1 has received word.
1	"1" = Receiver 1 word has a parity error.
2	"1" = Receiver 1 error (32 bits received before idle state).
3	"1" = Receiver 2 has received word.
4	"1" = Receiver 2 word has a parity error.
5	"1" = Receiver 2 error (32 bits received before idle state).
6	"1" = Transmitter buffer and FIFO entirely empty (Up to 5 words may be written to transmitter). .
7	"1" = Transmitter FIFO full. Do not write more words to transmit FIFO. (Words written while this bit is set will be ignored). "0" = FIFO has room for at least 1 word.

Transmitter/General Status Register

Bits	Description		
0	XMIT Data.		
1	XMIT Clock (Data changes on the rising edge).		
2	Parity Sense (1 = ODD, 0 = EVEN).		
3	Receiver 1 data rate: 0 = LOW (12-14.5 kbps); 1 = HIGH (100 kbps).		
4	Same as bit 3 for receiver 2.		
5	Transmitter Data Rate: 0 = LOW (12-14.5 kbps); 1 = HIGH (100 kbps).		
7:6	Input Clock Selection		
	00	12 MHz	
	01	6 MHz	
	1x	1 MHz	

RECEIVER OPERATION

Mode 0 Operation

This mode is established by presetting the receiver's ID label to 00H. In this mode the receiver accepts all data words transmitted to it. The receiver calculates incoming parity, compares it to the received parity bit and provides a status bit to indicate the correctness of the received parity. Any premature (before 32 bits are received) idle line condition resets the receiver and sets a status bit which is retained until a full word is received or until a reset is issued. Receipt of a full 32-bit word activates the interrupt and sets a status bit.

A 2µs open drain negative pulse is produced as an interrupt to the processor to indicate a full word has been received. The processor responds to the interrupt by reading interrupt status to determine what event caused the interrupt, to determine correctness of parity (if applicable) and to react to transmitter state. To read a received word, four successive reads are required. The first brings bits 1-8 to the data bus, the second brings bits 9-16, etc. A reset for the receiver being handled may be issued after reading the data, if such reset occurs before the first bit of the next word is received. If another read of the receiver data is issued after a reset, the most recent received word will again be read (until another word is received and the receive interrupt and corresponding status bits are thereby re-activated).

In mode 0, if another word is received before the current one has been read, the most recent word received replaces the previous unread one and causes another receive interrupt. This allows the processor a maximum of 2.2 ms (14.5 kpbs) or 0.32 ms (100 kbps) to respond to assure no loss of data if there is full speed throughput.

In Mode 0, the processor must read the received word before the next received word's parity bit (bit 32) arrives. If a read of one word is in progress during the end of the receiving procedure (bits 32, 33) of the next word, data may not be correct.

Mode 1 Operation:

Any non-zero byte written to a receiver's ID label register activates this mode and causes a receiver reset. Mode 1 functions identically to mode 0 except that the interrupt is generated only if the address label of the received word matches that of the preset ID label. Also, if the interrupt for the received word has not been handled by the time a subsequent word arrives, the first received word is retained. Retention is indefinite (until a reset is issued).

TRANSMIT FIFO OPERATION

One Transmit channel is provided. Outputs are as follows:

Data	Asserted Output	Negated Output
Idle	LO	LO
1	Pulses HI (RZ)	LO
0	LO	Pulses HI (RZ)

A FIFO buffer allows five transmit words to be queued up while a preceding one is being serialized. These may be written to the HI-6011 with a minimum of 8µs between the last byte write (fourth) of one word and the first byte write of the next word. The interrupt is activated when the FIFO is full and no more transmit words can be written (any written under this condition are ignored and thus, lost).

The Interrupt is also activated when the transmitter becomes empty, a condition when six words may be written to the FIFO system.

To write a word to the transmitter, status should first be checked to determine if the FIFO can except data. Then four consecutive writes are performed: the first is for bits 1-8, the second for bits 9-16, etc. Bit 1 is the first transmitted bit in the serial stream followed sequentially by bit 2 through 32. Data written to the transmitter must be stable during the trailing (rising) edge of $\overline{WR}$.

The transmitter inserts the proper parity bit on transmitted words. Bit 32 written to the transmitter is ignored.

INTERRUPTS

Two low true interrupts ($\overline{RINT}$ and $\overline{XINT}$) are provided on separate output pins. These are open drain outputs which may be "wire OR'd" together. Each pin is capable of sinking 4mA.

$\overline{RINT}$ is pulsed LOW ('0') for 2µs by either of the following conditions:

1. Receiver 1 has received a word – INT status retained until explicitly reset or until another word is received in mode 0.
2. Receiver 2 has received a word – INT status retained until explicitly reset or until another word is received in mode 0.

$\overline{XINT}$ is pulsed low for 2µs by either of the following conditions:

1. Transmitter FIFO and serializer completely empty (6 words may be written to it).
2. Transmitter buffer is full.

$\overline{RINT}$ and $\overline{XINT}$ are intended for use as edge activated signals. The Interrupt Status Register must be read to determine the source of the interrupts.

A reset (hardware or software) will not cause a $\overline{XINT}$ for transmitter empty. The controller should know this transmitter status exists by virtue of intentionally issuing such a reset.
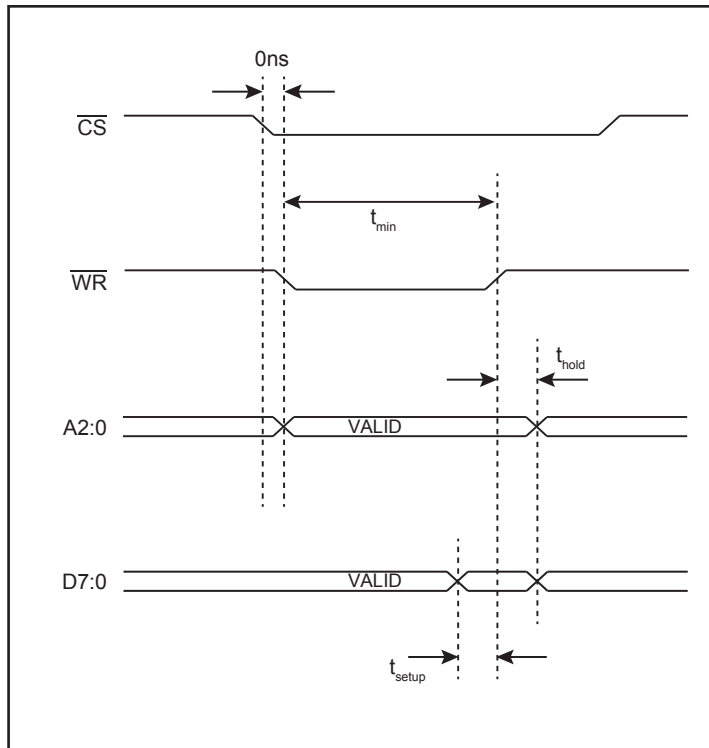
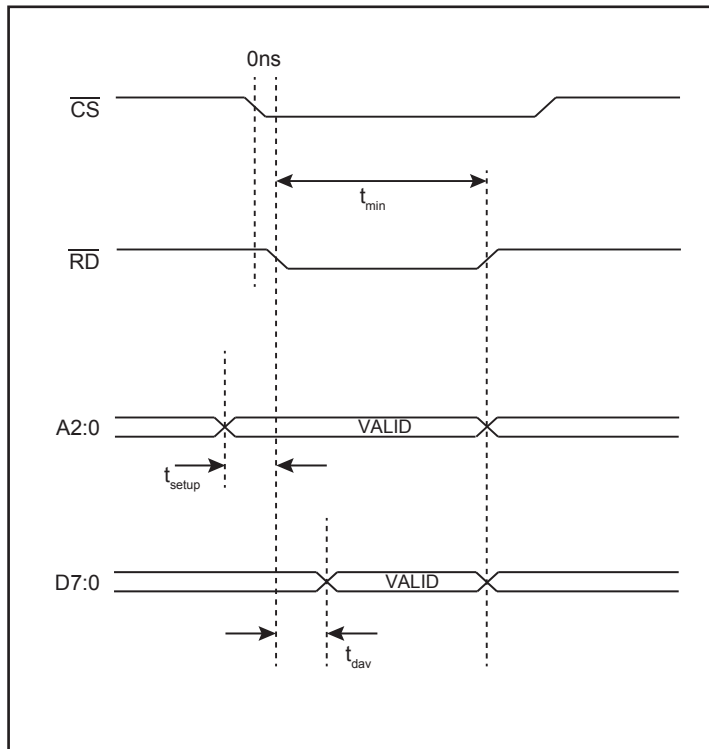## TIMING DIAGRAMS

Figure 2. Write cycle.

Figure 3. Read cycle.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Supply voltage (V_{DD}):	-0.5 V to +7.0 V	Power dissipation at 25°C:	500 mW
Input voltage range (V_{IN}):	-0.5 V to (V_{DD} + 0.5 V)	Operating Temp. Range:	Industrial: -40°C to +85°C Extended: -55°C to +125°C
Input current (I_{IN}):	+10mA	Lead Temperature:	300°C for 60 sec.
Output current (I_{OUT}):	+25mA	Storage Temperature:	-65°C to +150°C

DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Min. input voltage (HI)	V_{IH}		2.1	1.4		V
Max. input voltage (LO)	V_{IL}			1.4	0.7	V
Min. input current (HI)	I_{IH}	V_{IH} = 4.9V			1.5	µA
Max. input current (LO)	I_{IL}	V_{IL} = 0.1V	-1.5			µA
Min. output voltage (HI)	V_{OH}	I_{OUT} = -1.5mA	2.7			V
Max. output voltage (LO)	V_{OL}	I_{OUT} = +1.8mA			0.7	V
Supply current	I_{DD}	f = 400KHz		0.8	2.8	mA

AC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Hold time (both address and data)	t_{hold}		50			ns
Set-up time	t_{setup}		50			ns
Time to data valid	t_{dav}		50			ns
Minimum active $\overline{RD}$ / $\overline{WR}$ cycle	t_{min}	3x clock period	3			µs

REVISION HISTORY

Revision	Date	Description of Change
DS6011, Rev. New	10/5/12	Initial Release

ORDERING INFORMATION

HI - 6011 <u>Cx</u> <u>x</u>

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
T	-55°C to +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH
CD	40-pin ceramic side-braised DIP	Gold

Note 1: Gold Terminal finish is Pb-Free, RoHs compliant

PACKAGE DIMENSIONS

40-PIN CERAMIC SIDE-BRAISED DIP

inches (millimeters)

Package Type 40C

$\frac{2.020}{(51.308)}$ max

$.610 \pm .010$ $\overline{(15.494 \pm .254)}$

$.595 \pm .010$ $\overline{(15.113 \pm .254)}$

$\frac{.050}{(1.270)}$ typ

$\frac{.225}{(5.715)}$ max

$.085 \pm .009$ $\overline{(2.159 \pm .229)}$

$.600 \pm .010$ $\overline{(15.240 \pm .254)}$

$\frac{.125}{(3.175)}$ min

$\frac{.018}{(.457)}$ typ

$\frac{.100}{(2.54)}$ BSC

$.010 +.002/-.001$ $\overline{(.254 +.051/-.025)}$

BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)