

Preliminary

Notice: This is not a final specification.
Some parametric limits are subject to change.

Renesas LSIs

M6MGD137W34DKT

134,217,728-BIT (8,388,608-WORD BY 16-BIT) CMOS FLASH MEMORY &
33,554,432-BIT (2,097,152-WORD BY 16-BIT) CMOS mobileRAM
Stacked- mMCP (micro Multi Chip Package)

DESCRIPTION

The M6MGD137W34DKT is a Stacked micro Multi Chip Package (S- μ MCP) that contains 128M-bit Flash memory and 32M-bit mobileRAM in a 52-pin TSOP for lead free use.

128M-bit Flash memory is a 8,388,608 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

32M-bit mobileRAM is a 2,097,152 words high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM.

The cells are automatically refreshed and the refresh control is not required for system. The device also has the partial block refresh scheme and the power down mode by writing the command.

The M6MGD137W34DKT is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

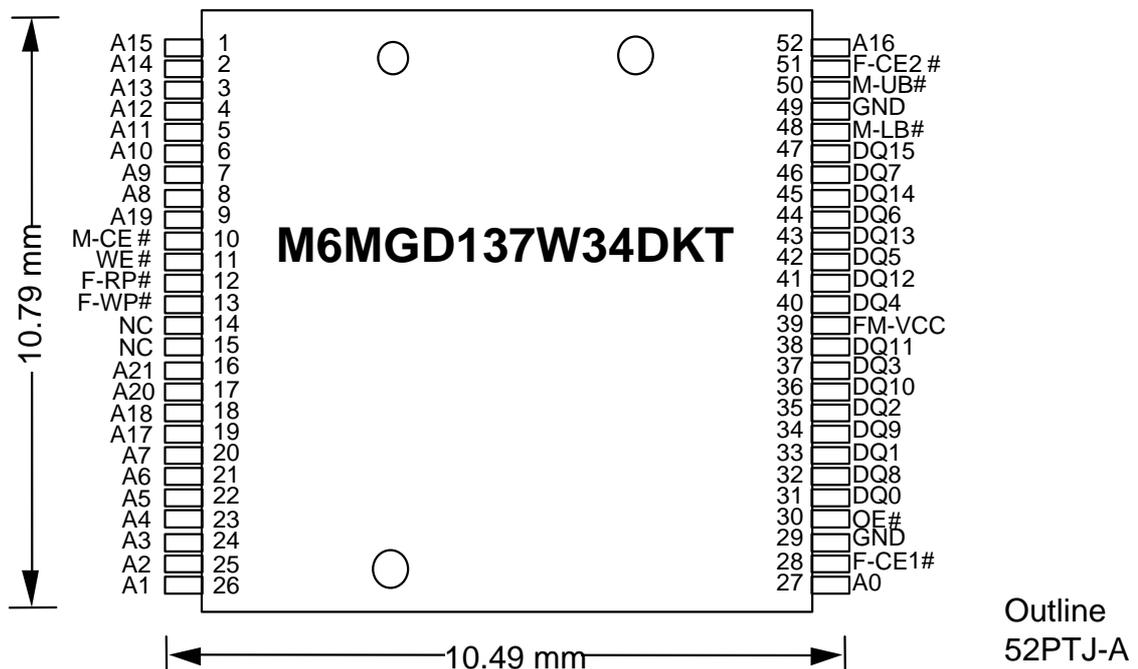
FEATURES

Access time	Flash	70ns (Max.)
	mobileRAM	80ns (Max.)
Supply voltage		FM-VCC = 2.7 ~ 3.0V
Ambient temperature		Ta=-40 ~ 85 °C
Package		52pin TSOP(Type-II), Lead pitch 0.4mm Outer-lead finishing:Sn-Cu

APPLICATION

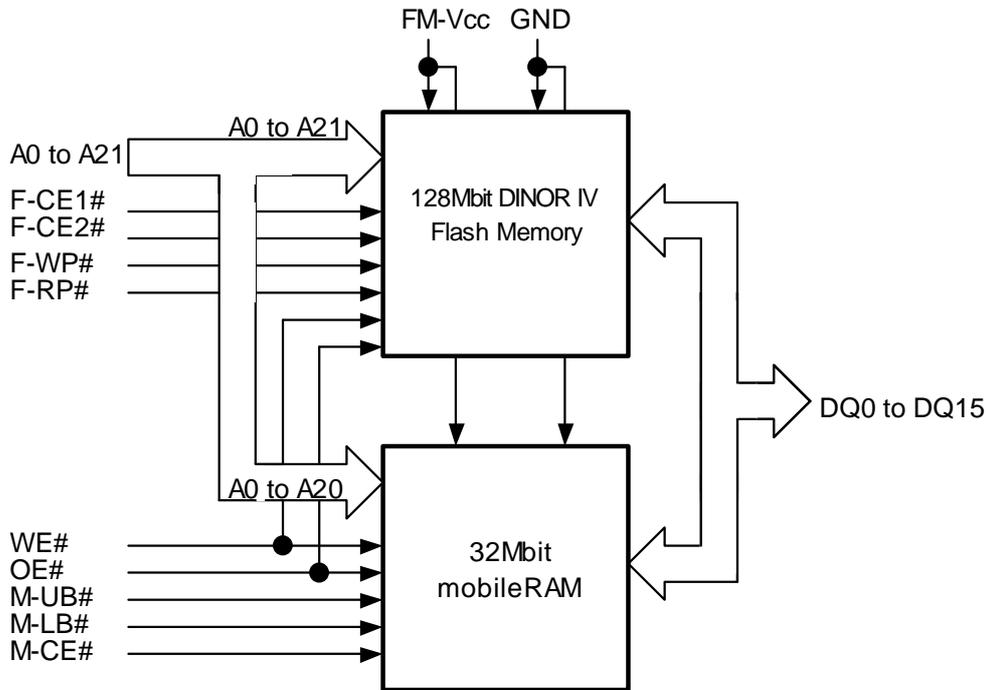
Mobile communication products

PIN CONFIGURATION (TOP VIEW)



FM-VCC	:Common VCC for Flash / mobileRAM	OE#	:Output enable for Flash/mobileRAM
GND	:Common GND for Flash / mobileRAM	WE#	:Write enable for Flash/mobileRAM
A0-A20	:Common address for Flash / mobileRAM	F-WP#	:Write protect for Flash
A21	:Address for Flash	F-RP#	:Reset power down for Flash
DQ0-DQ15	:Data I/O	M-LB#	:Lower byte control for mobileRAM
F-CE1#	:Flash chip enable1	M-UB#	:Upper byte control for mobileRAM
F-CE2#	:Flash chip enable2		
M-CE#	:mobileRAM chip enable		

MCP Block Diagram



Note: In the 128M-bit DINOR(IV) Flash Memory lower 64Mbit is selected by F-CE1#="L" and upper 64Mbit is done by F-CE2#="L". Never select each chip at the same time.
In the data sheet there are "VCC"s which mean "FM-VCC" (Common Vcc for Flash / mobileRAM).
In the Flash Memory part they mean A21, OE# and WE# are F-A21, F-OE# and F-WE#.
In the mobileRAM part UB#, LB#, OE# and WE# are M-UB#, M-LB#, M-OE# and M-WE#, respectively.

Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A21-A0, OE#, WE#, F-WP#, F-RP#, M-CE#, M-LB#, M-UB#, F-CE1#, F-CE2#	Ta=25°C, f=1MHz, Vin=Vout=0V			26	pF
							pF
							pF
							pF
COUT	Output Capacitance	DQ15-DQ0			34	pF	

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Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REJ03C0124

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New publication, effective April 2003.
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