

FDB047N10

N-Channel PowerTrench® MOSFET

100 V, 164 A, 4.7 mΩ

Description

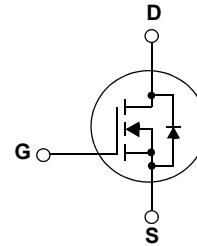
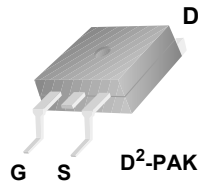
- $R_{DS(on)} = 3.9 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 75 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	FDB047N10	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	164*
		- Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	116*
		- Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	120
I_{DM}	Drain Current	- Pulsed (Note 1)	656*
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1153
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	375
		- Derate above 25°C	2.5
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDB047N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in ² pad of 2 oz copper), Max.	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB047N10	FDB047N10	D ² -PAK	330mm	24mm	800

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.1	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$	-	-	500	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 75\text{A}$	-	3.9	4.7	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}$, $I_D = 75\text{A}$	-	170	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	11500	15265	pF
C_{oss}	Output Capacitance		-	1120	1500	pF
C_{rss}	Reverse Transfer Capacitance		-	455	680	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 25\Omega$	-	174	358	ns	
t_r	Turn-On Rise Time		-	386	782	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	-	344	698	ns
t_f	Turn-Off Fall Time		(Note 4)	-	244	499	ns
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 80\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$	-	160	210	nC	
Q_{gs}	Gate to Source Gate Charge		(Note 4)	-	56	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	36	-	nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	164*	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	656	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_{SD} = 75\text{A}$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}$, $I_{SD} = 75\text{A}$	-	88	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	245	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 0.41\text{mH}$, $I_{AS} = 75\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 75\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

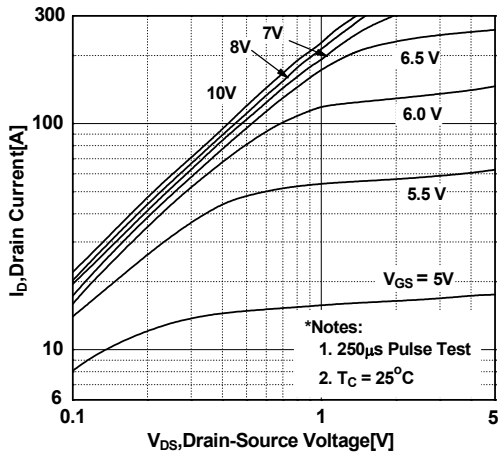


Figure 2. Transfer Characteristics

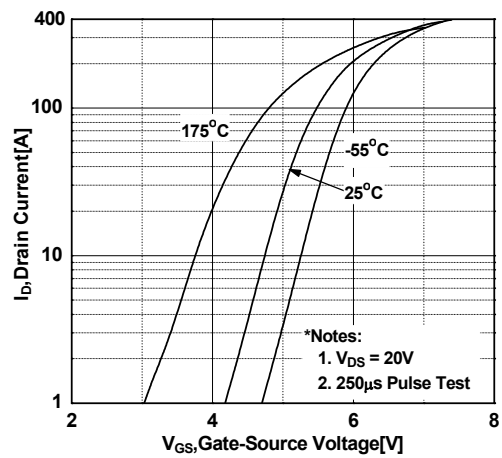


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

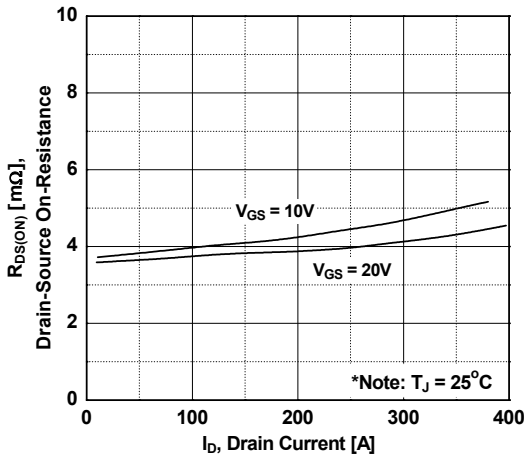


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

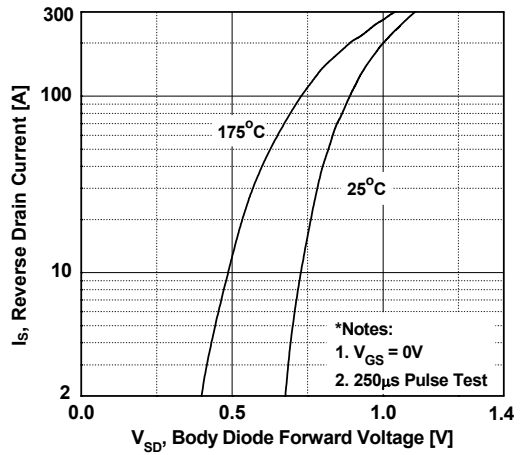


Figure 5. Capacitance Characteristics

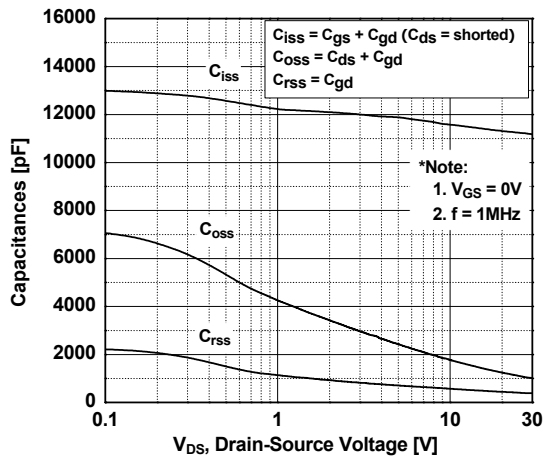
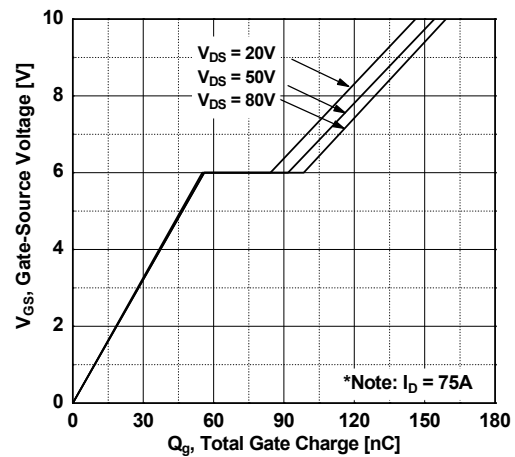


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

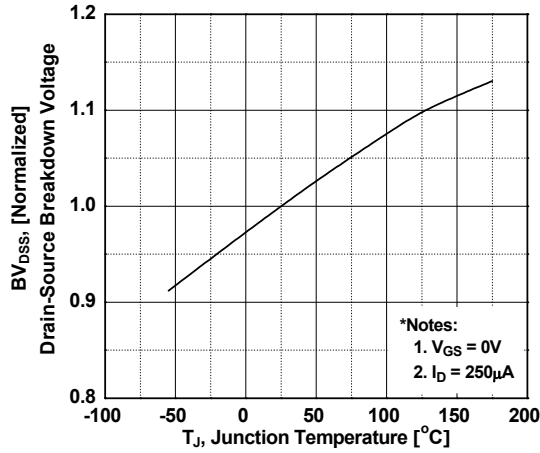


Figure 8. On-Resistance Variation vs. Temperature

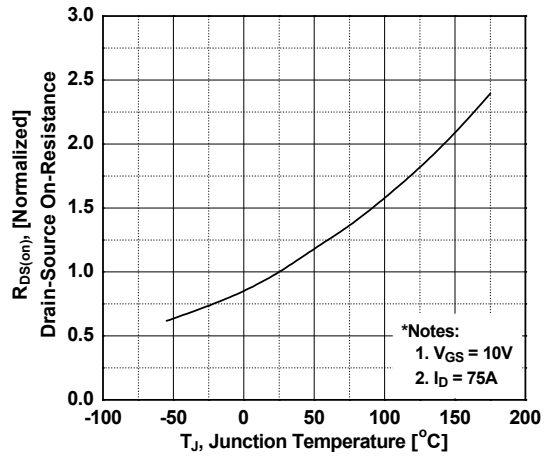


Figure 9. Maximum Safe Operating Area

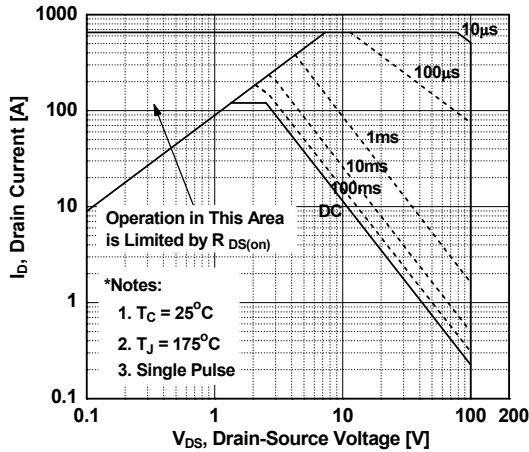


Figure 10. Maximum Drain Current vs. Case Temperature

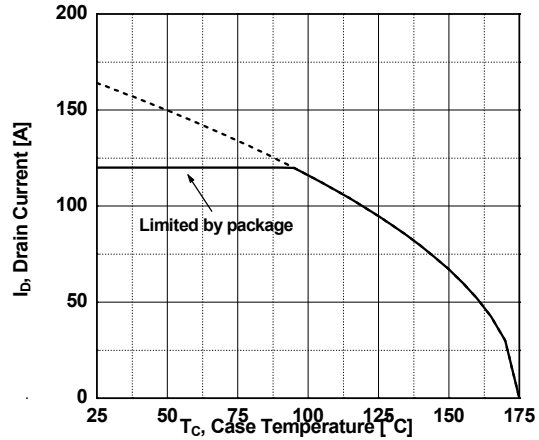
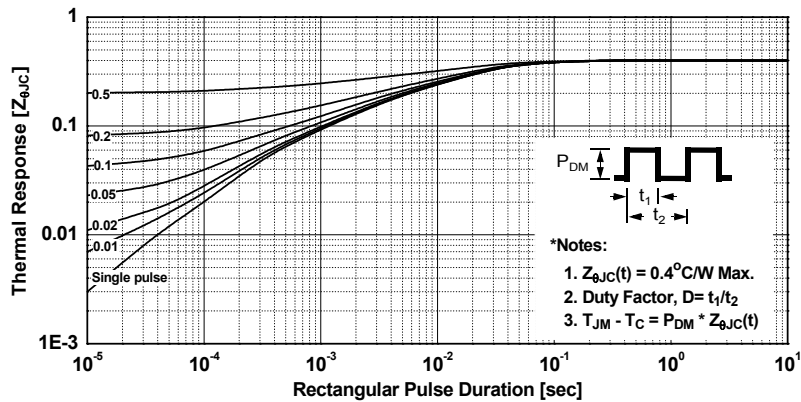
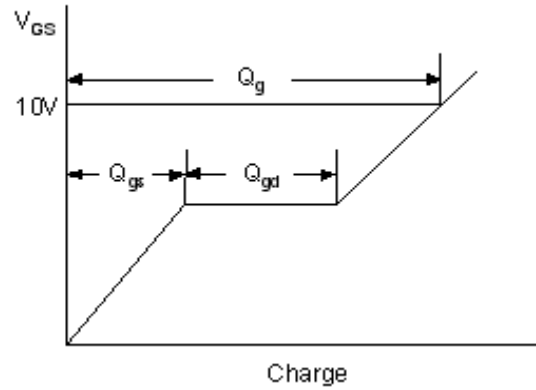
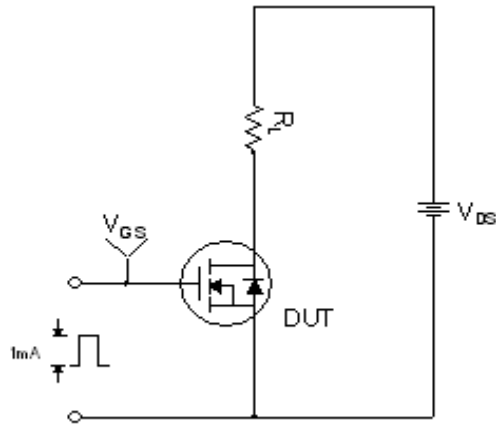


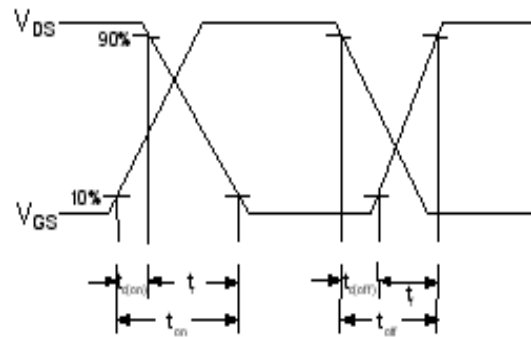
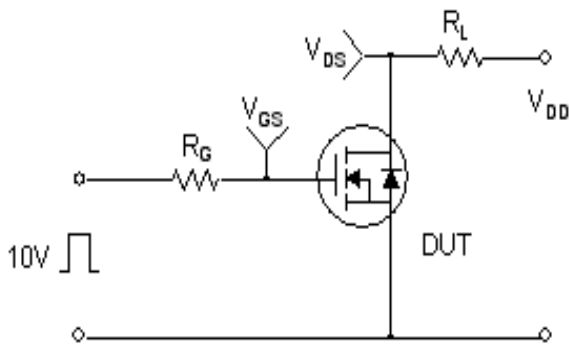
Figure 11. Transient Thermal Response Curve



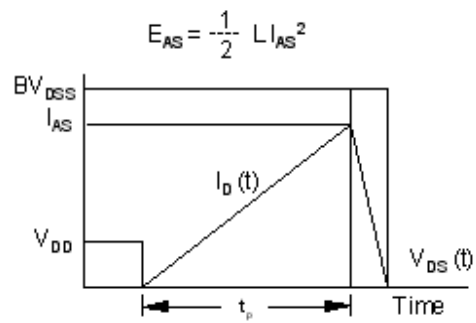
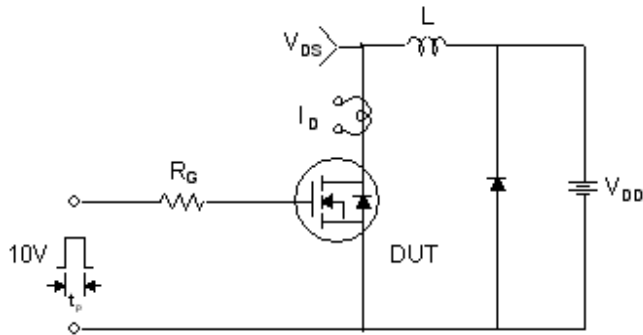
Gate Charge Test Circuit & Waveform



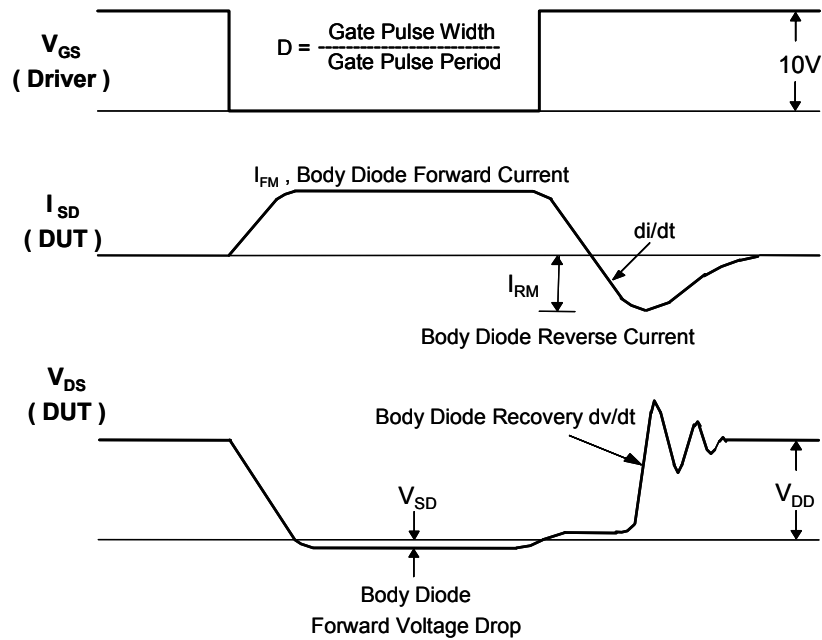
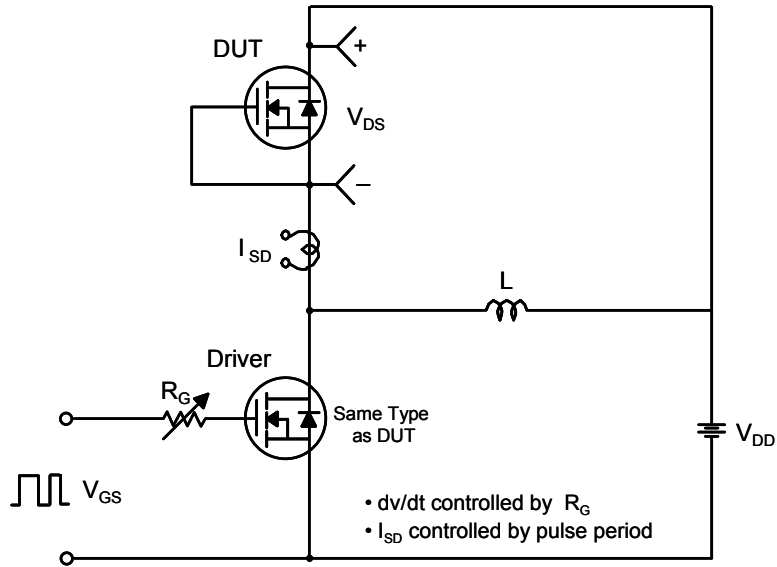
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

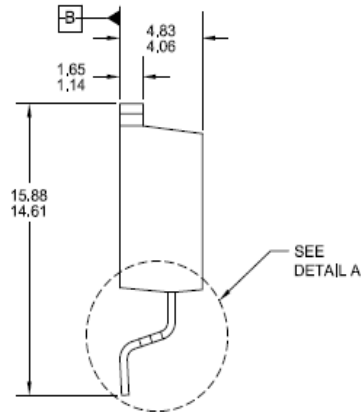
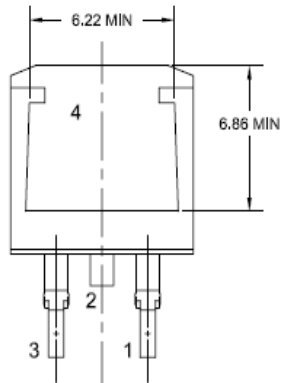
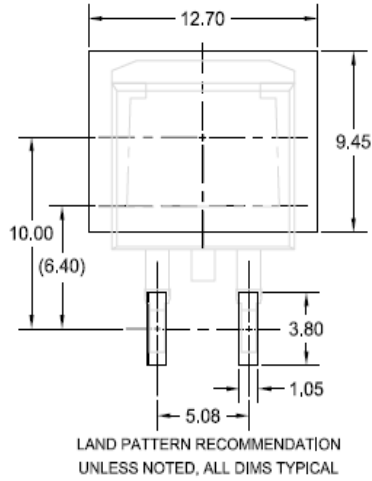
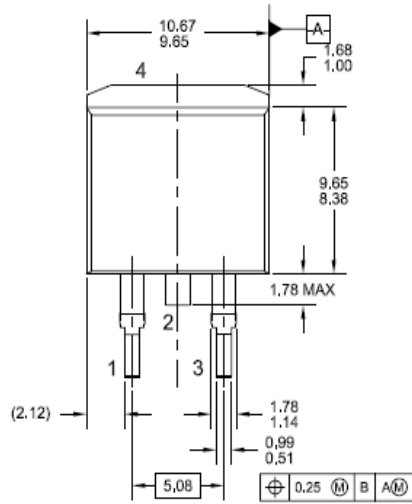


Peak Diode Recovery dv/dt Test Circuit & Waveforms

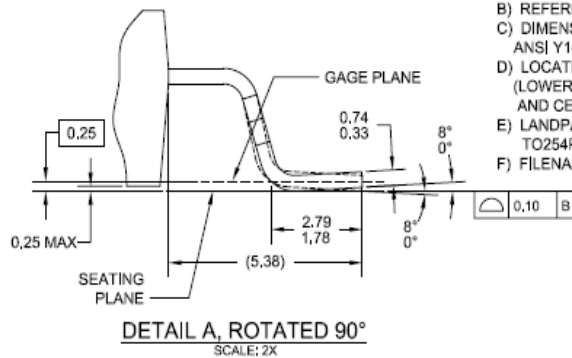


Mechanical Dimensions

D²PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) REFERENCE JEDEC, TO-263, VARIATION AB.
 C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.
 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
 F) FILENAME: TO263A02REV6




Dimensions in Millimeters
 Dimensions in Millimeters



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|---|---|----------------------------|------------------|
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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