STB6N80K5, STD6N80K5, STI6N80K5, STP6N80K5

N-channel 800 V, 1.3 Ω typ., 4.5 A MDmesh™ K5 Power MOSFETs in D²PAK, DPAK, I²PAK and TO-220 packages

Datasheet - production data

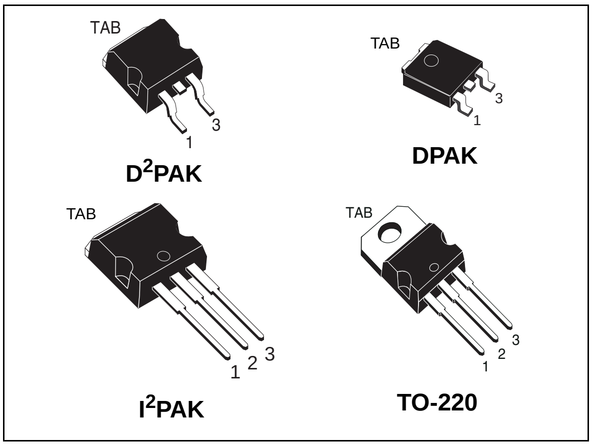
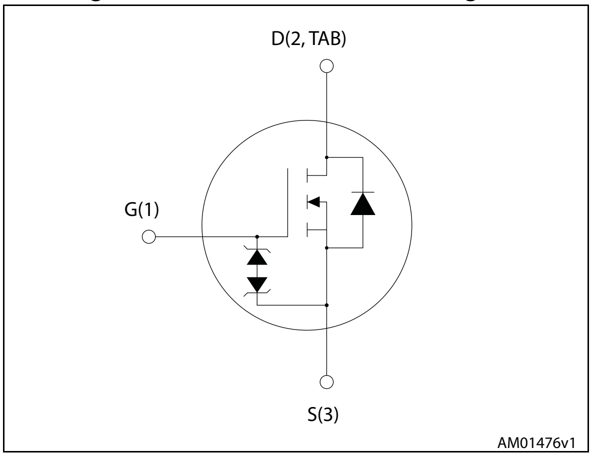


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$max	I_D	P_{TOT}
STB6N80K5	800 V	1.6 Ω	4.5 A	85 W
STD6N80K5				
STI6N80K5				
STP6N80K5				

- Industry's lowest RDS(on)
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STB6N80K5	6N80K5	D^2PAK	Tape and reel
STD6N80K5		DPAK	
STI6N80K5		I^2PAK	Tube
STP6N80K5		TO-220	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.5	A
I_D	Drain current (continuous) at T_C = 100 °C	2.8	A
I_{DM} (1)	Drain current (pulsed)	18	A
P_{TOT}	Total dissipation at T_C = 25 °C	85	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	1.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	85	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq$ 4.5 A, di/dt $\leq$ 100 A/µs, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D^2PAK	DPAK	I^2PAK	TO-220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.47				°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb			62.50	62.50	
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	30	50			

1. When mounted on FR-4 board of 1 inch², 2 oz Cu

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 800 V V_{DS} = 800 V, T_j = 125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2 A		1.3	1.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V f = 1 MHz V_{GS} = 0	-	270	-	pF
C_{oss}	Output capacitance		-	25	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V_{DS} = 0	-	38	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	16	-	pF
R_G	Intrinsic gate resistance	f = 1MHz, I_D = 0	-	7.5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 4.5 A V_{GS} = 10 V	-	13	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	nC
Q_{gd}	Gate-drain charge		-	9.6	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 2.25 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	16	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	28.5	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		18	A
V_{SD}(2)	Forward on voltage	I_{SD} = 4.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A, V_{DD} = 60 V di/dt = 100 A/µs,	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.2		µC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	I_{SD} = 4.5 A,V_{DD} = 60 V di/dt =1 00 A/µs, Tj = 150 °C	-	450		ns
Q_{rr}	Reverse recovery charge		-	3.15		µC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

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Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V(BR)GSO	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D = 0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK, TO-220 and I²PAK

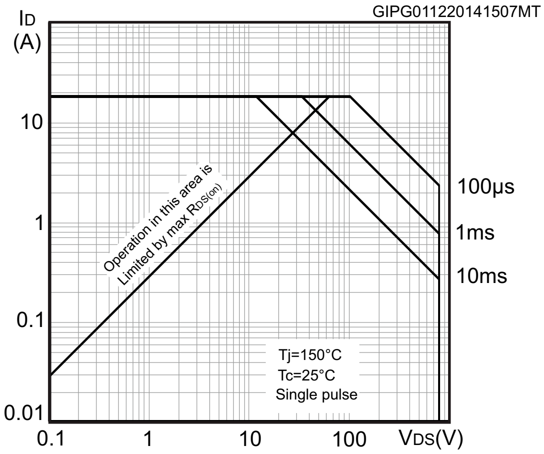


Figure 3. Thermal impedance for D²PAK, TO-220 and I²PAK

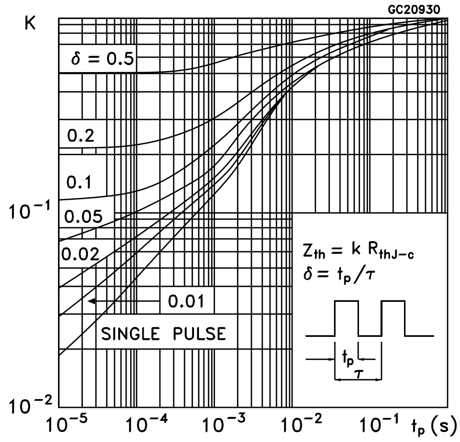


Figure 4. Safe operating area for DPAK

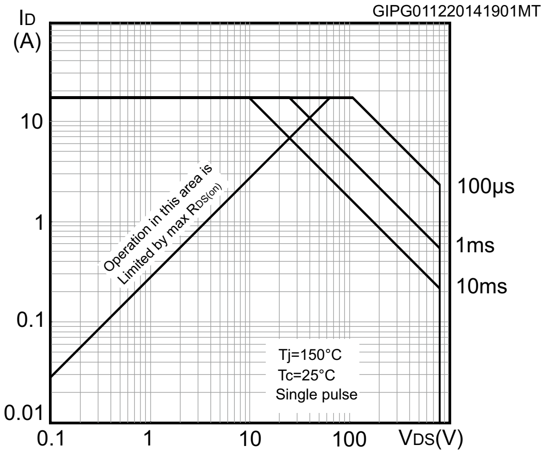


Figure 5. Thermal impedance for DPAK

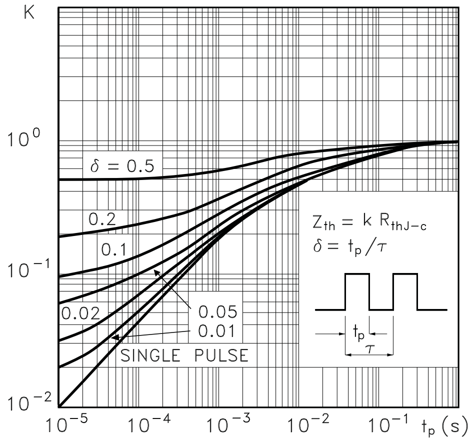


Figure 6. Output characteristics

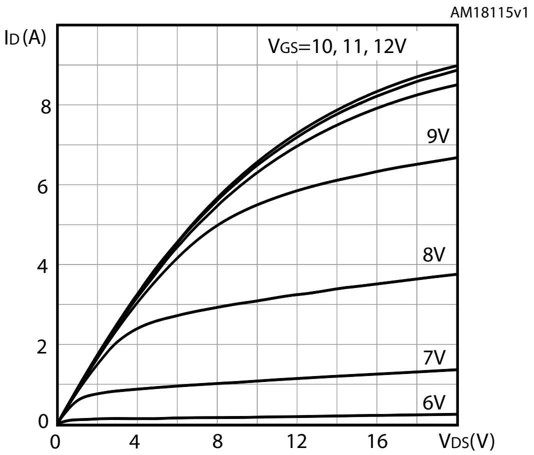


Figure 7. Transfer characteristics

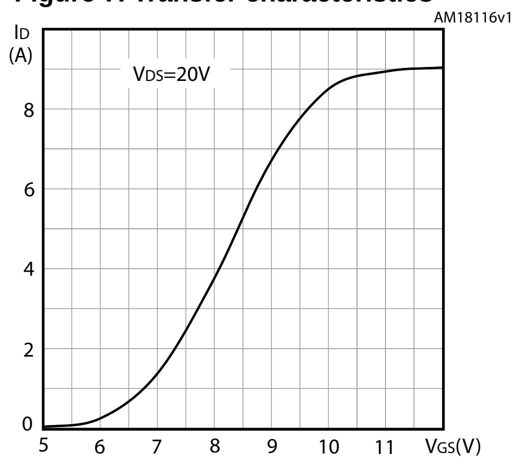


Figure 8. Gate charge vs gate-source voltage

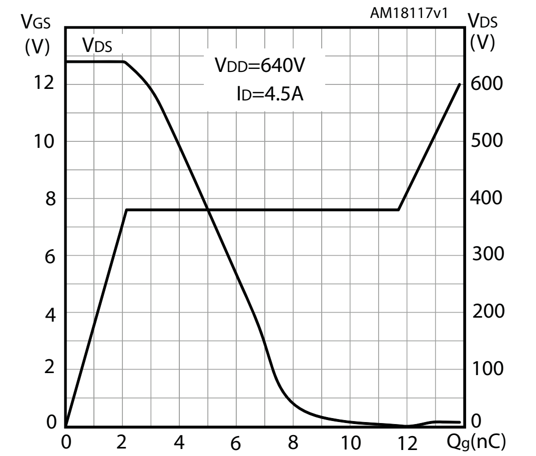


Figure 9. Static drain-source on-resistance

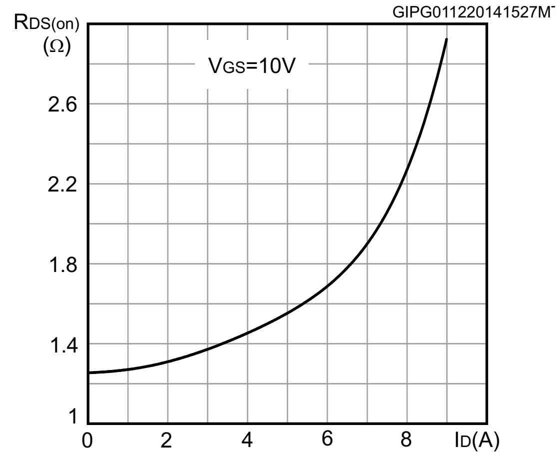


Figure 10. Capacitance variations

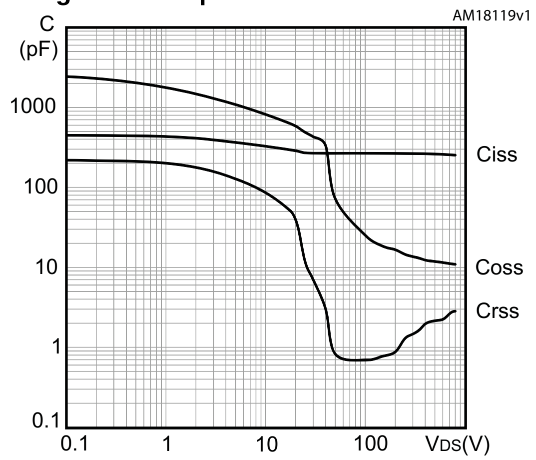


Figure 11. Output capacitance stored energy

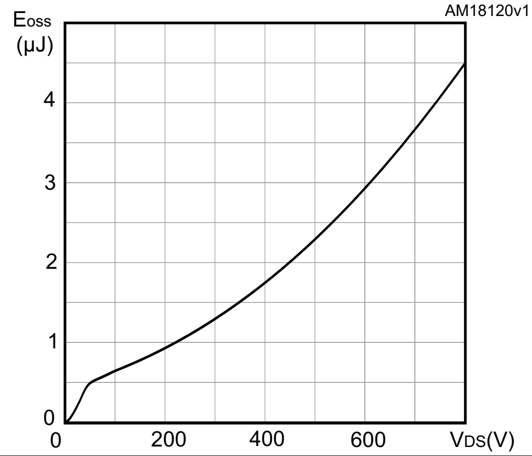


Figure 12. Normalized gate threshold voltage vs temperature

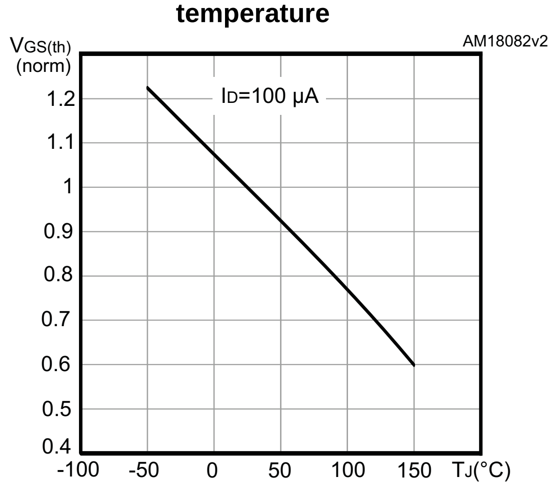


Figure 13. Normalized on-resistance vs temperature

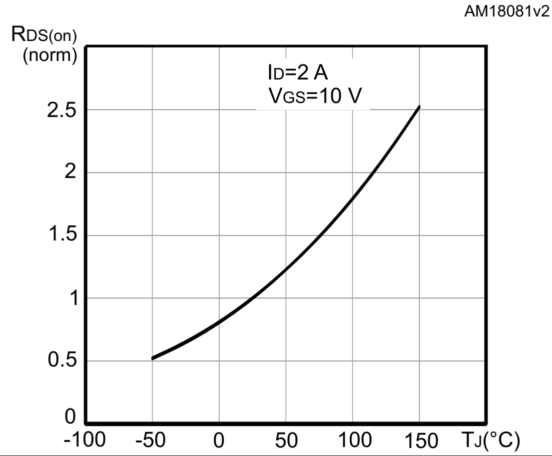


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

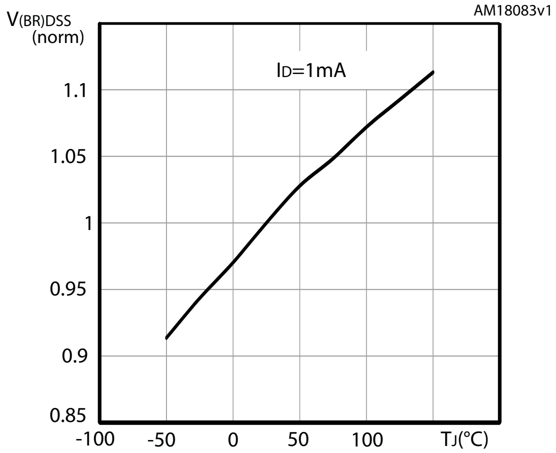
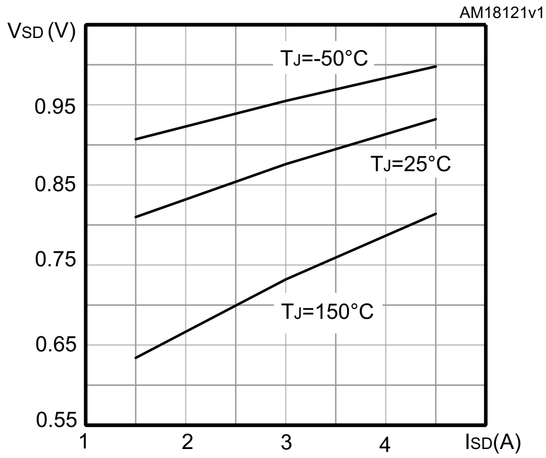


Figure 15. Source-drain diode forward characteristics



3 Test circuits

Figure 16. Switching times test circuit for resistive load

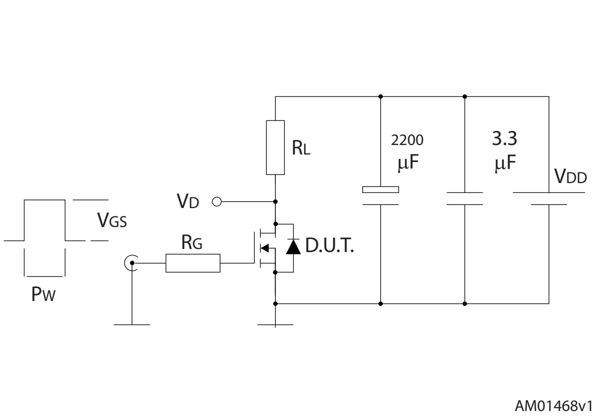


Figure 17. Gate charge test circuit

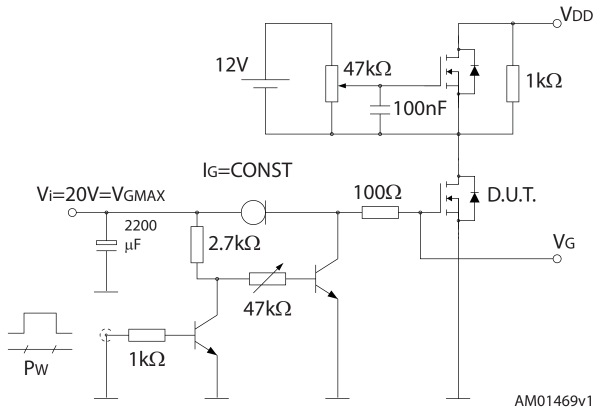


Figure 18. Test circuit for inductive load switching and diode recovery times

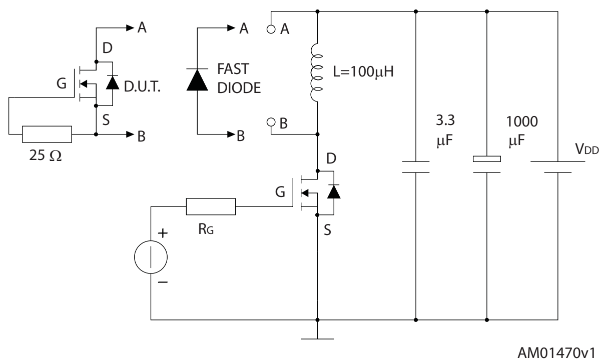


Figure 19. Unclamped inductive load test circuit

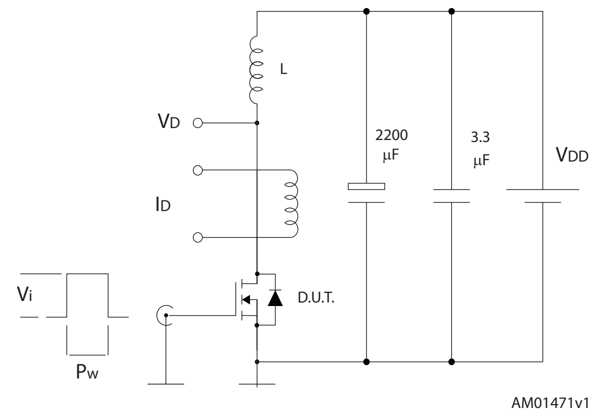


Figure 20. Unclamped inductive waveform

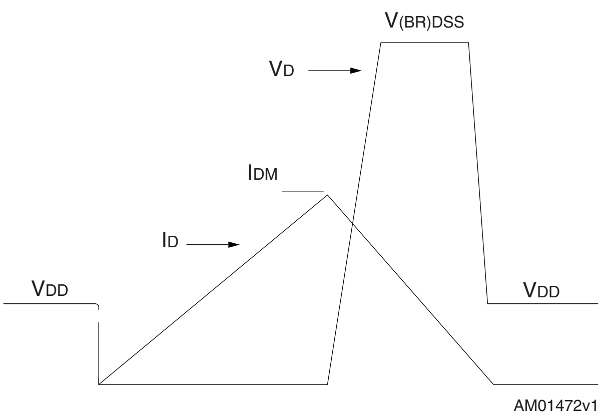
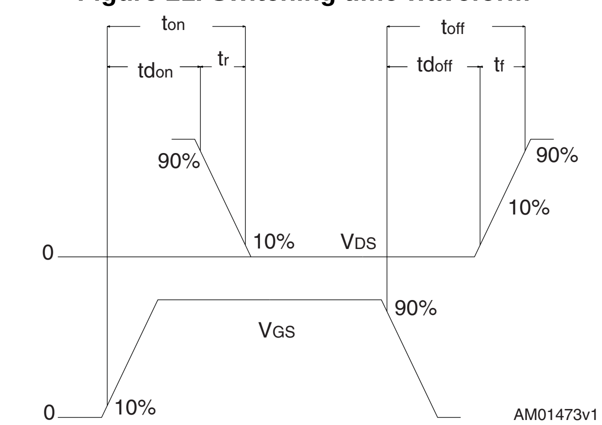


Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 D²PAK, STB6N80K5

Figure 22. D²PAK drawing

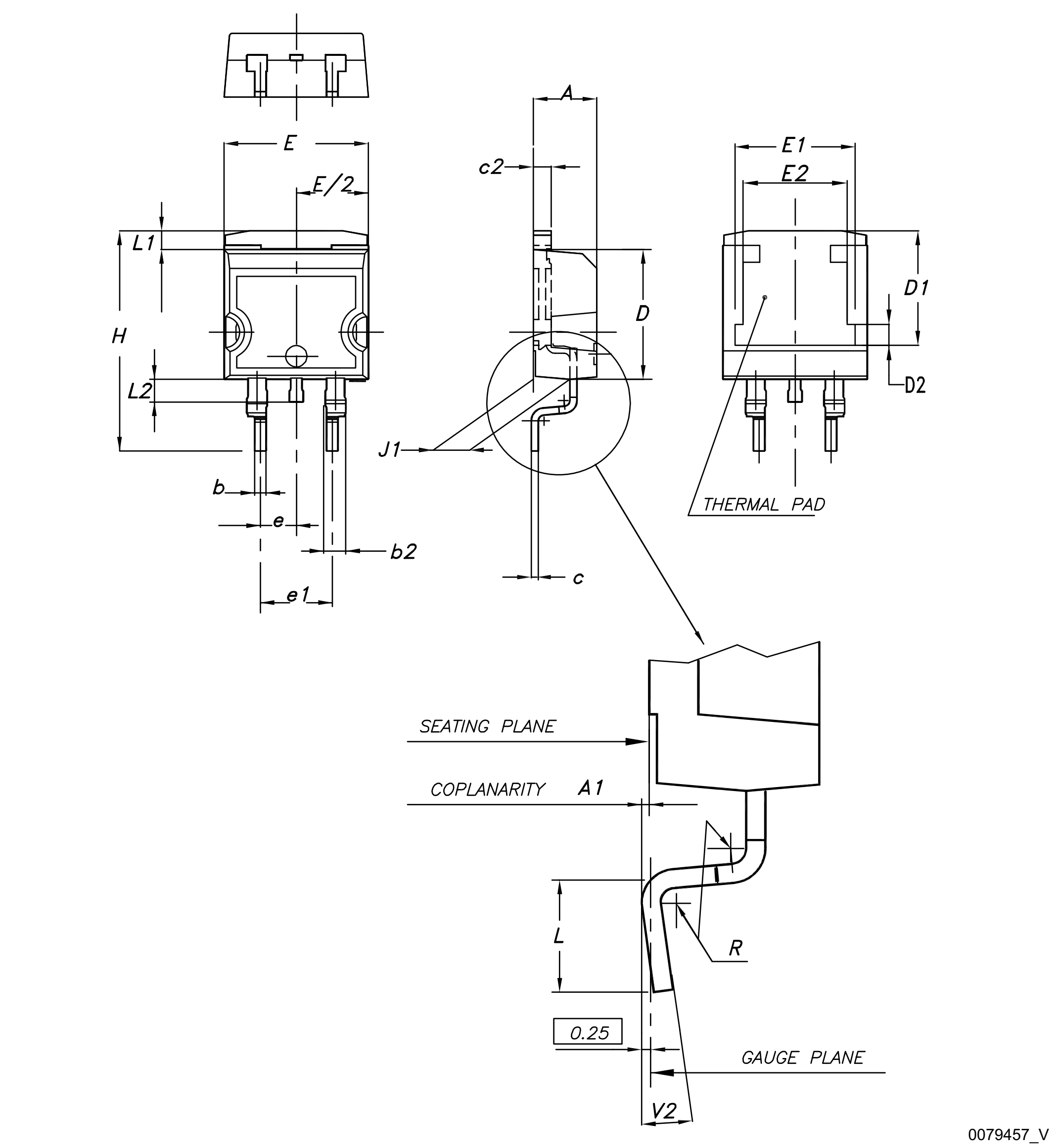
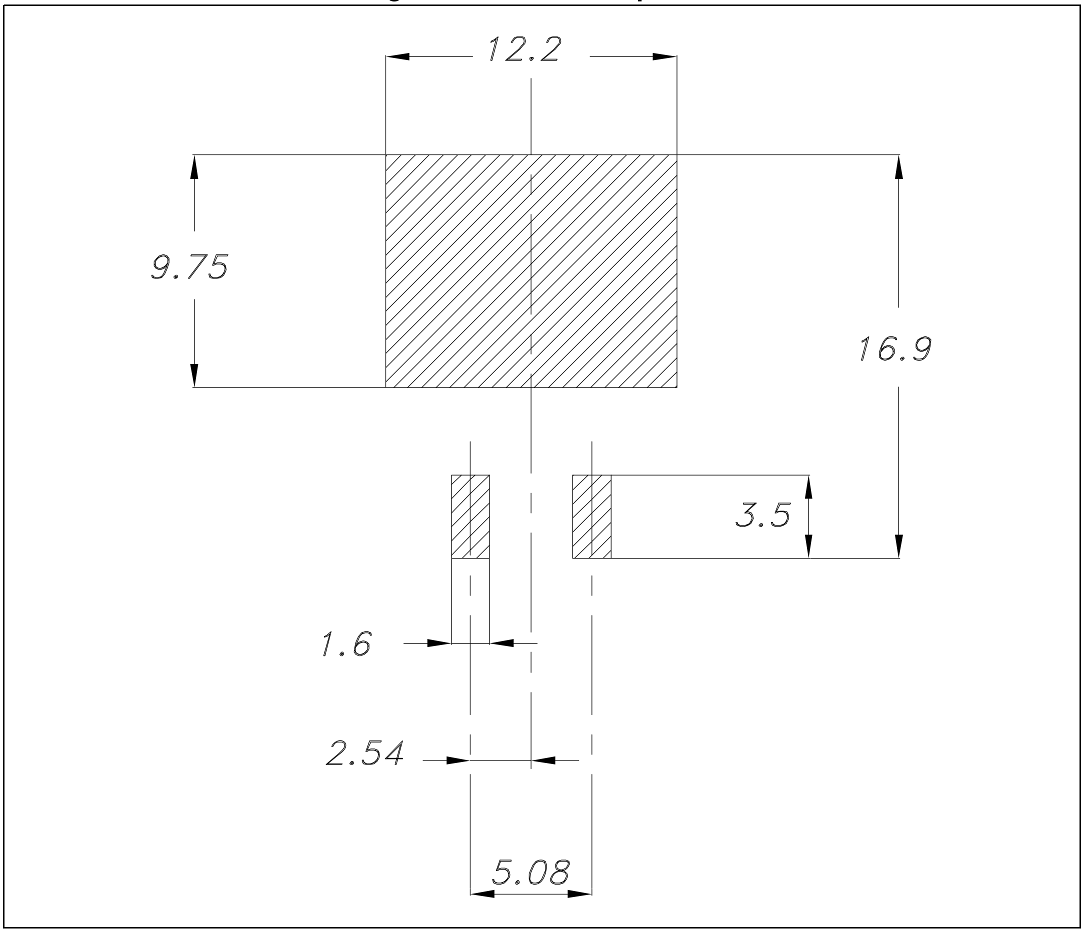


Table 9. D²PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK footprint[(a)]



a. All dimension are in millimeters

4.2 DPAK, STD6N80K5

Figure 24. DPAK type A drawing

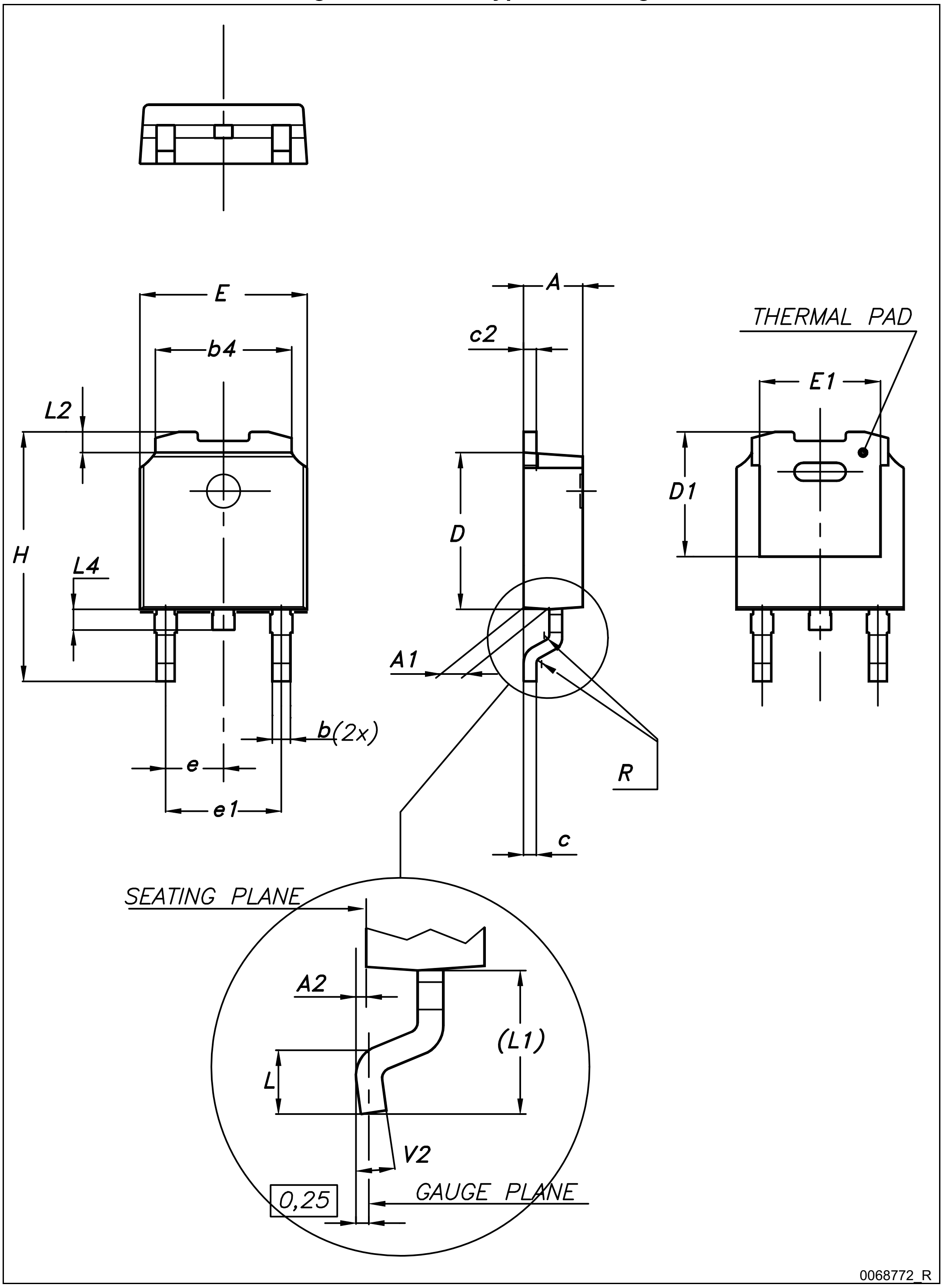
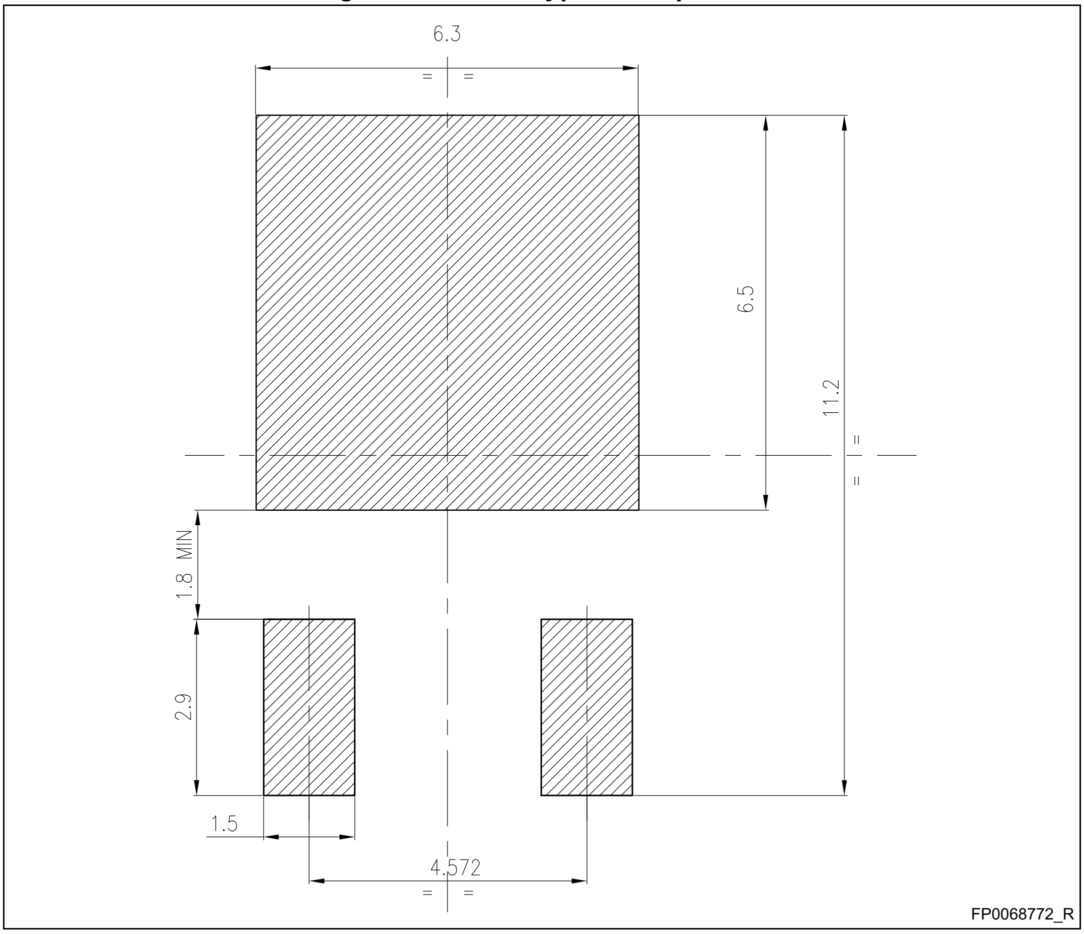


Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK type A footprint [b]



b. All dimensions are in millimeters

4.3 I²PAK, STI6N80K5

Figure 26. I²PAK drawing

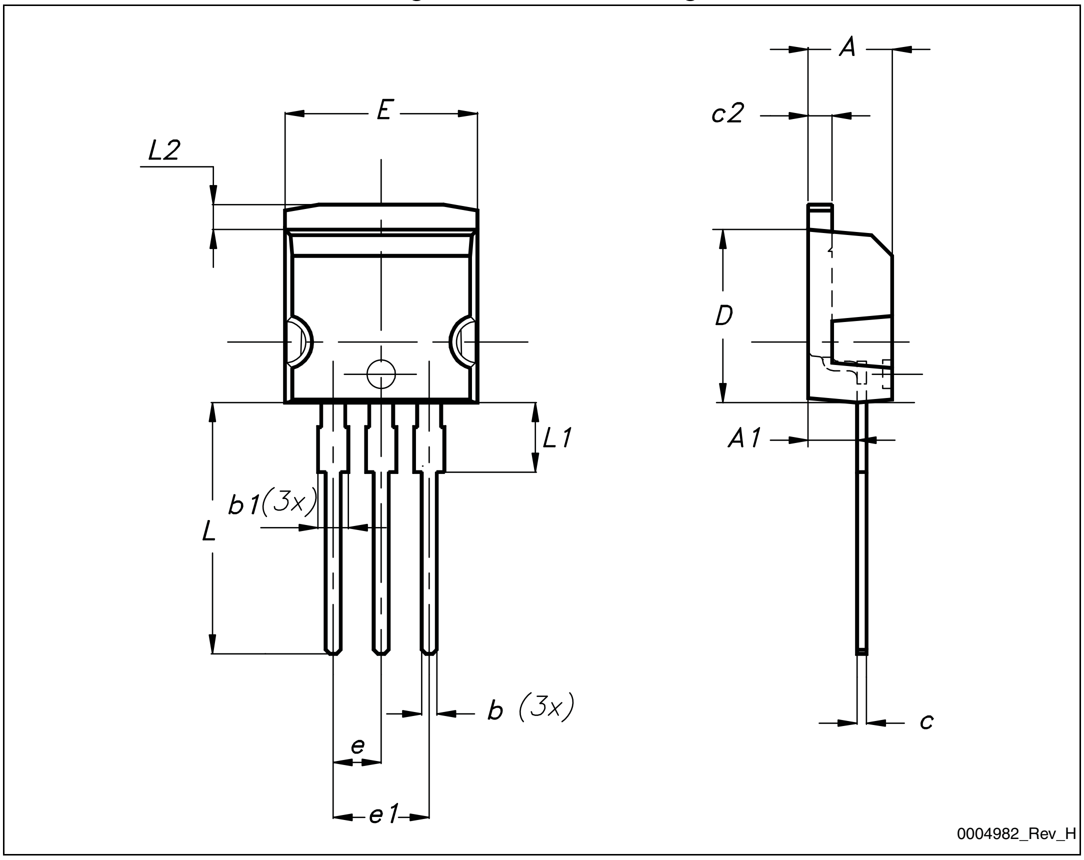


Table 11. I²PAK mechanical data

DIM.	mm.		
	min.	typ.	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

4.4 TO-220, STP6N80K5

Figure 27. TO-220 type A drawing

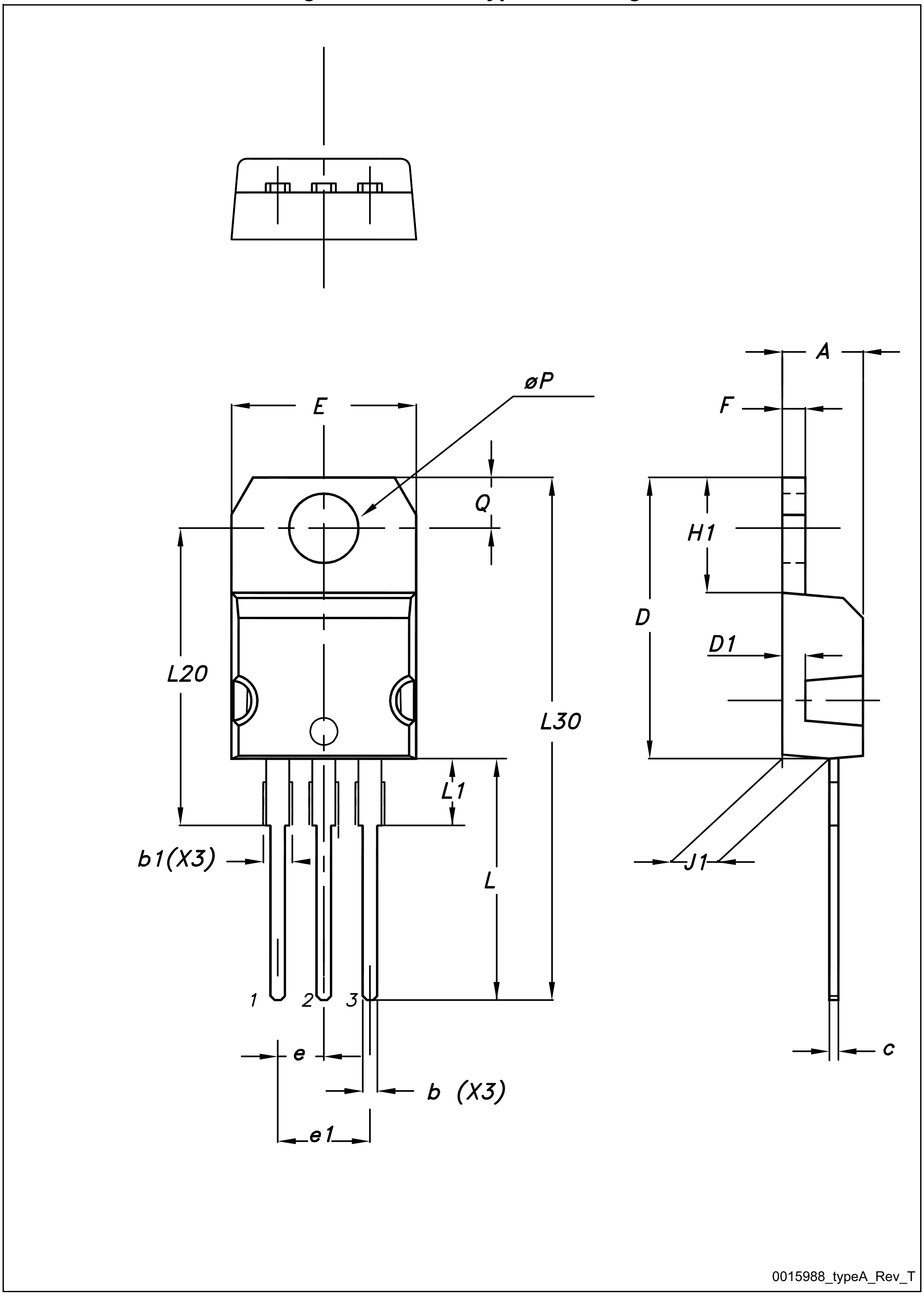


Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

5 Packaging information

5.1 D²PAK and DPAK tape and reel mechanical data

Figure 28. Tape for D²PAK and DPAK

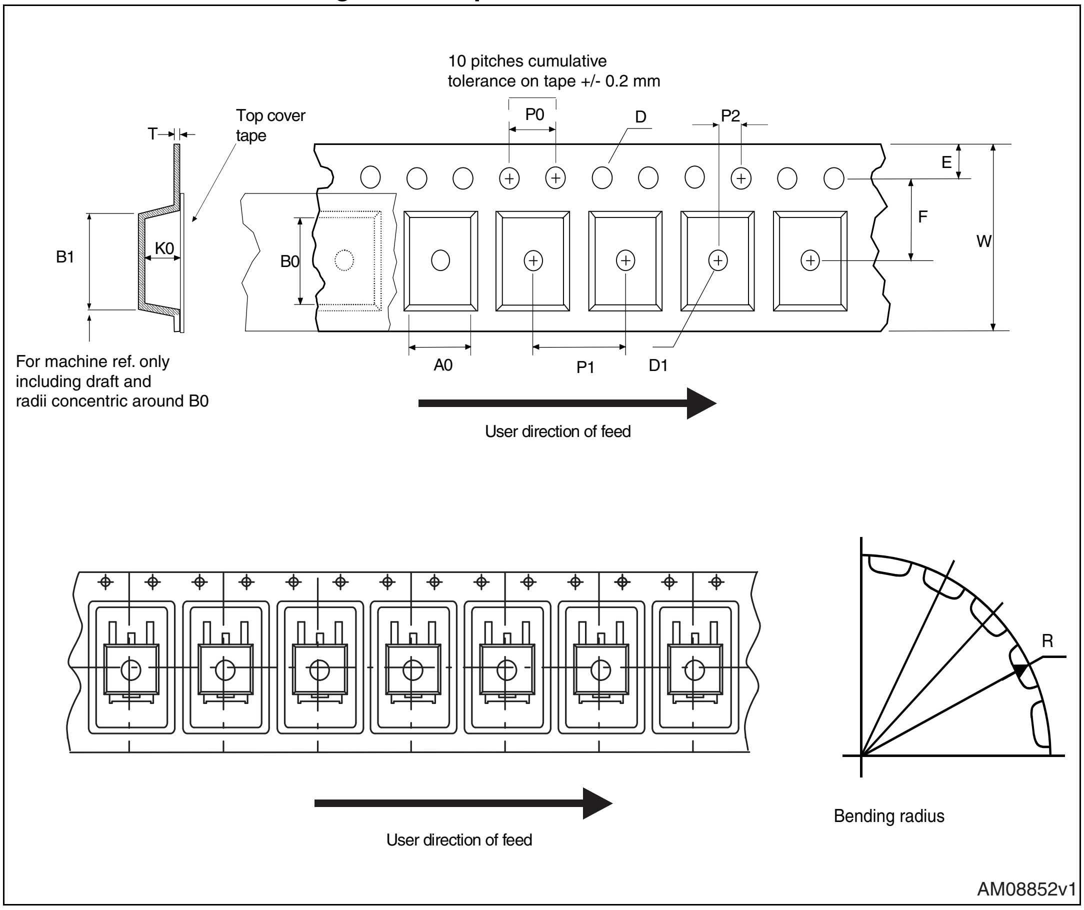


Figure 29. Reel for D²PAK and DPAK

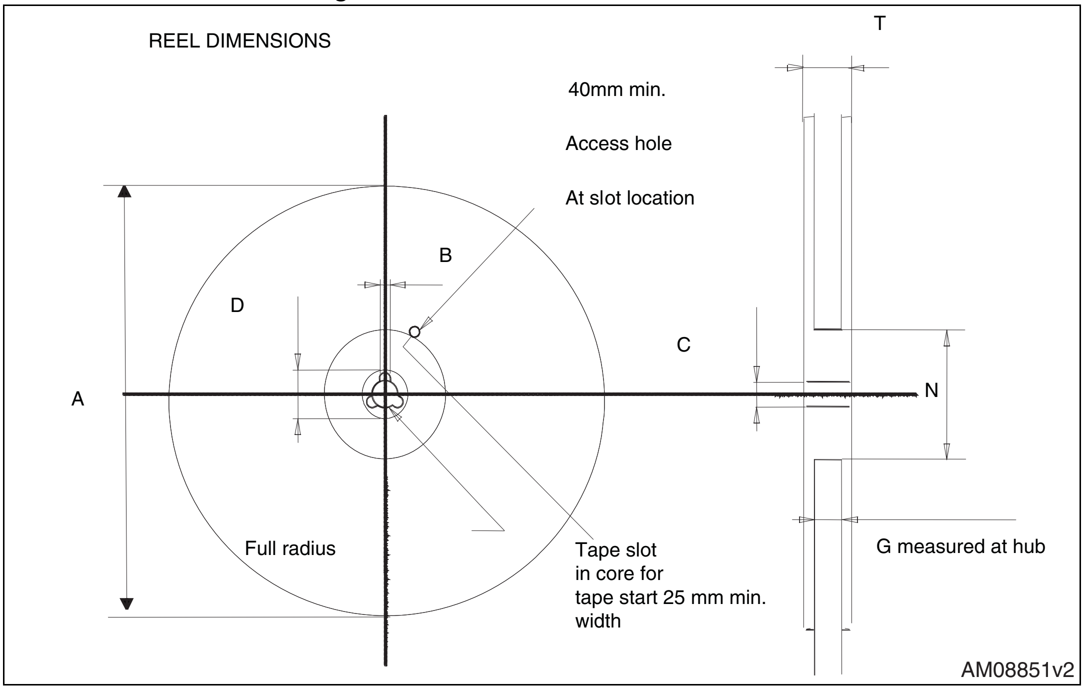


Table 13. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 14. DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 15. Document revision history

Date	Revision	Changes
28-May-2013	1	First release.
05-Dec-2014	2	Updated title, features and description in cover page. Added *Section 2.1: Electrical characteristics (curves)*. Updated *Section 4: Package mechanical data*. Minor text changes.