FS6012-02

I²C™ Digital Video/Audio Clock Generator IC

August 1998

1.0 Features

- Triple phase-locked loop (PLL) device provides exact ratiometric derivation of Audio, Processor, and Utility Clocks
- I²C™-bus interface for Audio and Utility Clock frequency selection
- I²C™-bus/board programmable Processor Clock frequency selection
- On-chip tunable voltage-controlled crystal oscillator (VCXO) allows precise system frequency tuning
- Tunable Audio Clock frequencies for undetectable resynchronization of audio and video streams
- Custom frequency selections available - contact your local AMI Sales Representative for more information

2.0 Description

The FS6012-02 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

At the core of the FS6012-02 is circuitry that implements a voltage controllable crystal oscillator when an external resonator is attached. The circuitry allows device frequencies to be precisely adjusted for use in systems that have frequency matching requirements, such as digital satellite receivers.

Three high-resolution phase-locked loops independently generate three other selectable frequencies derived from the VCXO frequency. These clock frequencies are related to the VCXO frequency and to each other by exact ratios. The locking of all the output frequencies together can eliminate unpredictable artifacts in video systems and reduces electromagnetic interference (EMI) due to frequency harmonic stacking.

Figure 1: Block Diagram

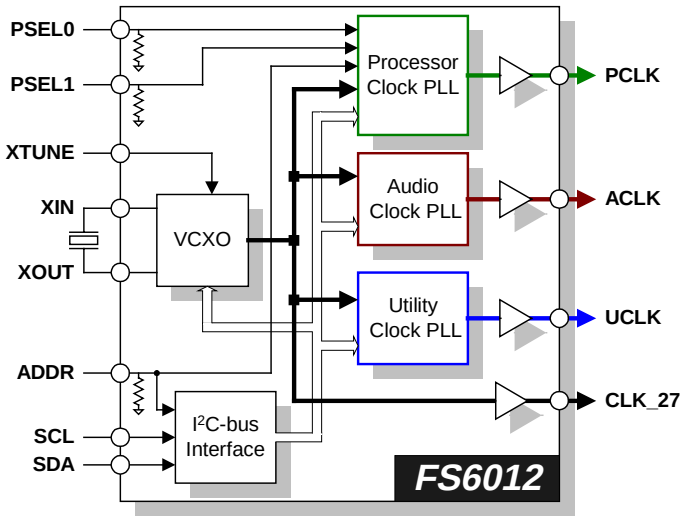
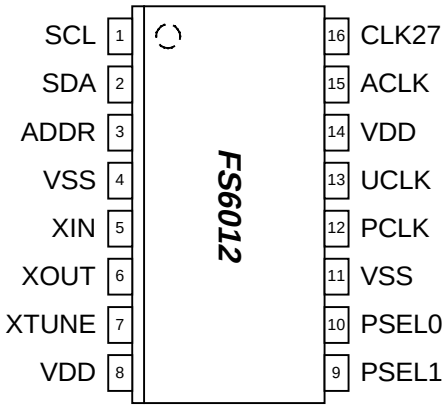


Figure 2: Pin Configuration



16-pin (0.150") SOIC

ISO9001

Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	DI	SCL	Serial Data Clock
2	DIO	SDA	Serial Data Input/Output
3	DI_D	ADDR	Address Select Bit
4	P	VSS	Ground
5	AI	XIN	VCXO Feedback
6	AO	XOUT	VCXO Drive
7	AI	XTUNE	VCXO Tune
8	P	VDD	Power Supply (+5V)
9	DI_D	PSEL1	PCLK Select MSB
10	DI_D	PSEL0	PCLK Select LSB
11	P	VSS	Ground
12	DO	PCLK	Processor Clock Output
13	DO	UCLK	Utility Clock Output
14	P	VDD	Power Supply (+5V)
15	DO	ACLK	Audio Clock Output
16	DO	CLK27	Reference Clock Output

3.0 Functional Block Description

3.1 Phase-Locked Loops

Each one of the three on-chip PLLs in the FS6012 is a standard frequency- and phase-locked loop architecture. Each PLL multiplies the reference oscillator to the desired frequency by a ratio of integers. The frequency multiplication is exact.

An onboard ROM contains the PLL settings that control the relationship between reference and output frequencies. The I^2C-bus communications are used to choose a desired ROM setting. Custom frequency selections are available for this device. Contact your local AMI Sales Representative for more information

3.2 Output Tristate Control

All four clock outputs of the FS6012 may be tristated to facilitate circuit board testing. To place the outputs in tristate mode, follow this sequence:

1. force XIN low (i.e. ground)
2. apply power to the device
3. wait until the internal power-on reset has de-asserted
4. apply a negative-going transition to the PSEL0 pin

Outputs may be re-enabled by removing and reapplying VDD to the device. To re-enable outputs without removing power, apply a positive-going transition to the XIN in and follow it with a negative-going transition on the PSEL0 pin.

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3.3 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6012 system components. Loading capacitance for the crystal is internal to the FS6012. No external components (other than the resonator itself) are required for operation of the VCXO.

The resonator loading capacitance is adjustable under register control. This permits factory coarse tuning of inexpensive resonators to the necessary precision for digital video applications.

Continuous fine-tuning of the VCXO frequency is accomplished by varying the voltage on the XTUNE pin. The total change (from one extreme to the other) in effective loading capacitance is 1.5pF nominal.

The oscillator operates the crystal resonator in the parallel-resonant mode. Crystal warping, or the "pulling" of the crystal oscillation frequency, is accomplished by altering the effective load capacitance presented to the crystal by the oscillator circuit. The actual amount that changing the load capacitance alters the oscillator frequency will be dependent on the characteristics of the crystal as well as the oscillator circuit itself.

Specifically, the motional capacitance of the crystal (usually referred to by crystal manufacturers as C_1), the static capacitance of the crystal (C_0), and the load capacitance (C_L) of the oscillator determine the warping capability of the crystal in the oscillator circuit.

A simple formula to obtain the warping capability of a crystal oscillator is:

$$\Delta f\,(ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where C_{L1} and C_{L2} are the two extremes of the applied load capacitance. A crystal with the following parameters is used. With C_1 = 0.02pF, C_0 = 5pF, C_{L1} = 10pF, C_{L2} = 22.66pF, the coarse tuning range is:

$$\Delta f = \frac{0.02 \times (22.66 - 10) \times 10^6}{2 \times (5 + 22.66) \times (5 + 10)} = 305\,ppm$$

4.0 Programming Information

Table 2: Register Summary

BIT D[x]	REGISTER BIT DESCRIPTION	
0	ACLK Select (LSB)	
1	ACLK Select	
2	ACLK Select	
3	ACLK Select (MSB)	
4	UCLK Select (LSB)	
5	UCLK Select	
6	UCLK Select	
7	UCLK Select (MSB)	
8	PCLK Select (LSB)	
9	PCLK Select	
10	PCLK Select (MSB)	
11	Crystal Oscillator Coarse Tune (LSB)	
12	Crystal Oscillator Coarse Tune	
13	Crystal Oscillator Coarse Tune	
14	Crystal Oscillator Coarse Tune (MSB)	
15	VCXO Fine Tune Enable/Disable	
	Bit = 0	Disable Fine Tune
	Bit = 1	Enable Fine tune

4.1 Audio PLL Clock Frequencies (ACLK)

The ACLK frequency is controlled by register bits D[0], D[1], D[2], and D[3], accessed via the serial interface. ACLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz.

Table 3: ACLK Frequency Select via I²C-bus

D[3]	D[2]	D[1]	D[0]	PLL DIVIDER RATIO	ACLK (MHz)
0	0	0	0	32 / 27	32.0000
0	0	0	1	784 / 1875	11.2896
0	0	1	0	512 / 1875	7.3728
0	0	1	1	128 / 1875	1.8432
0	1	0	0	8 / 9	24.0000
0	1	0	1	1	27.0000
0	1	1	0	823 / 1968	11.2912
0	1	1	1	461 / 1688	7.3738
1	0	0	0	99 / 1450	1.8434
1	0	0	1	809 / 910	24.0033
1010 to 1111				Duplicate of 0010 to 0111 selections	

NOTE: Contact AMI for custom PLL frequencies

4.2 Utility PLL Clock Frequencies (UCLK)

The UCLK frequency is controlled by register bits D[4], D[5], D[6] and D[7], accessed via the serial interface. UCLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz.

Table 4: UCLK Frequency Select via I²C-bus

D[7]	D[6]	D[5]	D[4]	PLL DIVIDER RATIO	UCLK (MHz)
0	0	0	0	32 / 27	32.0000
0	0	0	1	34 / 143	6.4196
0	0	1	0	68 / 143	12.8392
0	0	1	1	488 / 2025	6.5067
0	1	0	0	976 / 2025	13.0133
0	1	0	1	13 / 54	6.5000
0	1	1	0	13 / 27	13.0000
0	1	1	1	10 / 11	24.5454
1	0	0	0	1	27.0000
1	0	0	1	10 / 33	8.1818
1010 to 1111				Duplicate of 0010 to 0111 selections	

NOTE: Contact AMI for custom PLL frequencies

4.3 Processor PLL Frequencies (PCLK)

The PCLK frequency is controlled by either the logic levels on the PSEL inputs or through bits D[10:8]. PCLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz. These inputs have weak pull-downs.

Table 5: PCLK Frequency Select via Pins

ADDR	PSEL1	PSEL0	PLL DIVIDER RATIO	PCLK (MHz)
0	0	0	35 / 66	14.31818
0	0	1	423 / 644	17.73447
0	1	0	35 / 264	3.579545
0	1	1	See Table 6	
1	0	0	427 / 2600	4.43423
1	0	1	423 / 2576	4.433618
1	1	0	1135 / 6912	4.4335937
1	1	1	See Table 6	

NOTE: Contact AMI for custom PLL frequencies

For the special case where both PSEL inputs are high, the PCLK frequency is controlled by data bits D[10:8]. PCLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz.

Table 6: PCLK Frequency Select via I²C-bus

D[10]	D[9]	D[8]	PLL DIVIDER RATIO	PCLK (MHz)
0	0	0	35 / 66	14.3182
0	0	1	423 / 644	17.7345
0	1	0	35 / 264	3.5795
0	1	1	728 / 375	52.4160
1	0	0	427 / 2600	4.4342
1	0	1	423 / 2576	4.43361
1	1	0	1135 / 6912	4.43359
1	1	1	18 / 25	19.4400

NOTE: Contact AMI for custom PLL frequencies

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4.4 VCXO Coarse Tuning and Enable

The VCXO may be coarse tuned by a programmable adjustment of the crystal load capacitance via D[14:11]. The actual amount of frequency warping caused by the tuning capacitance will depend on the crystal used. The VCXO tuning capacitance includes an external load capacitance of 6pF (12pF from the XIN pin to ground and 12pF from the XOUT pin to ground).

The fine tuning capability of the VCXO can be enabled by setting D[15] to a logic-one or disabled by clearing the bit to a logic-zero.

Table 7: VCXO Coarse Tuning via I²C-bus

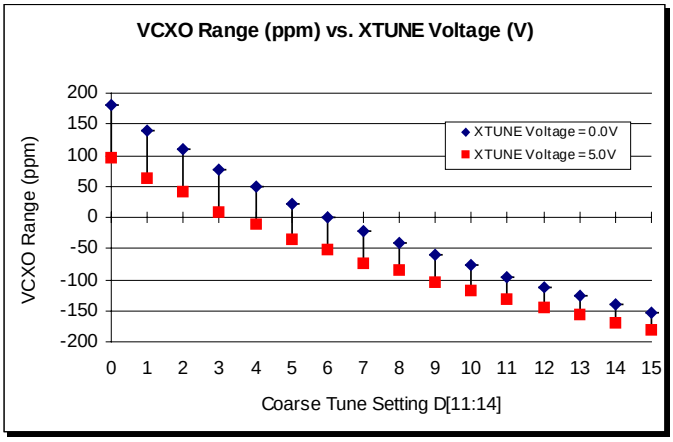
D[14]	D[13]	D[12]	D[11]	VCXO TUNING CAPACITANCE (pF)
0	0	0	0	10.00
0	0	0	1	10.84
0	0	1	0	11.69
0	0	1	1	12.53
0	1	0	0	13.38
0	1	0	1	14.22
0	1	1	0	15.06
0	1	1	1	15.91
1	0	0	0	16.75
1	0	0	1	17.59
1	0	1	0	18.43
1	0	1	1	19.28
1	1	0	0	20.13
1	1	0	1	20.97
1	1	1	0	21.81
1	1	1	1	22.66

4.5 VCXO Range

Figure 3 shows the typical effect of the coarse and fine tuning mechanisms. The difference in VCXO frequency in parts-per-million (ppm) is shown as the fine tuning voltage on the XTUNE pin varies from 0V to 5V. The coarse tune range as shown is about 350ppm. As the crystal load capacitance is increased (with increasing Coarse Tune setting) the frequency is pulled somewhat less with each coarse step and the fine tuning range decreases.

The fine tuning range always overlaps a few coarse tuning ranges, eliminating the possibility of holes in the VCXO response. Note that different crystal warping characteristics will change the scaling on the Y-axis, but not the overall characteristic of the curves.

Figure 3: VCXO Range



5.0 I²C-bus Control Interface

This device is a read/write slave device meeting all Philips I²C-bus specifications except a "general call". The bus has to be controlled by a master device that generates the serial clock SCL, controls bus access, and generates the START and STOP conditions while the device works as a slave. Both master and slave can operate as a transmitter or receiver, but the master device determines which mode is activated. A device that sends data onto the bus is defined as the transmitter, and a device receiving data as the receiver.

I²C-bus logic levels noted herein are based on a percentage of the power supply (VDD). A logic-one corresponds to a nominal voltage of VDD, while a logic-zero corresponds to ground (VSS).

5.1 Bus Conditions

Data transfer on the bus can only be initiated when the bus is not busy. During the data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high. Changes in the data line while the clock line is high will be interpreted by the device as a START or STOP condition. The following bus conditions are defined by the I²C-bus protocol.

5.1.1 Not Busy

Both the data (SDA) and clock (SCL) lines remain high to indicate the bus is not busy.

5.1.2 START Data Transfer

A high to low transition of the SDA line while the SCL input is high indicates a START condition. All commands to the device must be preceded by a START condition.

5.1.3 STOP Data Transfer

A low to high transition of the SDA line while SCL is held high indicates a STOP condition. All commands to the device must be followed by a STOP condition.

5.1.4 Data Valid

The state of the SDA line represents valid data if the SDA line is stable for the duration of the high period of the SCL line after a START condition occurs. The data on the SDA line must be changed only during the low period of the SCL signal. There is one clock pulse per data bit.

Each data transfer is initiated by a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is determined by the master device, and can continue indefinitely. However, data that is overwritten to the device after the first eight bytes will overflow into the first register, then the second, and so on, in a first-in, first-overwritten fashion.

5.1.5 Acknowledge

When addressed, the receiving device is required to generate an Acknowledge after each byte is received. The master device must generate an extra clock pulse to coincide with the Acknowledge bit. The acknowledging device must pull the SDA line low during the high period of the master acknowledge clock pulse. Setup and hold times must be taken into account.

The master must signal an end of data to the slave by not generating and acknowledge bit on the last byte that has been read (clocked) out of the slave. In this case, the slave must leave the SDA line high to enable the master to generate a STOP condition.

5.2 I²C-bus Operation

All programmable registers can be accessed randomly or sequentially via this bi-directional two wire digital interface. The device accepts the following I²C commands.

5.2.1 Slave Address

After generating a START condition, the bus master broadcasts a seven-bit slave address followed by a R/W bit. The address of the device is:

A6	A5	A4	A3	A2	A1	A0
1	0	1	1	X	0	0

where X is controlled by the logic level at the ADDR pin. The variable ADDR bit allows two different devices to exist on the same bus. Note that every device on an I²C-bus must have a unique address to avoid bus conflicts.

5.2.2 Random Register Write Procedure

Random write operations allow the master to directly write to any register. To initiate a write procedure, the R/W bit that is transmitted after the seven-bit device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write eight bits of data into the addressed regis-

ter. A final acknowledge is returned by the device, and the master generates a STOP condition.

If either a STOP or a repeated START condition occurs during a Register Write, the data that has been transferred is ignored.

5.2.3 Random Register Read Procedure

Random read operations allow the master to directly read from any register. To perform a read procedure, the R/W bit that is transmitted after the seven-bit address is a logic-low, as in the Register Write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits the eight-bit word. The master does not acknowledge the transfer but does generate a STOP condition.

5.2.4 Sequential Register Write Procedure

Sequential write operations allow the master to write to each register in order. The register pointer is automatically incremented after each write. This procedure is more efficient than the Random Register Write if several registers must be written.

To initiate a write procedure, the R/W bit that is transmitted after the seven-bit device address is a logic-low. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is written into the slave's address pointer. Following an acknowledge by the slave, the master is allowed to write up to eight bytes of data into the addressed register before the register address pointer overflows back to the beginning address. An acknowledge by the device between each byte of data must occur before the next data byte is sent.

5.2.5 Sequential Register Read Procedure

Sequential read operations allow the master to read from each register in order. The register pointer is automatically incremented by one after each read. This procedure is more efficient than the Random Register Read if several registers must be read from.

To perform a read procedure, the R/W bit that is transmitted after the seven-bit address is a logic-low, as in the Register Write procedure. This indicates to the addressed slave device that a register address will follow after the slave device acknowledges its device address. The register address is then written into the slave's address pointer.

Following an acknowledge by the slave, the master generates a repeated START condition. The repeated START terminates the write procedure, but not until after the slave's address pointer is set. The slave address is then resent, with the R/W bit set this time to a logic-high, indicating to the slave that data will be read. The slave will acknowledge the device address, and then transmits all eight bytes of data starting with the initial addressed register. The register address pointer will overflow if the initial register address is larger than zero. After the last byte of data, the master does not acknowledge the transfer but does generate a STOP condition.

Figure 4: Random Register Write Procedure

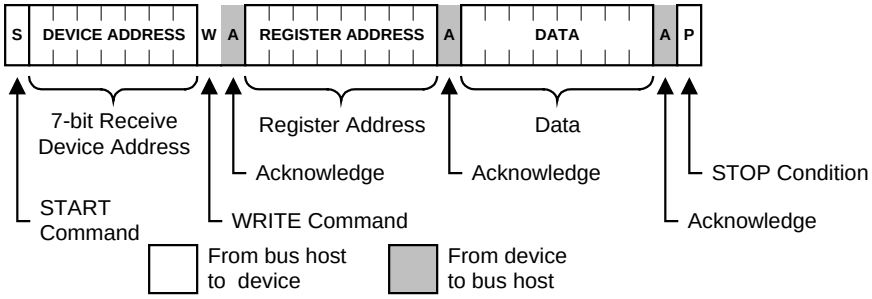


Figure 5: Random Register Read Procedure

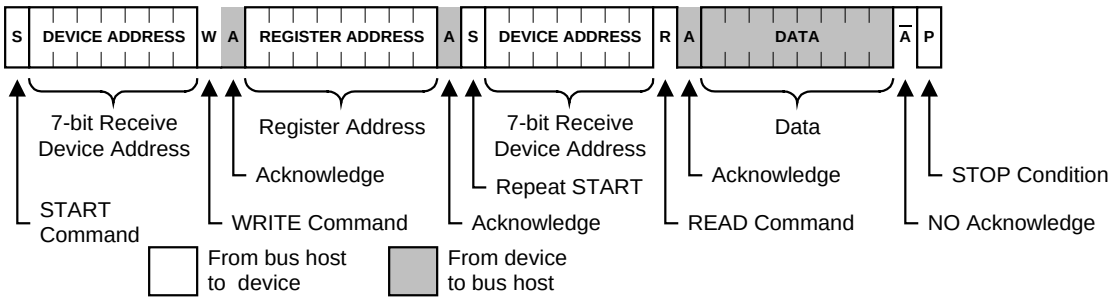


Figure 6: Sequential Register Write Procedure

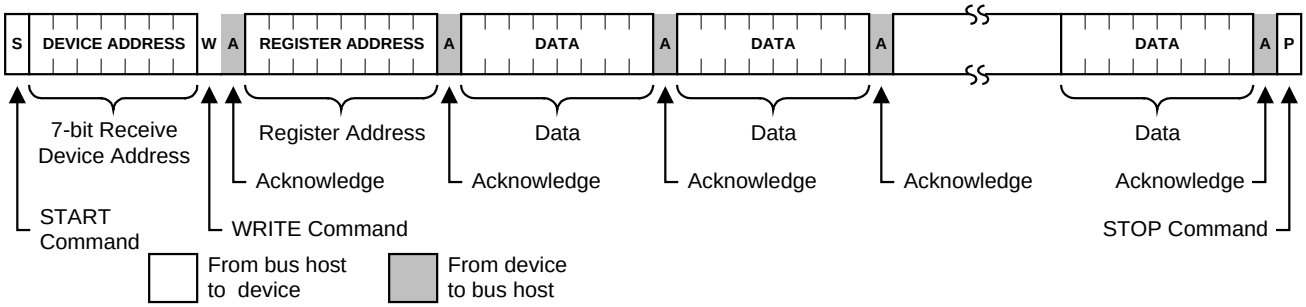
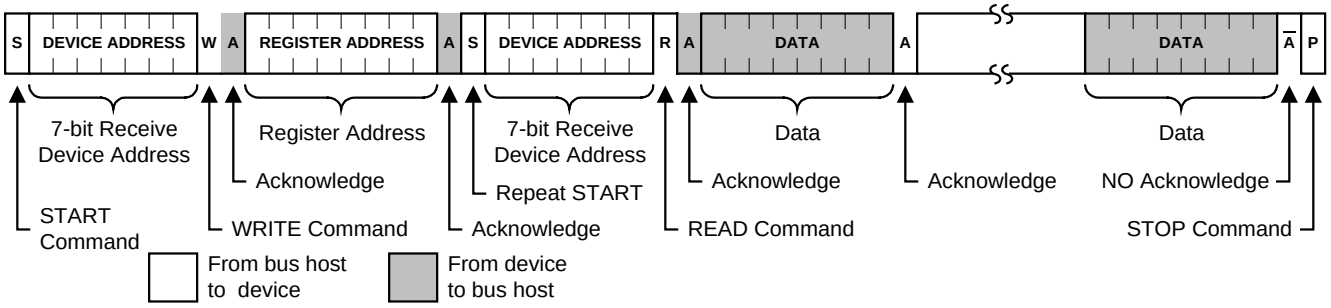


Figure 7: Sequential Register Read Procedure



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6.0 Electrical Specifications

Table 8: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 9: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	5V ± 10%	4.5	5	5.5	V
Ambient Operating Temperature Range	T_A		0		70	°C
Resonator or Crystal Frequency	f_{XIN}		24	27	28	MHz
Resonator Motional Capacitance	C_{MOT}	AT cut		25		fF
Output Load Capacitance	C_L				15	pF
I^2C Data Transfer Rate		Standard Mode		100	400	kHz

Table 10: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{CLK} = 27MHz; $C_L \approx$ 15pF		58	80	mA
Supply Current, Static	I_{DDL}	f_{XIN} = 0		25		mA
VCXO Range		Assumes 6pF load capacitance (12pF from both XIN and XOUT to ground)		350		ppm
Serial Communication I/O (SDA, SCL)						
High-Level Input Voltage	V_{IH}		$0.7V_{DD}$		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		$0.3V_{DD}$	V
Hysteresis Voltage	V_{hys}			$0.4V_{DD}$		V
Input Leakage Current	I_I		-1		1	µA
Low-Level Output Sink Current (SDA)	I_{OL}	V_{OL} = 0.4V, V_{DD} = 4.5V	10	25		mA
Control Inputs (ADDR, PSEL0, PSEL1)						
High-Level Input Voltage	V_{IH}		2.4		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current (pull-down)	I_{IH}	$V_{IH} = V_{DD}$ = 5.5V	5	12.7	50	µA
Low-Level Input Current	I_{IL}		-1		1	µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage *	V_{TH}			$0.5V_{DD}$		V
Input Leakage Current	I_I		-1		1	µA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT; VCXO tuning disabled		10		pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XIN; XOUT unconnected; VCXO disabled		20		pF
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current *	I_{OH}	V_O = 0V; D[15] = 0		-45		µA
		V_O = 0V, V(XTUNE) = 5V; D[15] = 1		-52		
Low-Level Output Sink Current *	I_{OL}	V_O = 5V; D[15] = 0		53		µA
		V_O = 5V, V(XTUNE) = 5V; D[15] = 1		63		
VCXO Tuning Input (XTUNE)						
Input Leakage Current	I_I		-1		1	µA
Clock Outputs (ACLK, CLK27, PCLK, UCLK)						
High-Level Output Source Current	I_{OH}	V_O = 2.4V		-46		mA
Low-Level Output Sink Current	I_{OL}	V_O = 0.4V		64		mA
Output Impedance	z_{OH}	$V_O = 0.5V_{DD}$; output driving high		53		Ω
	z_{OL}	$V_O = 0.5V_{DD}$; output driving low		57		
Tristate Output Current	I_{OZ}		-10		+10	µA
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-60		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 5V; shorted for 30s, max.		65		mA

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Table 11: AC Timing Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (PCLK)							
Duty Cycle *		From rising edge to rising edge at 2.5V	14.318	48		52	%
			17.734	48		52	
			3.579	48		52	
			52.416	40		44	
			4.4342	48		52	
			4.4336	48		52	
			4.4335	48		52	
			19.440	48		52	
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	14.318		800		ps
			17.734		1410		
			3.579		870		
			52.416		980		
			4.4342		1070		
			4.4336		1300		
			4.4335		1630		
			19.440		1430		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	14.318		510		ps
			17.734		500		
			3.579		520		
			52.416		620		
			4.4342		680		
			4.4336		750		
			4.4335		740		
			19.440		580		
Clock Stabilization *	t_{STB}	Output active from power-up			960		µs
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.5		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			1.8		ns
Clock Output (CLK27)							
Duty Cycle *		Crystal oscillator frequency out, from rising edge to rising edge at 2.5V	27	45		48	%
Clock Stabilization Time *	t_{STB}	Output active from power-up			300		µs
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.5		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.2		ns

Table 12: AC Timing Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (ACLK)							
Duty Cycle *		From rising edge to rising edge at 2.5V	32.0000	44		48	%
			11.2896	48		52	
			7.3728	48		52	
			1.8432	48		52	
			24.0000	44		48	
			27.0000	44		48	
			11.2912	48		52	
			7.3738	48		52	
			1.8434	48		52	
			24.0033	44		48	
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	32.0000		1700		ps
			11.2896		510		
			7.3728		600		
			1.8432		2360		
			24.0000		330		
			27.0000		230		
			11.2912		520		
			7.3738		940		
			1.8434		890		
			24.0033		920		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	32.0000		440		ps
			11.2896		670		
			7.3728		600		
			1.8432		750		
			24.0000		510		
			27.0000		1660		
			11.2912		680		
			7.3738		560		
			1.8434		710		
			24.0033		600		
Clock Stabilization Time *	t_{STB}	Output active from power-up			770		µs
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.5		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			1.8		ns

Table 13: AC Timing Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (UCLK)							
Duty Cycle *		From rising edge to rising edge at 2.5V	32.0000	44		48	%
			6.4196	48		52	
			12.8392	48		52	
			6.5067	48		52	
			13.0133	48		52	
			6.5000	48		52	
			13.0000	48		52	
			24.5454	45		49	
			27.0000	44		48	
			8.1818	48		52	
Jitter, Long Term ($\sigma_y^2(\tau)$) *	$t_{j(LT)}$	From rising edge to 1st rising edge after 500µs at 2.5V, C_L = 15pF, all PLLs active	32.0000		1380		ps
			6.4196		850		
			12.8392		810		
			6.5067		880		
			13.0133		870		
			6.5000		660		
			13.0000		930		
			24.5454		770		
			27.0000		380		
			8.1818		720		
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C_L = 15pF, all PLLs active	32.0000		470		ps
			6.4196		470		
			12.8392		510		
			6.5067		620		
			13.0133		620		
			6.5000		650		
			13.0000		550		
			24.5454		550		
			27.0000		1940		
			8.1818		610		
Clock Stabilization Time *	t_{STB}	Output active from power-up			600		µs
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.6		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.0		ns

Table 14: Serial Interface Timing Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	STANDARD MODE		UNITS
			MIN.	MAX.	
Clock frequency	f_{SCL}	SCL	0	100	kHz
Bus free time between STOP and START	t_{BUF}		4.7		µs
Set up time, START (repeated)	$t_{su:STA}$		4.7		µs
Hold time, START	$t_{hd:STA}$		4.0		µs
Set up time, data input	$t_{su:DAT}$	SDA	250		ns
Hold time, data input	$t_{hd:DAT}$	SDA	0		µs
Output data valid from clock	t_{AA}	Minimum delay to bridge undefined region of the fall-ing edge of SCL to avoid unintended START or STOP		3.5	µs
Rise time, data and clock	t_R	SDA, SCL		1000	ns
Fall time, data and clock	t_F	SDA, SCL		300	ns
High time, clock	t_{HI}	SCL	4.0		µs
Low time, clock	t_{LO}	SCL	4.7		µs
Set up time, STOP	$t_{su:STO}$		4.0		µs

Figure 8: Bus Timing Data

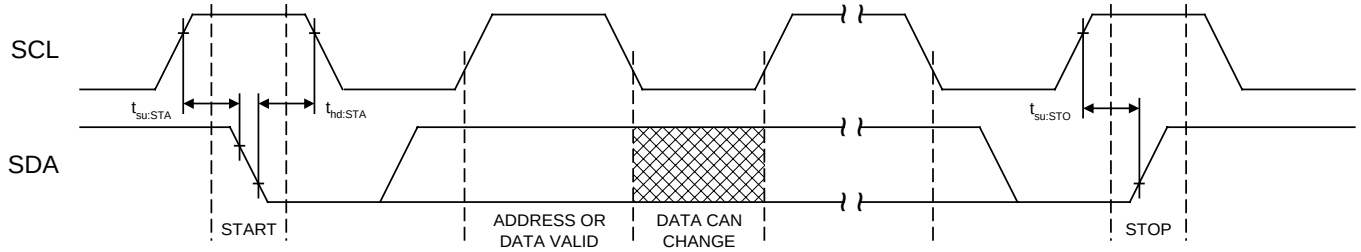
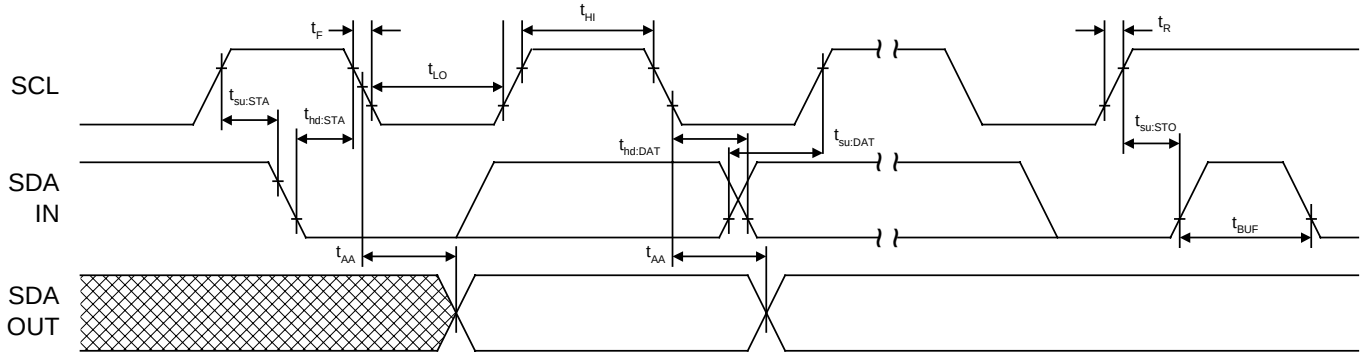


Figure 9: Data Transfer Sequence



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7.0 Package Information

Table 15: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

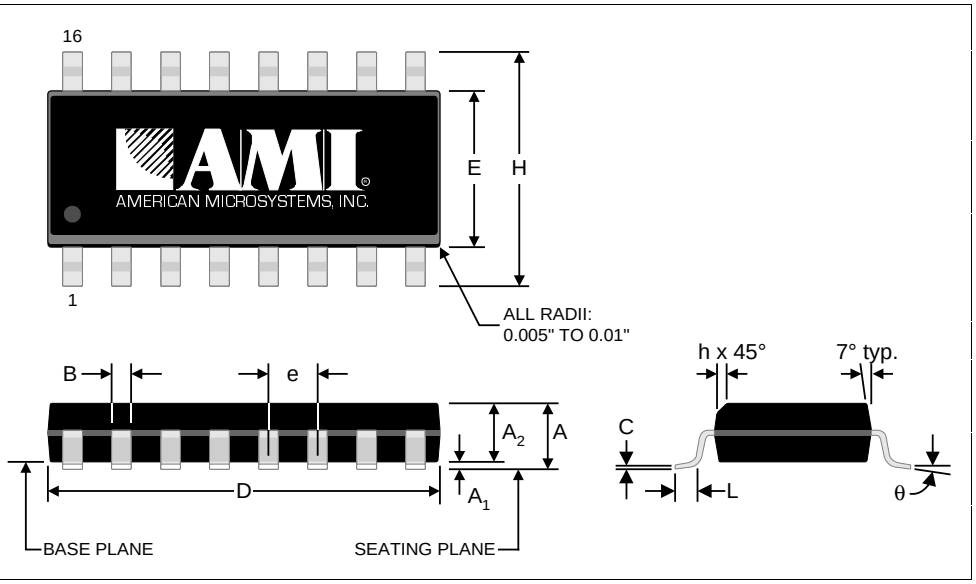

Table 16: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{jA}	Air flow = 0 m/s	108	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

8.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	FONT	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11212-002	FS6012	-02	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes

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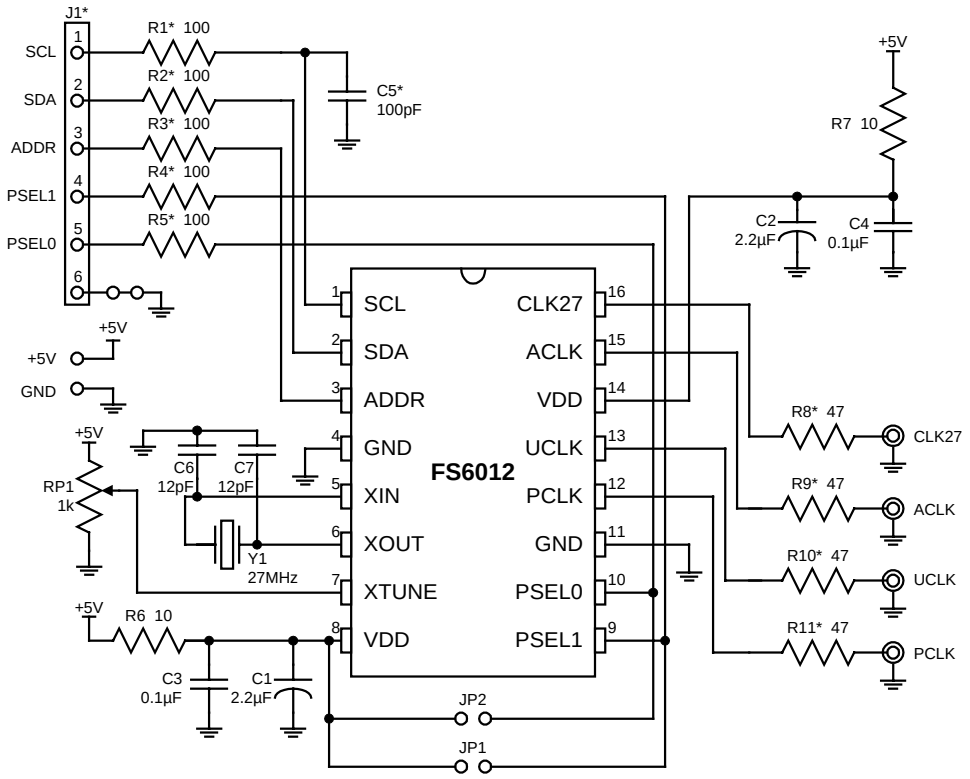
9.0 Demonstration Board Schematic

A simple demonstration board and DOS-based software is available from American Microsystems that illustrates the capabilities of the FS6012-02. The board schematic is shown below. Components listed with an asterisk (*) are not required in an actual application, and are used here to preserve signal integrity with the cabling associated with the board. A cabled interface between a computer parallel port (DB25 connector) and the board (J1) is provided.

Contact your local sales representative or the company directly for more information.



9.1 Contents

- Demonstration board
- Interface cable (DB25 to 6-pin connector)
- Data sheet
- Self-uncompressing exe file containing demonstration software, including:
  - INSTALL.BAT 0.73kB
  - FS6012.BAT 0.24kB
  - FS6012T.BAS 12.96kB

9.2 Requirements

- PC running MS-DOS or MS Windows® 3.1x, with accessible parallel (LPT1) port
- MS-QBasic v. 1.1 or later (or equivalent software)
- 13.9kB available free space on drive C:

9.3 Board Setup and Software Installation Instructions

1. At the appropriate disk drive prompt (A:\) type **Install** to automatically copy demo files to the C: drive. NOTE: This demo software requires Microsoft QBasic or equivalent to run. Make sure the directory containing qbasic.exe is in the DOS path statement, or move the demo files to a directory containing Basic.
2. Connect a +5 Volt power supply to the board: RED = +5V, BLACK = ground.
3. Remove all software keys from the computer parallel port.
4. Connect the supplied interface cable to the parallel port (DB25 connector) and to the demo board (6-pin connector). Make sure the cable is facing away from the board – pin 1 is the red wire.
5. Connect the clock outputs to the target application board with a twisted-pair cable.

9.4 Demo Program

1. Type **FS6012** at the C:\FS6012 prompt to run the Qbasic-based demo program.
2. The following heading banner should appear:

Figure 10: Banner

```
*********************************************
*                                           *
*           FS6012 Utility Program          *
*                                           *
*        PRESS ANY KEY TO CONTINUE.....     *
*                                           *
*********************************************
```

3. After pressing any key, a menu should appear containing a list of the program hot keys, a message that the computer parallel (LPT1) port was found, and the address at which the port was found.

Figure 11: Menu

```
**********************
* FS6012 Utility     *
*                    *
* (R)ead             *
* (W)rite            *
* (V)CXO coarse set  *
* (A)CLK set         *
* (U)CLK set         *
* (P)CLK set         *
* (E)nable VCXO      *
* (S)et PSEL strap   *
* addrse(L) strap set *
* e(X)it             *
**** POWER IS ON  *****
```

Refer to Table 17 for a description of each hot key.

4. To change the frequency of the desired clock, press the appropriate hot key. The keys are *not* case sensitive. Refer to Table 3 for ACLK frequencies, Table 4 for UCLK frequencies, Table 6 for PCLK frequencies. Refer to Table 7 for the VCXO coarse tune bits.
5. Data is sent to the device in a two-byte sequence, referred to as address 0 and address 1. The address 0 byte contains bits 0 to 7 (see Table 2) and the address 1 byte contains bits 8-15. During a read/write operation, data is displayed in the following format:

```
READ of address {0 or 1} is {data in decimal(data in hex)}
Writing {data in decimal(data in hex)} to address {0 or 1}
```

Table 17: Hot Key Description

COMMAND	KEY	BITS	ADDRESS	RANGE	DESCRIPTION
Read	R	0-7	0	-	Manual Read with selectable address
		8-15	1		
Write	W	0-7	0	All 15 bits	Manual Write with selectable address and user-defined data
		8-15	1		
ACLK	A	0-3	0	0000-1111	Cycles through ACLK frequencies (Table 3)
UCLK	U	4-7	0	0000-1111	Cycles through UCLK frequencies (Table 4)
PCLK	P	8-10	1	000-111	Cycles through PCLK frequencies (Table 6)
VCXO Course Set	V	11-14	1	0000-1111	Digital coarse tune of the VCXO
VCXO Enable	E	15	1	0-1	Enables fine tune of the VCXO via the XTUNE pin
Set PSEL Strap	S	-	-	00-11	Cycles through PCLK frequencies via PSEL0 and PSEL1 pins (Table 5)
Address Select Strap	L	-	-	0-1	Alters ADDR bit in the I²C address
Exit	X	-	-	-	Exits the demo program

6. Observe the response to the hot key selection. Repeated pressing of the same key will scroll through the entire range of settings for the selected command, returning to the initial setting.
7. The Read and Write commands permit the user to read data from a desired register or to manually overwrite data into a desired register.
8. Pressing a hot key strobes a 15-bit message to the demo board via the interface cable. An example of the response to the key selection is shown below:

```
Reading...
READ of address 0 is 22(0x16)
Read DONE...
Writing 17(0x11) to address 0
Write DONE...
```

9. The Set PSEL Strap and ADDRsel Strap Set commands drive pins 3, 4 and 5 (ADDR, PSEL0, and PSEL1) directly. No read/write activity will be observed on the screen.
10. The FS6012 uses I²C-bus communication. The interface cable must be correctly attached to the demo board prior to performing any functions or an error message will be displayed.

Figure 12: Error Messages

```
************************************************
*                                              *
* WARNING !! - I2C BYTE SEND ACK failed !!!    *
*                                              *
*       (press any key to continue)            *
*                                              *
************************************************
```

During a Write procedure (from the computer to the device), an Acknowledge bit should be returned by the device. The above error occurs if the computer fails to receive an Acknowledge from the device.

```
************************************************
*                                              *
* WARNING !! - I2C CONTROL ACK failed !!!      *
*                                              *
*       (press any key to continue)            *
*                                              *
************************************************
```

The state of the I²C-bus is checked by the software during a Sequential Register Read to the device. The above message is displayed if the I²C-bus has a one-conflict when the Acknowledge was supposed to occur.

```
************************************************
*                                              *
* WARNING !! - I2C write of 1 failed !!!       *
*                                              *
*       (press any key to continue)            *
*                                              *
************************************************
```

The state of the I²C-bus is checked by the software during the transfer of information to the device. The above message is displayed if the I²C-bus has a data bit zero-conflict when the bit was supposed to be a one.

```
*********************************************
*                                           *
* WARNING !! - I2C write of 0 failed !!!    *
*                                           *
*       (press any key to continue)         *
*                                           *
*********************************************
```

The state of the I²C-bus is checked by the software during the transfer of information to the device. The above message is displayed if the I²C-bus has a data bit one-conflict when the bit was supposed to be a zero.

```
*********************************************
*                                           *
* WARNING !! - I2C Bus not in ACTIVE state !! *
*                                           *
*       (press any key to continue)         *
*                                           *
*********************************************
```

The state of the I²C-bus is checked by the software just *before* a STOP command is given to the device. The above message is displayed if the I²C-bus has inadvertently become idle (before the STOP command is given) when it is supposed to be active.

```
*********************************************
*                                           *
* WARNING !! - I2C Bus not in IDLE state !! *
*                                           *
*       (press any key to continue)         *
*                                           *
*********************************************
```

The state of the I²C-bus is checked by the software just *after* a STOP command is given to the device. The above message is displayed if the I²C-bus has not become idle (after the STOP command is given).

```
*******************************************
* WARNING !! - Hardware error detected !! *
*******************************************
```

This error occurs if I²C communication cannot be established with the device.

Table 18: Cable Interface

Color	J1	DB25	Signal
Red	1	2	SCL
White	2	16	SDA
Green	3	8	ADDR
Blue	4	5	PSEL1
Brown	5	4	PSEL0
Black	6	25	GND

Figure 13: Board Silkscreen

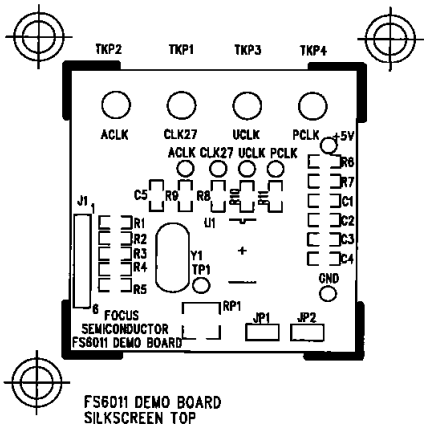


Figure 14: Board Traces - Component Side

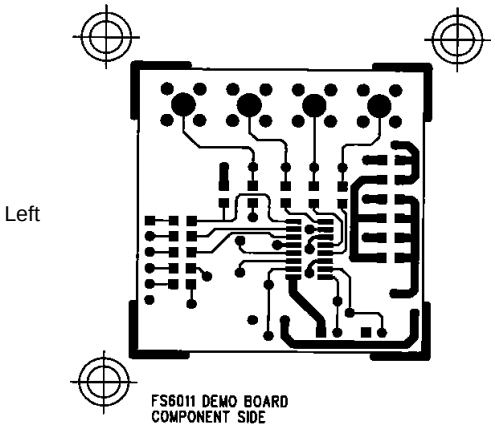


Figure 15: Board Traces - Solder Side