

## Product Summary

$V_{(BR)DSS}$	$R_{DS(on) \max}$	$I_D$ $T_C = +25^\circ\text{C}$
700V	$1.25\Omega @ V_{GS} = 10V$	3.9A

## Description

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## Applications

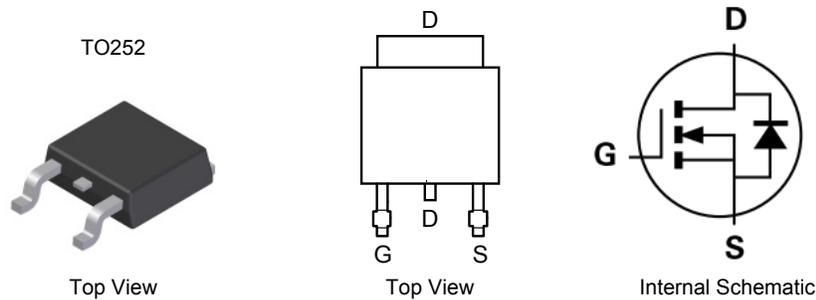
- Switching

## Features

- 100% Unclamped Inductive Switch (UIS) test in production
- Low Gate Input Resistance
- Low Input Capacitance
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability**

## Mechanical Data

- Case: TO252 (DPAK)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208  $\text{E3}$
- Weight: 0.33 grams (approximate)

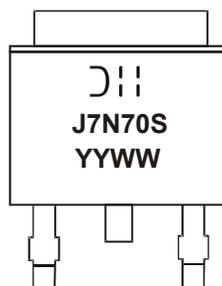


## Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
DMJ7N70SK3-13	Standard	TO252	2,500/Tape & Reel

- Notes:
- EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  - See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  - For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



$\text{J7N70S}$  = Manufacturer's Marking  
 $\text{J7N70S}$  = Product Type Marking Code  
 $\text{YYWW}$  = Date Code Marking  
 $\text{YY}$  = Last Digit of Year (ex: 13 = 2013)  
 $\text{WW}$  = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	700	V
Gate-Source Voltage	V <sub>GSS</sub>	±30	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 10V	I <sub>D</sub>	T <sub>C</sub> = +25°C	3.9
		T <sub>C</sub> = +100°C	2.5
Maximum Body Diode Forward Current (Note 5)	I <sub>S</sub>	3.0	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I <sub>DM</sub>	15.6	A
Avalanche Current (Note 6)	I <sub>AR</sub>	1.5	A
Avalanche Energy (Note 6)	E <sub>AR</sub>	76	mJ
Peak Diode Recovery dv/dt	dv/dt	11.8	V/ns

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	T <sub>C</sub> = +25°C	28
		T <sub>C</sub> = +100°C	11
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	38	°C/W
Thermal Resistance, Junction to Case (Note 5)	R <sub>θJC</sub>	2.1	
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	700	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 700V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	100	nA	V <sub>GS</sub> = ±30V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	2	2.9	4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	1	1.25	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A
Diode Forward Voltage	V <sub>SD</sub>	—	0.9	1.3	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 5A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	351	—	pF	V <sub>DS</sub> = 50V, f = 1MHz, V <sub>GS</sub> = 0V
Output Capacitance	C <sub>oss</sub>	—	66	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	1.1	—		
Gate Resistance	R <sub>G</sub>	—	3.5	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	13.9	—	nC	V <sub>DD</sub> = 560V, I <sub>D</sub> = 5A, V <sub>GS</sub> = 10V
Gate-Source Charge	Q <sub>gs</sub>	—	1.9	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	8.5	—		
Turn-On Delay Time	t <sub>D(on)</sub>	—	8.5	—	ns	V <sub>DD</sub> = 350V, V <sub>GS</sub> = 10V, R <sub>G</sub> = 4.7Ω, I <sub>D</sub> = 2.5A
Turn-On Rise Time	t <sub>r</sub>	—	11.6	—		
Turn-Off Delay Time	t <sub>D(off)</sub>	—	24.5	—		
Turn-Off Fall Time	t <sub>f</sub>	—	10	—		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	—	212	—	ns	I <sub>S</sub> = 5A, dI/dt = 100A/µs
Body Diode Reverse Recovery Time (T <sub>J</sub> = +150°C)	t <sub>rr</sub>	—	251	—	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	—	1.8	—	µC	
Body Diode Reverse Recovery Charge (T <sub>J</sub> = +150°C)	Q <sub>rr</sub>	—	2.3	—	µC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper pad layout.
  - UIS in production with V<sub>DD</sub> = 50V, V<sub>GS</sub> = 10V, L = 60mH, T<sub>J</sub> = +25°C.
  - Short duration pulse test used to minimize self-heating effect
  - Guaranteed by design. Not subject to production testing

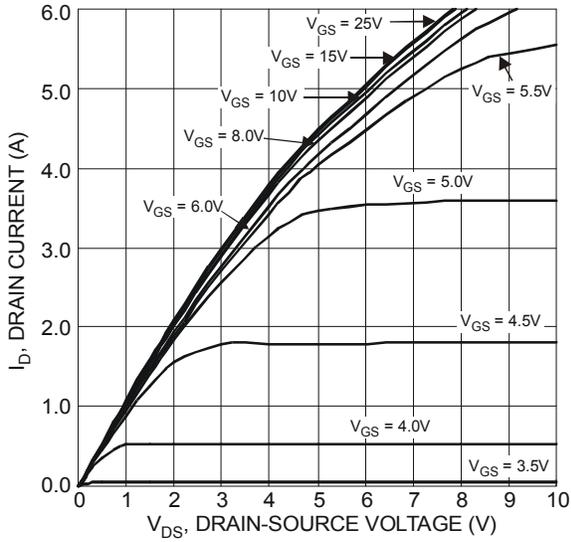


Figure 1 Typical Output Characteristics

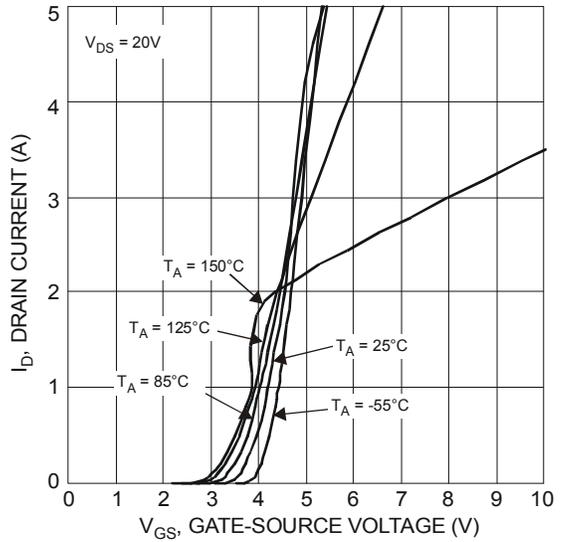


Figure 2 Typical Transfer Characteristics

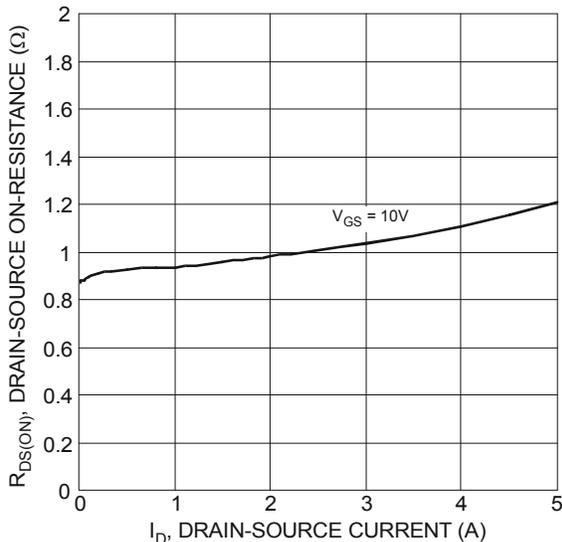


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

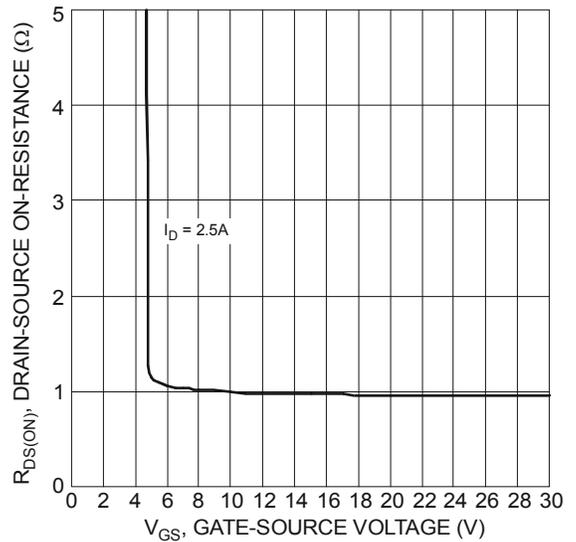


Figure 4 Typical Transfer Characteristics

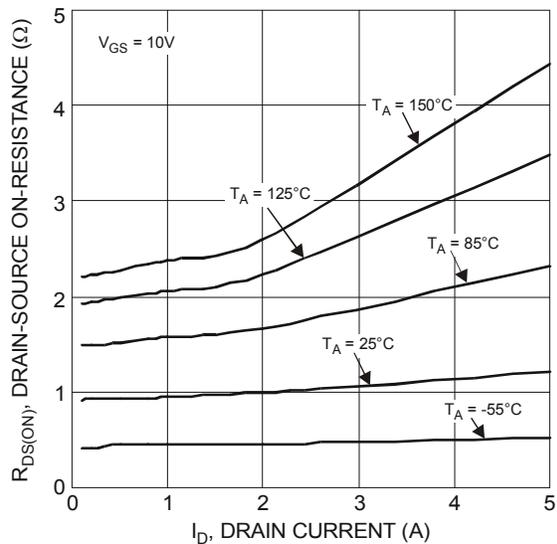


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

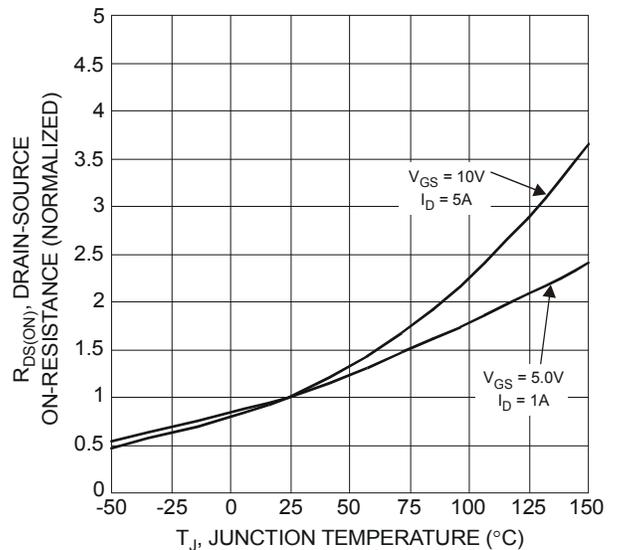


Figure 6 On-Resistance Variation with Temperature

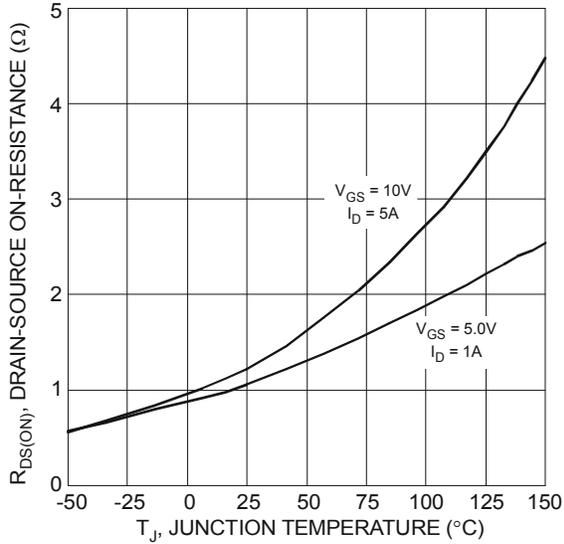


Figure 7 On-Resistance Variation with Temperature

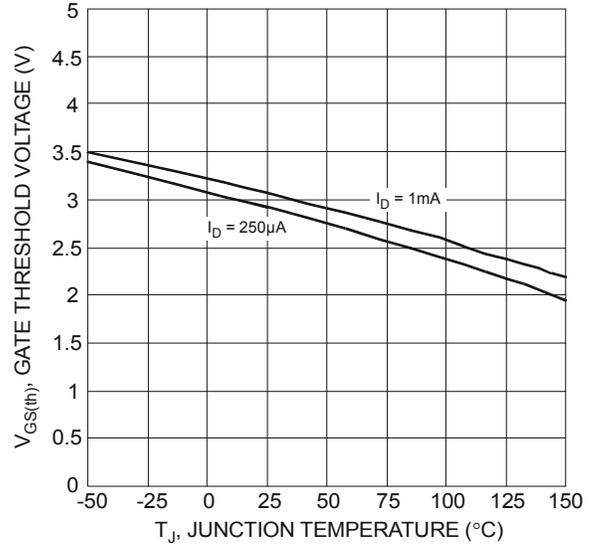


Figure 8 Gate Threshold Variation vs. Ambient Temperature

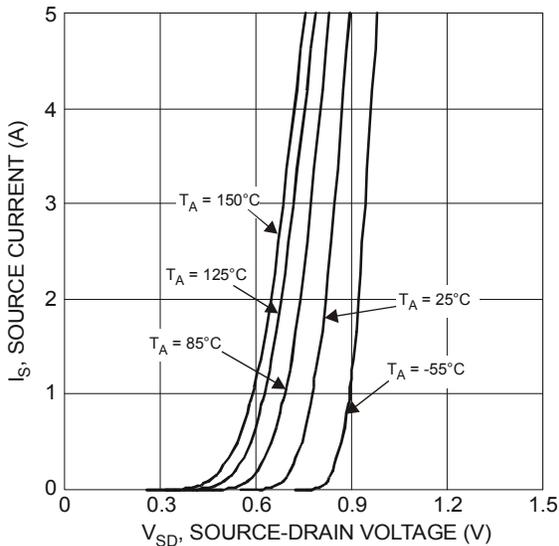


Figure 9 Diode Forward Voltage vs. Current

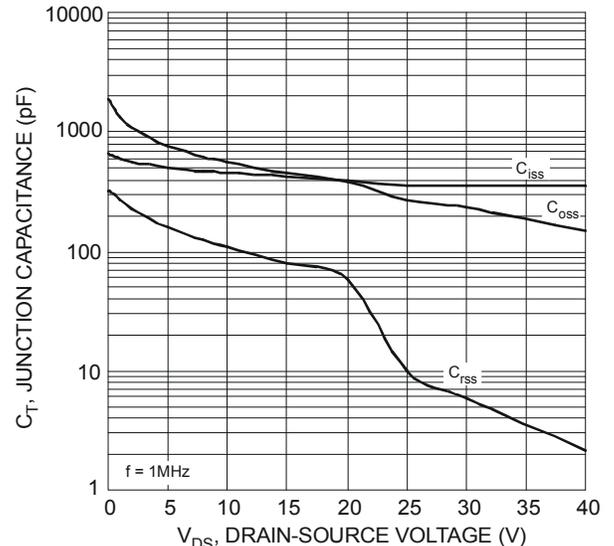


Figure 10 Typical Junction Capacitance

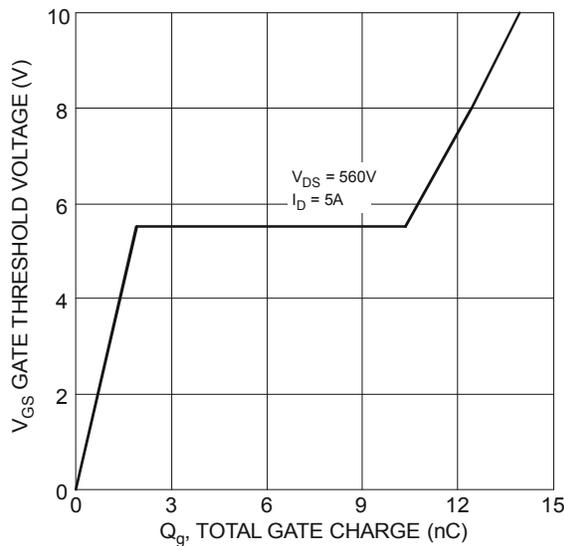


Figure 11 Gate Charge

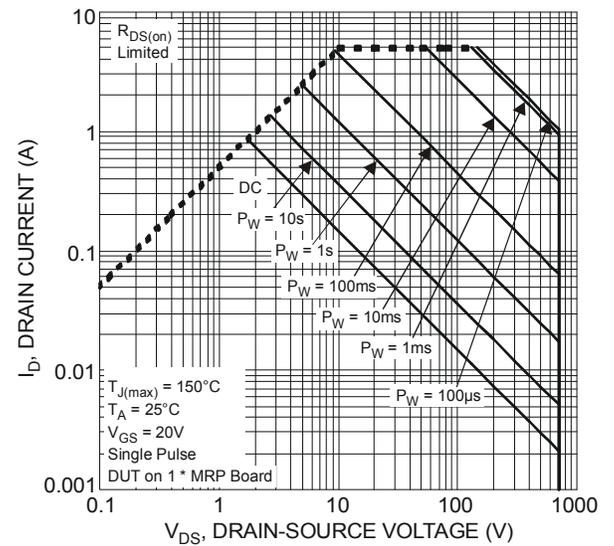
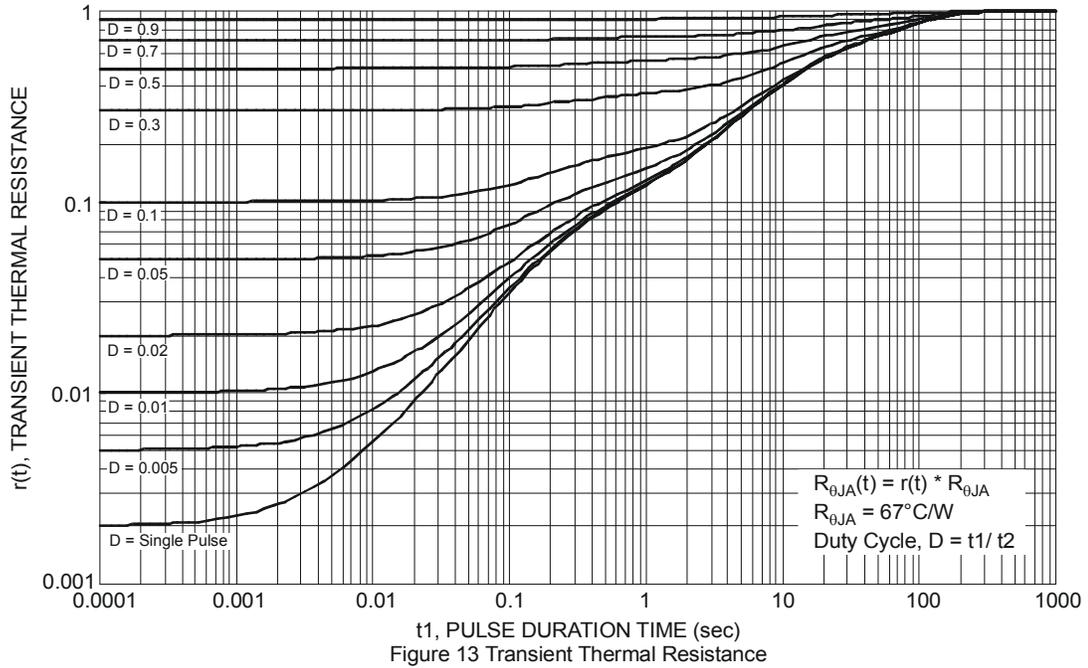
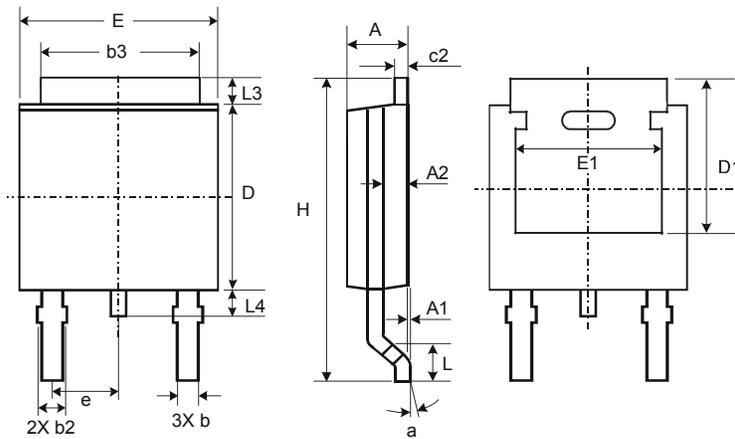


Figure 12 SOA, Safe Operation Area



**Package Outline Dimensions**

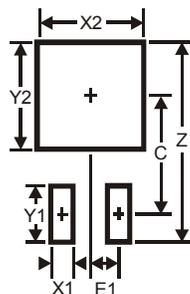
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



TO252			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c2	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
Z	11.6
X1	1.5
X2	7.0
Y1	2.5
Y2	7.0
C	6.9
E1	2.3

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