

DATA SHEET

83C576/87C576

80C51 8-bit microcontroller family

8K/256 OTP/ROM, 6 channel 10-bit A/D,
4 comparators, failure detect circuitry, watchdog timer

Product specification
Supersedes data of 1998 Jan 06
IC20 Data Handbook

1998 Jun 04

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FEATURES

- 80C51 based architecture
 - 8k × 8 ROM (83C576)
 - 8k × 8 EPROM (87C576)
 - 256 × 8 RAM
 - 10-bit, 6 channel A/D
 - Three 16-bit counter/timers
 - 2 PWM outputs
 - Programmable Counter Array
 - Universal Peripheral Interface
 - Enhanced UART
 - Oscillator fail detect
 - Low active reset
 - 4 analog comparators
 - Watchdog timer
 - Low V_{CC} detect
 - Power-on detect
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- 6 to 16MHz
- Extended temperature ranges

- OTP available
- That can be programmed in circuit
- Software Reset
- 15 source, 2 level interrupt structure
- Lower EMI noise
- Programmable I/O pins
- Serial on-board programming
- Schmitt trigger inputs on Port 1

DESCRIPTION

The Philips 83C576/87C576 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC576 contains an 8k × 8 ROM (83C576) EPROM (87C576), a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a Programmable Counter Array (PCA), a 10-bit, 6 channel A/D, 2 PWM outputs, an 8-bit UPI interface, a fifteen-source, two-priority level nested interrupt structure, an enhanced UART, four analog comparators, power-fail detect and oscillator fail detect circuits, and on-chip oscillator and clock circuits.

In addition, the 8XC576 has a low active reset, and a software reset. There is also a fully configurable watchdog timer, and internal power on clear circuit. The part includes idle mode and power-down mode states for reduced power consumption.

ORDERING INFORMATION

ROM	EPROM ¹		TEMPERATURE RANGE °C AND PACKAGE	FREQ (MHz)	DRAWING NUMBER
P83C576EBPN	P87C576EBPN	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P83C576EBAA	P87C576EBAA	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
P83C576EBBB	P87C576EBBB	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	16	SOT307-2
P83C576EFPN	P87C576EBPN	OTP	–40 to +85, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P83C576EFAA	P87C576EFAA	OTP	–40 to +85, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
P83C576EFBB	P87C576EFBB	OTP	–40 to +85, 44-Pin Plastic Quad Flat Pack	16	SOT307-2
P83C576EHPN	P87C576EHPN	OTP	–40 to +125, 40-Pin Plastic Dual In-line Package	16	SOT129-1
P83C576EHAA	P87C576EHAA	OTP	–40 to +125, 44-Pin Plastic Leaded Chip Carrier	16	SOT187-2
P83C576EHBB	P87C576EHBB	OTP	–40 to +125, 44-Pin Plastic Quad Flat Pack	16	SOT307-2

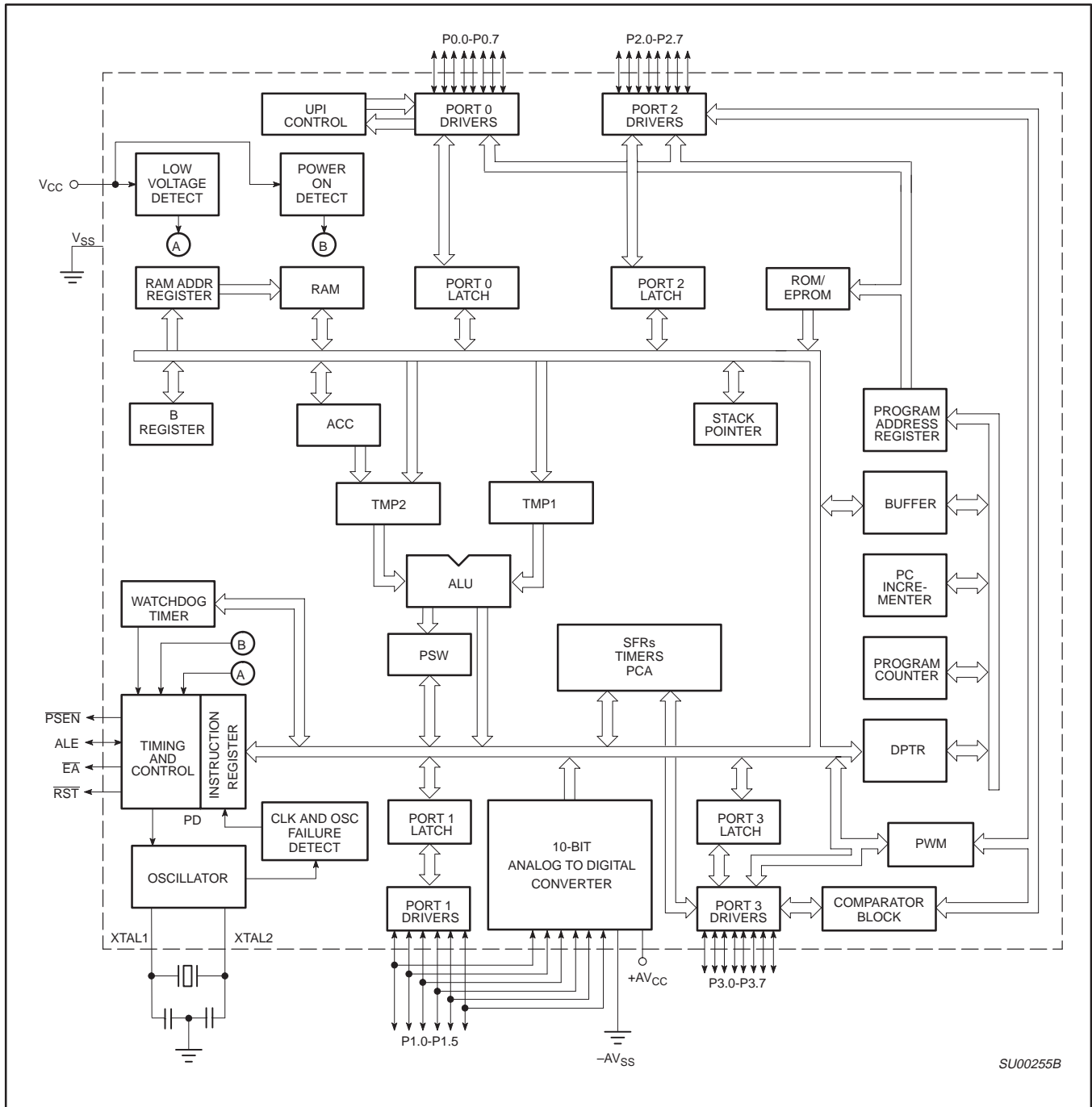
NOTE:

1. OTP - One Time Programmable EPROM.

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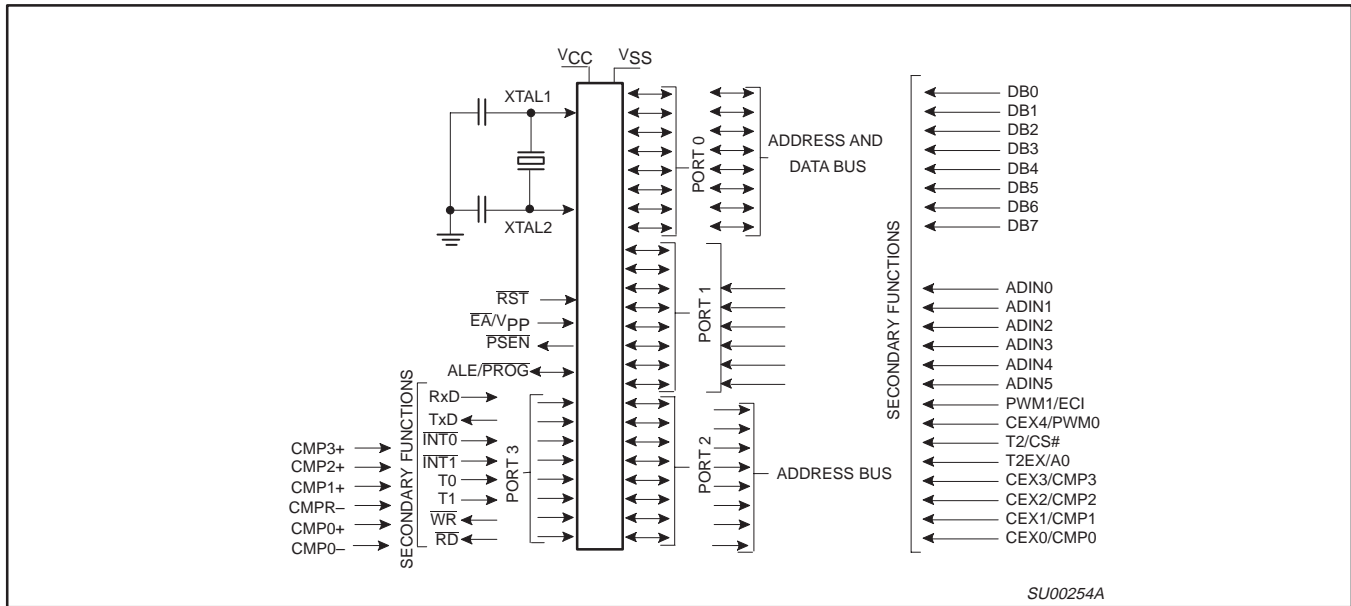
BLOCK DIAGRAM



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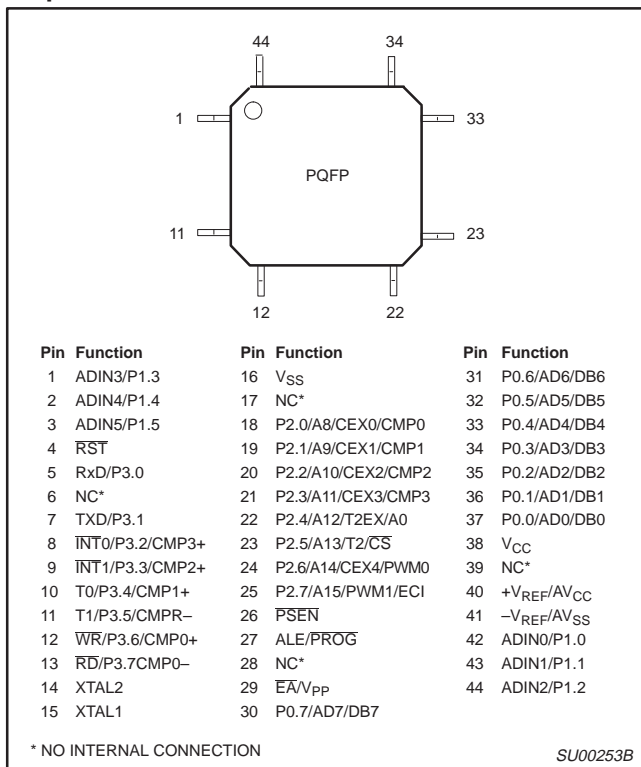
83C576/87C576

LOGIC SYMBOL

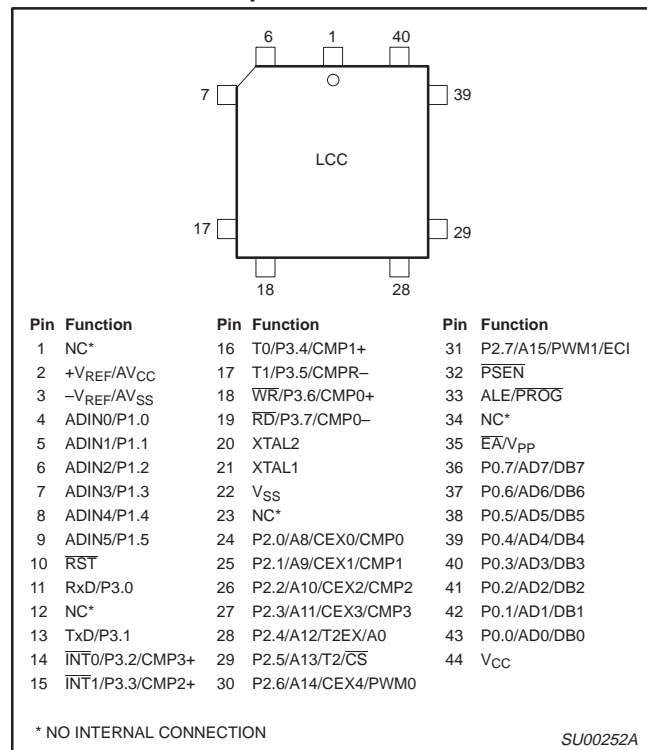


PIN CONFIGURATIONS

44-pin Plastic Quad Flat Pack



Plastic Leaded Chip Carrier



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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION																																																																																																																					
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V _{SS}	20	22	16	I	Ground: 0V reference.																																																																																																																					
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.																																																																																																																					
P0.0-0.7	39-32	43-36	37-30	I/O	<p>Port 0: Port 0 is a bidirectional I/O port. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory (see Note 5). In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also receives code bytes during parallel EPROM programming and outputs code bytes during verification. External pull-ups are required during program verification. During reset, the port register is loaded with 1's. Port 0 has 4 output modes selected on a per bit basis by writing to the P0M1 and P0M2 Special Function Registers as follows:</p> <table border="1"> <thead> <tr> <th>P0M1.x</th> <th>P0M2.x</th> <th>Mode Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Open drain (default). See Note 1.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Weak pullup. See Note 2.</td> </tr> <tr> <td>1</td> <td>0</td> <td>High impedance. See Note 3.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Push-pull. See Note 4.</td> </tr> </tbody> </table> <p>Port 0 is also the data I/O port for the Universal Peripheral Interface (UPI). When the UPI is enabled, port 0 must be configured as High-Z by the user. Input/Output through P0 is controlled by pin \overline{CS}, \overline{WR}, \overline{RD}, and A0. Output is push-pull when enabled.</p>	P0M1.x	P0M2.x	Mode Description	0	0	Open drain (default). See Note 1.	0	1	Weak pullup. See Note 2.	1	0	High impedance. See Note 3.	1	1	Push-pull. See Note 4.																																																																																																						
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P1.0-P1.5	3-8	5-9	42-44 1-3	I/O	<p>Port 1: Port 1 is a 6-bit bidirectional I/O port with Schmitt trigger inputs. Port 1 receives the control signals during program memory verification and parallel EPROM programming. During reset, port 1 is configured as a high impedance analog input port. Digital push-pull outputs are enabled by writing 1's to the P1M1 register. The programmer must take care to prevent digital outputs from switching while an A/D conversion is in progress. Port 1 has 3 output modes selected on a per bit basis by writing to the P1M1 and P1M2 special function registers as follows:</p> <table border="1"> <thead> <tr> <th>P1M1.X</th> <th>P1M2.X</th> <th>Mode Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>A/D only. (High impedance)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Digital input only. High impedance (default).</td> </tr> <tr> <td>1</td> <td>X</td> <td>Push-pull.</td> </tr> </tbody> </table> <p>Port 1 pins also serve alternate functions as follows:</p> <table border="1"> <thead> <tr> <th>Pin</th> <th>DIP</th> <th>LCC</th> <th>QFP</th> <th>Type</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>3</td> <td>4</td> <td>42</td> <td>I/O</td> <td>P1.0/ADIN0</td> </tr> <tr> <td>4</td> <td>5</td> <td>43</td> <td>I/O</td> <td>P1.1/ADIN1</td> </tr> <tr> <td>5</td> <td>6</td> <td>44</td> <td>I/O</td> <td>P1.2/ADIN2</td> </tr> <tr> <td>6</td> <td>7</td> <td>1</td> <td>I/O</td> <td>P1.3/ADIN3</td> </tr> <tr> <td>7</td> <td>8</td> <td>2</td> <td>I/O</td> <td>P1.4/ADIN4</td> </tr> <tr> <td>8</td> <td>9</td> <td>3</td> <td>I/O</td> <td>P1.5/ADIN5</td> </tr> </tbody> </table>	P1M1.X	P1M2.X	Mode Description	0	0	A/D only. (High impedance)	0	1	Digital input only. High impedance (default).	1	X	Push-pull.	Pin	DIP	LCC	QFP	Type	Function	3	4	42	I/O	P1.0/ADIN0	4	5	43	I/O	P1.1/ADIN1	5	6	44	I/O	P1.2/ADIN2	6	7	1	I/O	P1.3/ADIN3	7	8	2	I/O	P1.4/ADIN4	8	9	3	I/O	P1.5/ADIN5																																																																					
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P2.0-P2.7	21-28	24-31	18-25	I/O	<p>Port 2: Port 2 is an 8-bit bidirectional I/O port. Port 2 emits the high-order address byte during accesses to external program and data memory that use 16-bit addresses (MOVX @DPTR) (see Note 5). In this application, it uses strong internal pull-ups when emitting 1s. Port 2 receives the high-order address byte during program verification and parallel EPROM programming. During reset, the port 2 pullups are turned on synchronously, and the port register is loaded with 1's. Port 2 has the following output modes which can be selected on a per bit basis by writing to P2M1 and P2M0:</p> <table border="1"> <thead> <tr> <th>P2M1.X</th> <th>P2M2.X</th> <th>Mode Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Open drain. See Note 1.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Weak pullup (default). See Note 2.</td> </tr> <tr> <td>1</td> <td>0</td> <td>High impedance. See Note 3.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Push-pull. See Note 4.</td> </tr> </tbody> </table> <p>Port 2 pins serve alternate functions as follows:</p> <table border="1"> <thead> <tr> <th>Pin</th> <th>DIP</th> <th>LCC</th> <th>QFP</th> <th>Type</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>21</td> <td>24</td> <td>18</td> <td>P2.0</td> <td>CEX0</td> <td>PCA module 0 external I/O</td> </tr> <tr> <td></td> <td></td> <td></td> <td>CEX0</td> <td>CMP0</td> <td>comparator 0 output</td> </tr> <tr> <td>22</td> <td>25</td> <td>19</td> <td>P2.1</td> <td>CEX1</td> <td>PCA module 1 external I/O</td> </tr> <tr> <td></td> <td></td> <td></td> <td>CEX1</td> <td>CMP1</td> <td>comparator 1 output</td> </tr> <tr> <td>23</td> <td>26</td> <td>20</td> <td>P2.2</td> <td>CEX2</td> <td>PCA module 2 external I/O</td> </tr> <tr> <td></td> <td></td> <td></td> <td>CEX2</td> <td>CMP2</td> <td>comparator 2 output</td> </tr> <tr> <td>24</td> <td>27</td> <td>21</td> <td>P2.3</td> <td>CEX3</td> <td>PCA module 3 external I/O</td> </tr> <tr> <td></td> <td></td> <td></td> <td>CEX3</td> <td>CMP3</td> <td>comparator 3 output</td> </tr> <tr> <td>25</td> <td>28</td> <td>22</td> <td>P2.4</td> <td>T2EX</td> <td>timer 2 capture input</td> </tr> <tr> <td></td> <td></td> <td></td> <td>P2.4</td> <td>A0</td> <td>UPI address input</td> </tr> <tr> <td>26</td> <td>29</td> <td>23</td> <td>P2.5</td> <td>T2</td> <td>timer 2 external I/O — clock-out (programmable)</td> </tr> <tr> <td></td> <td></td> <td></td> <td>P2.5</td> <td>CS</td> <td>UPI chip select input</td> </tr> <tr> <td>27</td> <td>30</td> <td>24</td> <td>P2.6</td> <td>CEX4</td> <td>PCA module 4 external I/O</td> </tr> <tr> <td></td> <td></td> <td></td> <td>P2.6</td> <td>PWM0</td> <td>Pulse width modulator 0 output</td> </tr> <tr> <td>28</td> <td>31</td> <td>25</td> <td>P2.7</td> <td>ECl</td> <td>PCA count input</td> </tr> <tr> <td></td> <td></td> <td></td> <td>P2.7</td> <td>PWM1</td> <td>Pulse width modulator 1 output</td> </tr> </tbody> </table>	P2M1.X	P2M2.X	Mode Description	0	0	Open drain. See Note 1.	0	1	Weak pullup (default). See Note 2.	1	0	High impedance. See Note 3.	1	1	Push-pull. See Note 4.	Pin	DIP	LCC	QFP	Type	Function	21	24	18	P2.0	CEX0	PCA module 0 external I/O				CEX0	CMP0	comparator 0 output	22	25	19	P2.1	CEX1	PCA module 1 external I/O				CEX1	CMP1	comparator 1 output	23	26	20	P2.2	CEX2	PCA module 2 external I/O				CEX2	CMP2	comparator 2 output	24	27	21	P2.3	CEX3	PCA module 3 external I/O				CEX3	CMP3	comparator 3 output	25	28	22	P2.4	T2EX	timer 2 capture input				P2.4	A0	UPI address input	26	29	23	P2.5	T2	timer 2 external I/O — clock-out (programmable)				P2.5	CS	UPI chip select input	27	30	24	P2.6	CEX4	PCA module 4 external I/O				P2.6	PWM0	Pulse width modulator 0 output	28	31	25	P2.7	ECl	PCA count input				P2.7	PWM1	Pulse width modulator 1 output
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PIN DESCRIPTIONS (Continued)

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	DIP	LCC	QFP																																												
+V _{REF} /AV _{CC}	1	2	40	I	A/D positive power supply																																										
-V _{REF} /AV _{SS}	2	3	41	I	A/D 0V reference																																										
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<p>Port 3: Port 3 is an 8-bit bidirectional I/O port. Port 3 pins that have 1s written to them can be used as inputs but will source current when externally pulled low (see DC Electrical Characteristics: I_{IL}). During reset all pins will be synchronously driven high and will remain high until written to by software. Port 3 has the following output modes which can be selected on a per bit basis by writing to P3M1 and P3M2:</p> <table border="1"> <thead> <tr> <th>P3M1.X</th> <th>P3M2.X</th> <th>Mode Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Open drain. See Note 1.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Weak pullup (default). See Note 2.</td> </tr> <tr> <td>1</td> <td>0</td> <td>High impedance. See Note 3.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Push-pull. See Note 4.</td> </tr> </tbody> </table> <p>Port 3 pins serve alternate functions as follows:</p> <table border="1"> <thead> <tr> <th>Pin</th> <th>Function</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>P3.0</td> <td>RxD</td> <td>Serial receive port</td> </tr> <tr> <td>P3.1</td> <td>TxD</td> <td>Serial transmit port (enabled only when transmitting serial data)</td> </tr> <tr> <td>P3.2</td> <td>INT0</td> <td>External interrupt 0</td> </tr> <tr> <td>P3.3</td> <td>INT1</td> <td>External interrupt 1</td> </tr> <tr> <td>P3.4</td> <td>T0</td> <td>Timer/counter 0 input</td> </tr> <tr> <td>P3.5</td> <td>T1</td> <td>Timer/counter 1 input</td> </tr> <tr> <td>P3.6</td> <td>WR</td> <td>External data memory write strobe</td> </tr> <tr> <td>P3.7</td> <td>RD</td> <td>External data memory read strobe</td> </tr> </tbody> </table>	P3M1.X	P3M2.X	Mode Description	0	0	Open drain. See Note 1.	0	1	Weak pullup (default). See Note 2.	1	0	High impedance. See Note 3.	1	1	Push-pull. See Note 4.	Pin	Function	Description	P3.0	RxD	Serial receive port	P3.1	TxD	Serial transmit port (enabled only when transmitting serial data)	P3.2	INT0	External interrupt 0	P3.3	INT1	External interrupt 1	P3.4	T0	Timer/counter 0 input	P3.5	T1	Timer/counter 1 input	P3.6	WR	External data memory write strobe	P3.7	RD	External data memory read strobe
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RST	9	10	4	I	<p>Reset: A low on this pin synchronously resets all port pins to a high state. The pin must be held low with the oscillator running for 24 oscillator cycles to initialize the internal registers. An internal diffused resistor to V_{CC} permits a power on reset using only an external capacitor to V_{SS}. RST has a Schmitt trigger input stage to provide additional noise immunity with a slow rising input voltage.</p>																																										
ALE/PROG	30	33	27	I/O	<p>Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE is switched off if the bit 0 in the AUXR register (8EH) is set. This pin is also the program pulse input ($\overline{\text{PROG}}$) during parallel EPROM programming. (See also Internal Reset on page 24.)</p>																																										
PSEN	29	32	26	O	<p>Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.</p>																																										
E $\overline{\text{A}}$ /V _{PP}	31	35	29	I	<p>External Access Enable/Programming Supply Voltage: E$\overline{\text{A}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If E$\overline{\text{A}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If this pin is at V_{PP} voltage during reset the device enters the in-circuit programming mode.</p>																																										
XTAL1	19	21	15	I	<p>Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.</p>																																										
XTAL2	18	20	14	O	<p>Crystal 2: Output from the inverting oscillator amplifier.</p>																																										

NOTES:

- When Open Drain mode is selected, ports 0 and 2 have weak pulldowns to guarantee positive leakage current (see DC electrical characteristic I_{IH}).
- When Weak Pullup mode is selected, ports bits that have 1's written to them can be used as inputs but will source current when externally pulled low (see DC electrical characteristic I_{IL}).
- When High Impedance mode is selected, all pullups and pulldowns are turned off. The only current sourced or sunk by the pin is the parasitic leakage current (see DC electrical characteristic I_{L2} or I_{LC}, as applicable).
- When Push-Pull mode is selected, strong pullups are on continuously when emitting 1's (see DC electrical characteristic V_{OH}).
- When Open-Drain, Weak Pull-up, or Push-pull mode is selected.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

Table 1. 87C576 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB							LSB	
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
ADC0H#	A/D Channel 0 MSB	AAH									00H
ADC1H#	A/D Channel 1 MSB	ABH									00H
ADC2H#	A/D Channel 2 MSB	ACH									00H
ADC3H#	A/D Channel 3 MSB	ADH									00H
ADC4H#	A/D Channel 4 MSB	AEH									00H
ADC5H#	A/D Channel 5 MSB	AFH									00H
ADC0L#	A/D Channel 0 2-LSBits	9AH									00H
ADC1L#	A/D Channel 1 2-LSBits	9BH									00H
ADC2L#	A/D Channel 2 2-LSBits	9CH									00H
ADC3L#	A/D Channel 3 2-LSBits	9DH									00H
ADC4L#	A/D Channel 4 2-LSBits	9EH									00H
ADC5L#	A/D Channel 5 2-LSBits	9FH									00H
ADCON#	A/D Control	B1H	ADF	ADCE	AD8M	AMOD1	AMOD0	ASCA2	ASCA1	ASCA0	00H
ADCS#	A/D Channel Select	B2H									00H
AUXR#	Auxiliary	8EH	–	–	–	–	SRST	TXI	LO	AO	xxxx0000B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxB
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxB
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxB
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxB
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxB
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxB
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxB
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxB
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxB
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxB
CCAPM0#	Module 0 Mode	DAH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM3#	Module 3 Mode	DDH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM4#	Module 4 Mode	DEH	–	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCON*#	PCA Counter Control	D8H	DF	DE	DD	DC	DB	DA	D9	D8	00x00000B 00H 00H
CH#	PCA Counter High	F9H	CF	CR	–	CCF4	CCF3	CCF2	CCF1	CCF0	
CL#	PCA Counter Low	E9H									
CMOD#	PCA Counter Mode	D9H	CIDL	WDTE	–	–	–	CPS1	CPS0	ECF	00xxx000B
			C7	C6	C5	C4	C3	C2	C1	C0	
CMP*#	Comparator	C0H	EC3DP	EC2DP	EC1DP	EC0DP	C3RO	C2RO	C1RO	C0RO	00H
CMPE#	Comparator Enable	92H	EC3TDC	EC2TDC	EC1TDC	EC0TDC	EC3O	EC2O	EC1O	EC0O	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H	AF	AE	AD	AC	AB	AA	A9	A8	00H
IE0*#	Interrupt Enable 0	A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H
IE1*#	Interrupt Enable 1	E8H	EOB	EIB	EAD	EC4	EC3	EC2	EC1	EC0	00H

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

Table 1. 87C576 Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
IP0*	Interrupt Priority 0	B8H	BF	BE	BD	BC	BB	BA	B9	B8	x0000000B
			–	PPC	PT2	PS	PT1	PX1	PT0	PX0	
IP1*#	Interrupt Priority 1	F8H	POB	PIB	PAD	PC4	PC3	PC2	PC1	PC0	00H
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	ADIN5	ADIN4	ADIN3	ADIN2	ADIN1	ADIN0	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	ECI	CEX4	T2	T2EX	CEX3	CEX2	CEX1	CEX0	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
P0M1#	Port 0 Output Mode 1	84H									00H
P0M2#	Port 0 Output Mode 2	85H									00H
P1M1#	Port 1 Output Mode 1	94H									00H
P1M2#	Port 1 Output Mode 2	95H									3FH
P2M1#	Port 2 Output Mode 1	A4H									00H
P2M2#	Port 2 Output Mode 2	A5H									FFH
P3M1#	Port 3 Output Mode 1	B4H									00H
P3M2#	Port 3 Output Mode 2	B5H									FFH
PCON	Power Control	87H	SMOD1	SMOD0	OSF ¹	POF ¹	LVF ¹	WDT0F ¹	PD	IDL	00xxxx00B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
PWCON#	PWM Control	BCH	–	–	–	–	PWMF	EN/CLR	PWE1	PWE0	00H
PWMP#	PWM Prescaler	BDH									00H
PWM0#	PWM Register 0	BEH									00H
PWM1#	PWM Register 1	BFH									00H
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE ²	DCEN	xxxxxxxx0B

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

1. Reset value depends on reset source.
2. Programmable clock-out

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

Table 1. 87C576 Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
UCS#	UPI Control/Status	86H	ST7	ST6	ST5	ST4	UE	AF	IBF	OBE/OBF	00H
WDCON#	Watchdog Timer Control	C4H	PRE2	PRE1	PRE0	LVRE	OFRE	DPD	WDRUN	WDMOD	11111111B
WDL#	Watchdog Timer Reload	C1H									00H
WFEED1#	Watchdog Feed 1	C2H									xxH
WFEED2#	Watchdog Feed 2	C3H									xxH

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

1. Reset value depends on reset source.

The 8XC576 has a number of failure detect circuits to prevent abnormal operating conditions. These failure detect circuits generate resets as shown in Figure 1.

POWER ON CLEAR / POWER ON FLAG

An on-chip Power On Detect Circuit resets the 8XC576 and sets the Power Off Flag (PCON.4) on power up or if V_{CC} drops to zero momentarily. The POF can only be cleared by software. The RST pin is not driven by the power on detect circuit. The POF can be read by software to determine that a power failure has occurred and can also be set by software.

LOW VOLTAGE DETECT

An on-chip Low Voltage Detect circuit sets the Low Voltage Flag (PCON.3) if V_{CC} drops below V_{LOW} (see DC Electrical Characteristics) and resets the 8XC576 if the Low Voltage Reset Enable bit (WDCON.4) is set. If the LVRE is cleared, the reset is disabled but LVF will still be set if V_{CC} is low. The RST pin is not driven by the low voltage detect circuit. The LVF can be read by software to determine that V_{CC} was low. The LVF can be set or cleared by software.

OSCILLATOR FAIL DETECT

An on-chip Oscillator Fail Detect circuit sets the Oscillator Fail Flag (PCON.5) if the oscillator frequency drops below OSCF for one or more cycles (see AC Electrical Characteristics: OSCF) and resets the 8XC576 if the Oscillator Fail Reset Enable bit (WDCON.3) is set. If OFRE is cleared, the reset is disabled but OSF will still be set if the oscillator fails. The RST pin is not driven by the oscillator fail detect circuit. The OSF can be read by software to determine that an oscillator failure has occurred. The OSF can be set or cleared by software.

LOW ACTIVE RESET

One of the most notable features on this part is the low active reset. The low active reset operates exactly the same as high active reset with the exception that the part is put into the reset mode by applying a low level to the reset pin. For power-on reset it is also necessary to invert the power-on reset circuit; connecting the 8.2K resistor from the reset pin to V_{CC} and the 10 μ f capacitor from the reset pin to ground. Figure 1 shows the reset related circuitry.

When reset the port pins on the 8XC576 are driven high synchronously.

The 8XC576 also has Low voltage detection circuitry that will, if enabled, force the part to reset when V_{CC} (on the part) fails below a set level. Low Voltage Reset is enabled by a normal reset. Low Voltage Reset can be disabled by clearing LVRE (bit 4 in the WDCON SFR) then executing a watchdog feed sequence (A5H to WFEED1 followed immediately by 5AH to WFEED2). In addition there is a flag (LVF) that is set if a low voltage condition is detected. The LVF flag is set even if the Low Voltage detection circuitry is disabled. Notice that the Low voltage detection circuitry does not drive the RST# pin so the LVF flag is the only way that the microcontroller can determine if it has been reset due to a low voltage condition.

The 8XC576 has an on-chip power-on detection circuit that sets the POF (PCON.4) flag on power up or if the V_{CC} level momentarily drops to 0V. This flag can be used to determine if the part is being started from a power-on (cold start) or if a reset has occurred due to another condition (warm start).

The 8XC576 can be reset in software by setting the RST bit of the AUXR register (AUXR.3). See Figure 1 for reset diagram.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

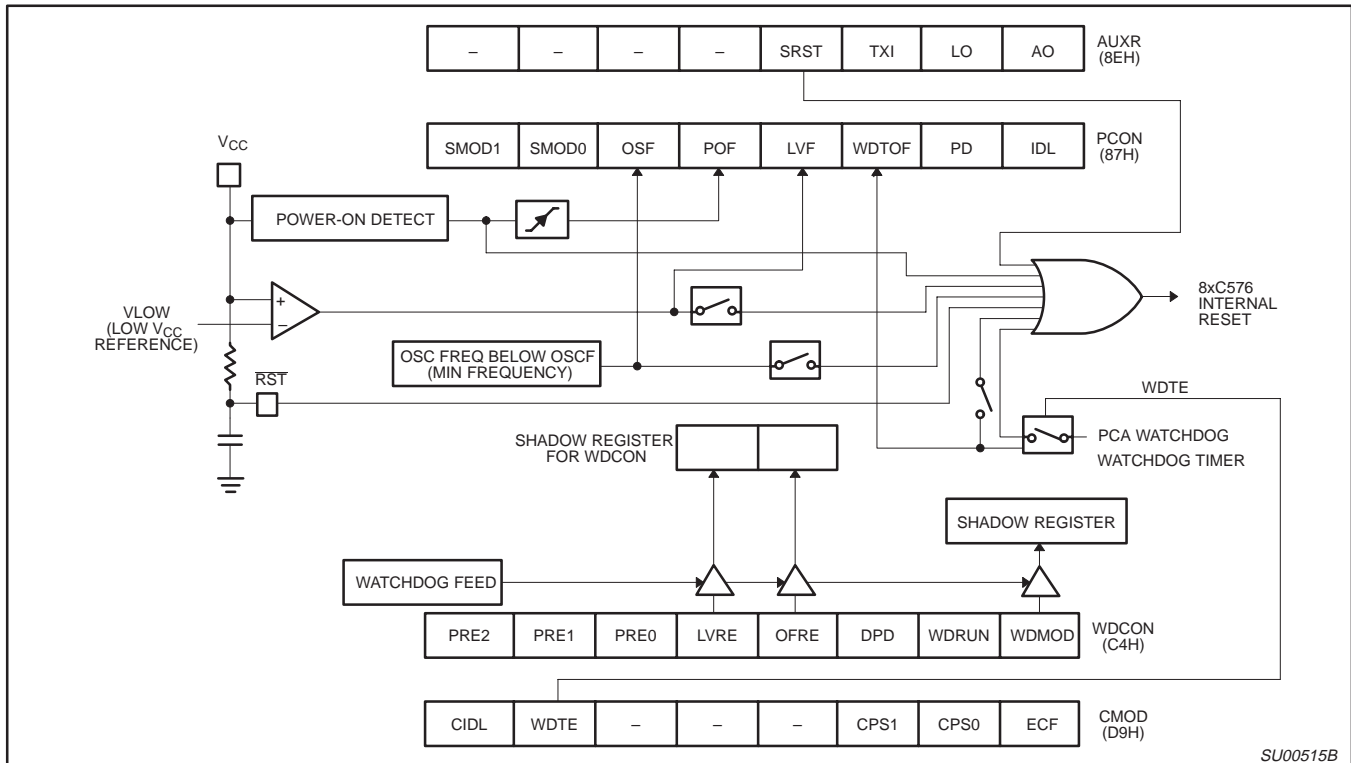


Figure 1. Reset Circuitry

TIMERS

The 8XC576 has four on-chip timers.

Timers 0 and 1 are identical in every way to Timers 0 and 1 on the 80C51.

Timer 2 on the 8XC576 is identical to the 80C52 Timer 2 (described in detail in the 80C52 overview) with the exception that it is an up or down counter. To configure the Timer to count down the DCEN bit in the T2MOD special function register must be set and a low level must be present on the T2EX pin (P1.1).

The Pulse Width Modulator (PWM) system can be used as a timer by disabling its outputs and monitoring its counter overflow flag, the PWMF bit in the PWCON register (see the PWM section for details).

The Watchdog timer operation and implementation is similar to the 8XC550 (for additional information see the 8XC550 datasheet) with the exception that the reset values of the WDCON and WDL special function registers have been changed. The changes in these registers cause the watchdog timer to be enabled with a timeout of $16384 \times T_{OSC}$ when the part is reset. The watchdog can be disabled by executing a valid feed sequence and then clearing WDRUN (bit 2 in the WDCON SFR). In timer mode, the timer is controlled by toggling the WDRUN bit. The timeout flag, WDTOF, is set when the timer overflows and must be cleared in software.

PROGRAMMABLE COUNTER ARRAY (PCA)

The Programmable Counter Array is a special Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 2. Module 0 is connected to P2.0(CEX0), module 1 to P2.1(CEX1), etc. The basic PCA configuration is shown in Figure 2.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P2.7). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 3):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin (P2.7)

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 3.

The watchdog timer function is implemented in module 4 as implemented in other parts that have a PCA that are available on the market. However, if a watchdog timer is required in the target application, it is recommended to use the hardware watchdog timer that is implemented on the 87C576 separately from the PCA (see Figure 15).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 6). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set, the CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

also can only be cleared by software. The PCA interrupt system shown in Figure 4.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 7). The registers contain the bits that control the mode that each module will operate in. The ECCFn bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 8 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 2) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 9.

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 10).

High Speed Output Mode

In this mode the CEX output (on port 2) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 11).

Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 12 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in the module's CCAPLn SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn. the allows updating the PWM without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

PCA Interrupt System

The PCA on most 80C51 family devices provides a single interrupt source, EC (IE.6). The 8xC576 expands the flexibility of the PCA by providing additional interrupt sources for each of the five PCA modules, EC0 (IE1.0) through EC4 (IE1.4), in addition to the original interrupt source EC (IE.6). Any of these sources can be enabled at any time. It is possible for both a module source (EC0 through EC4) to be enabled at the same time that the single source, EC, is enabled. In this case, a module event will generate an interrupt for both the module source and the single source, EC.

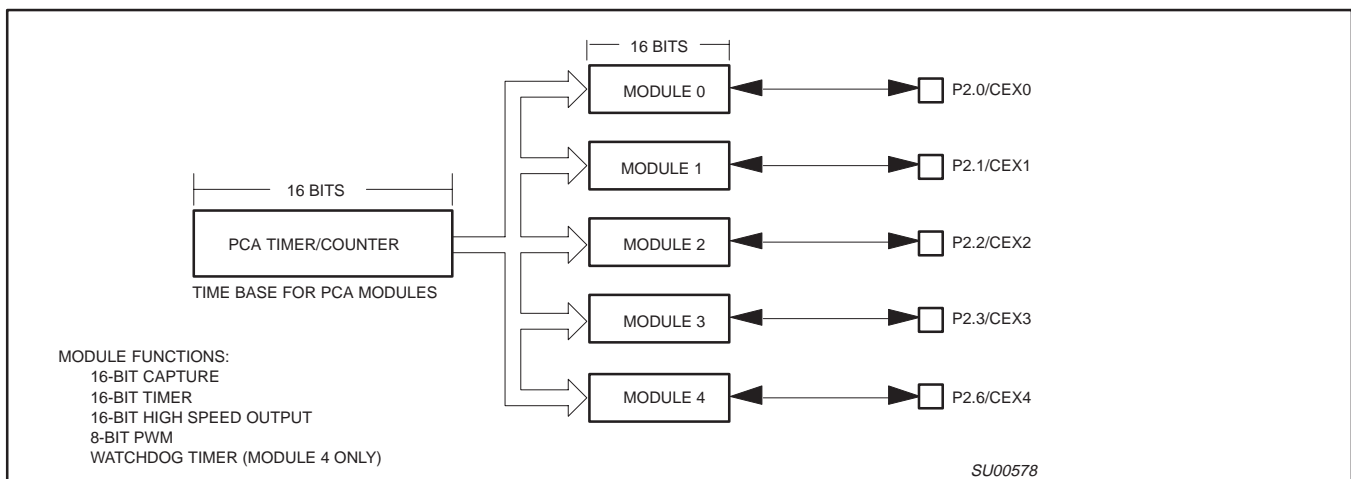


Figure 2. Programmable Counter Array (PCA)

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

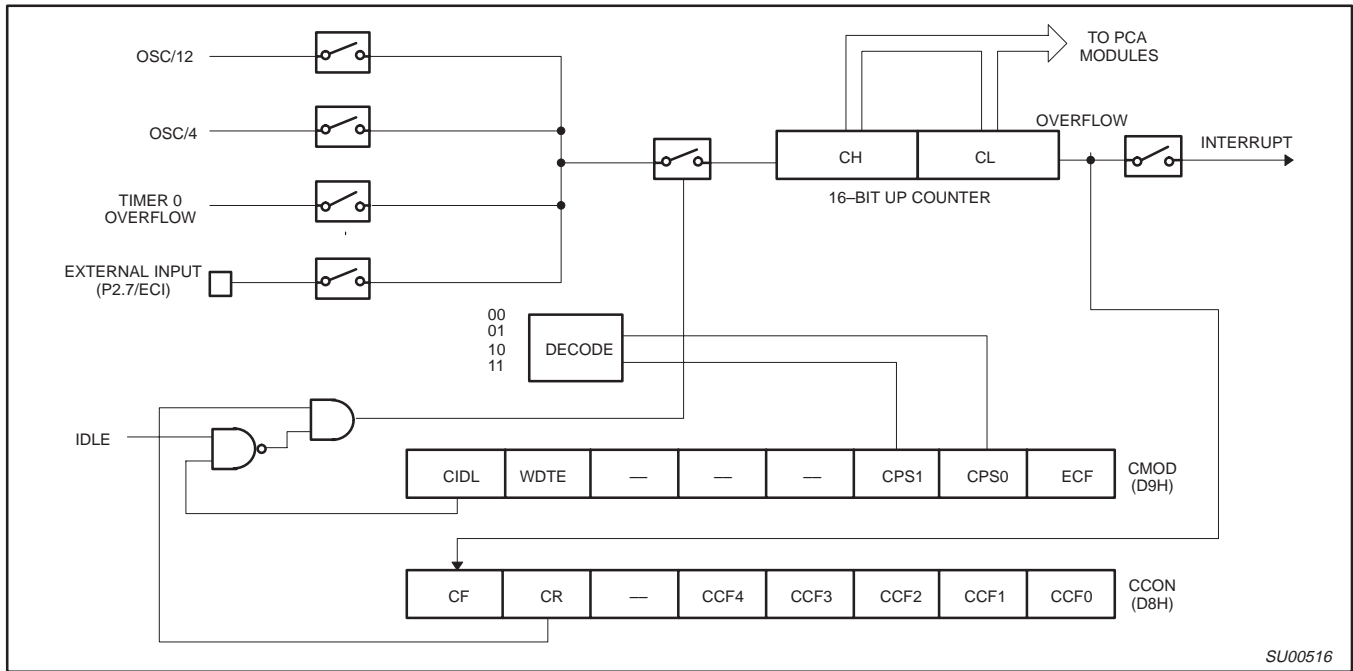


Figure 3. PCA Timer/Counter

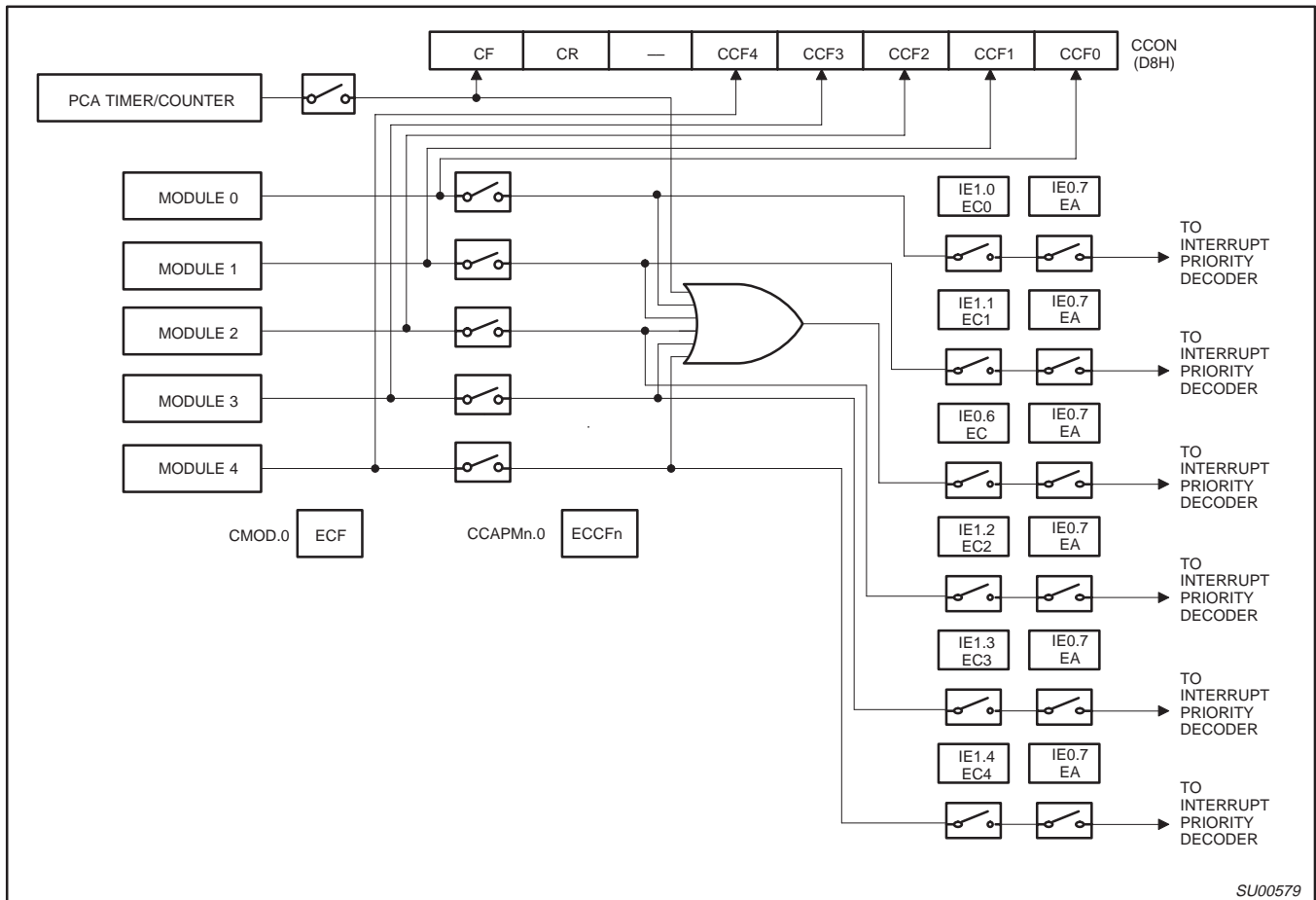


Figure 4. PCA Interrupt System

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

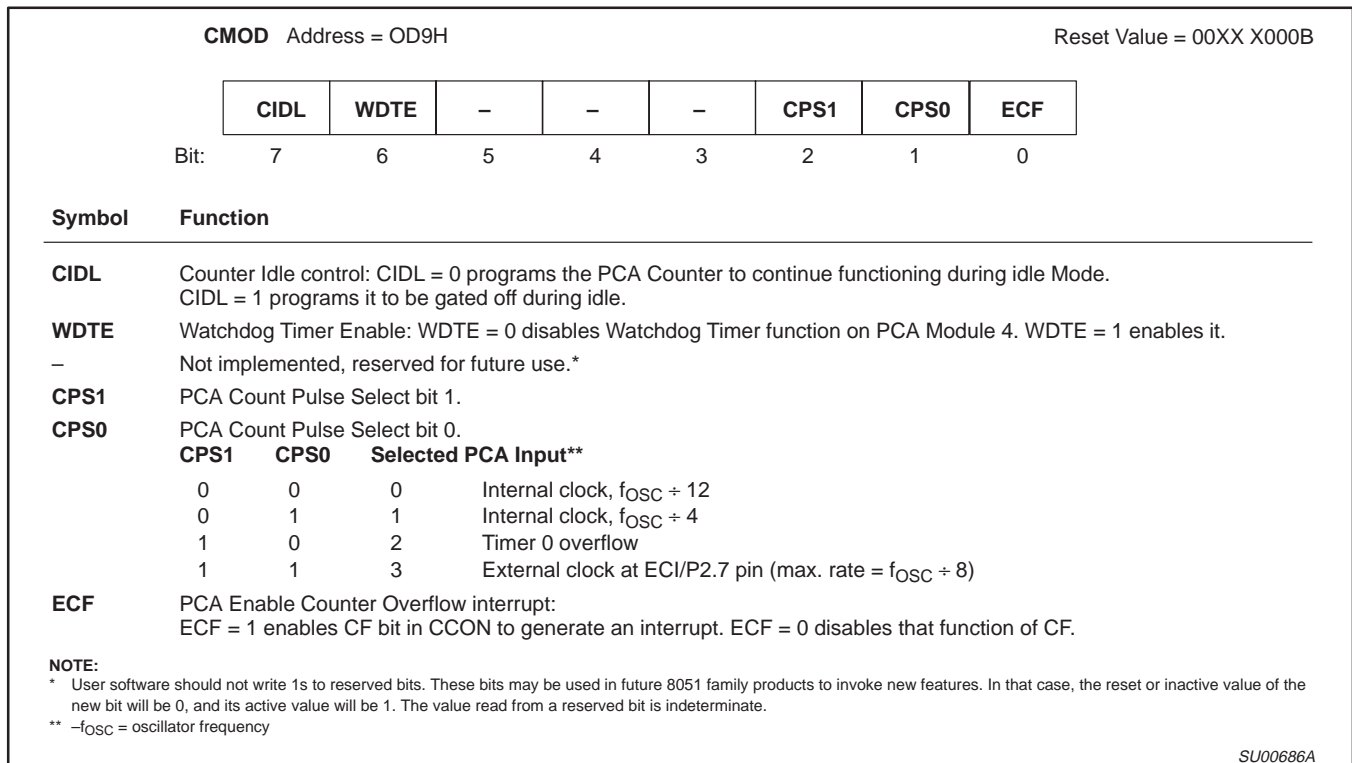


Figure 5. CMOD: PCA Counter Mode Register

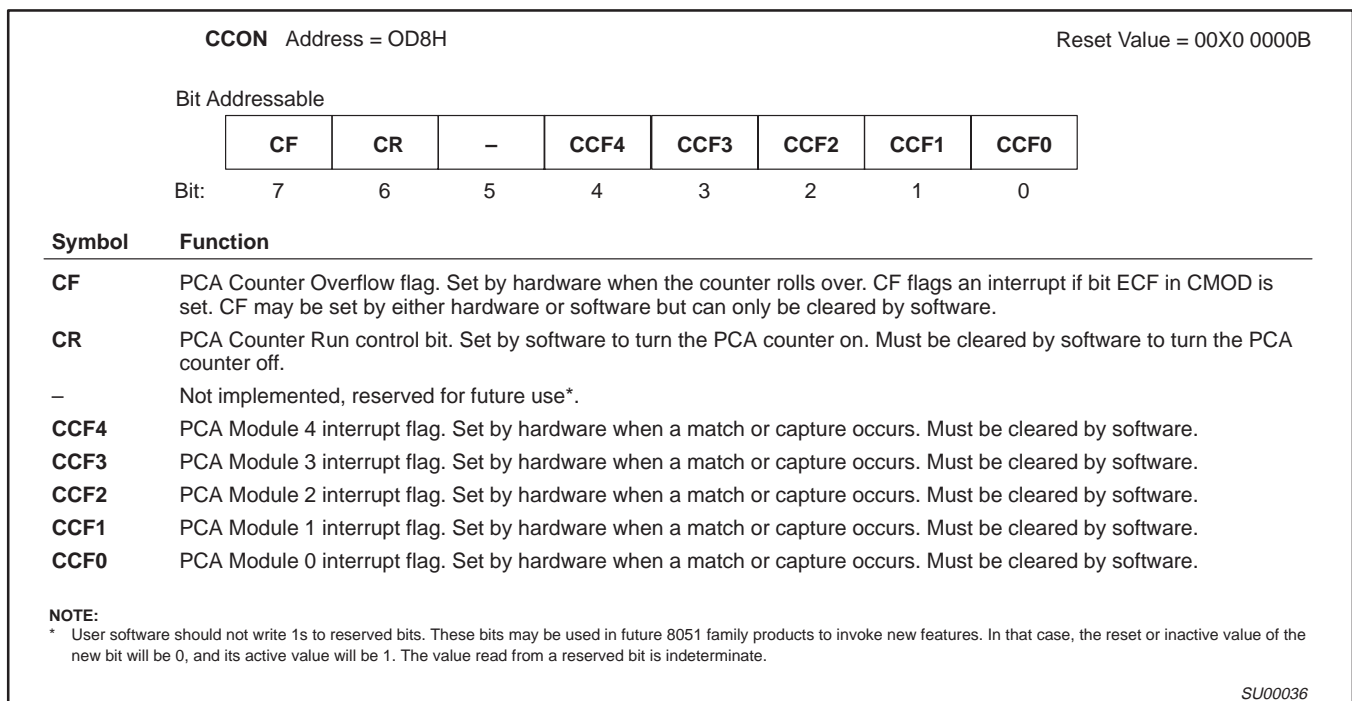


Figure 6. CCON: PCA Counter Control Register

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

CCAPMn Address	CCAPM0	0DAH						Reset Value = X000 000B
	CCAPM1	0DBH						
	CCAPM2	0DCH						
	CCAPM3	0DDH						
	CCAPM4	0DEH						
Not Bit Addressable								
	-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
Bit:	7	6	5	4	3	2	1	0
Symbol	Function							
-	Not implemented, reserved for future use*.							
ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function.							
CAPPn	Capture Positive, CAPPn = 1 enables positive edge capture.							
CAPNn	Capture Negative, CAPNn = 1 enables negative edge capture.							
MATn	Match. When MATn = 1, a match of the PCA counter with this module's compare/capture register causes the CCFn bit in CCON to be set, flagging an interrupt.							
TOGn	Toggle. When TOGn = 1, a match of the PCA counter with this module's compare/capture register causes the CEXn pin to toggle.							
PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn pin to be used as a pulse width modulated output.							
ECCFn	Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate an interrupt.							
NOTE:								
*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.								
SU00037								

Figure 7. CCAPMn: PCA Modules Compare/Capture Registers

-	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 8. PCA Module Modes (CCAPMn Register)

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

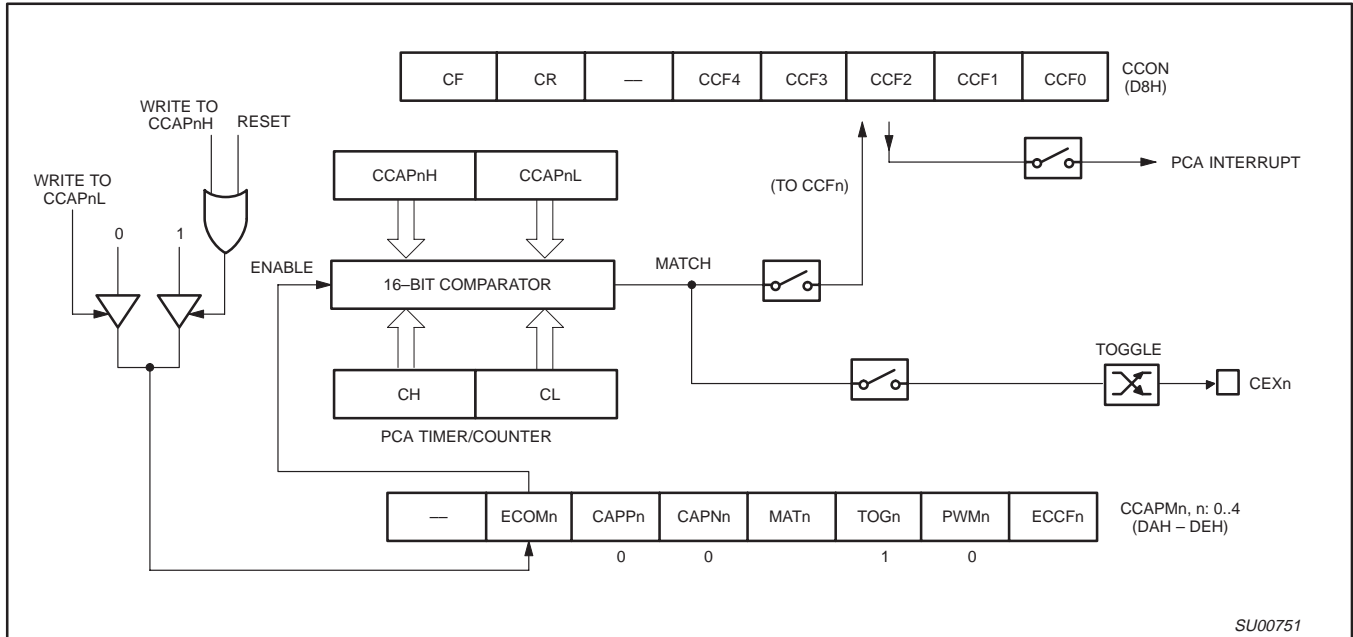


Figure 11. PCA High Speed Output Mode

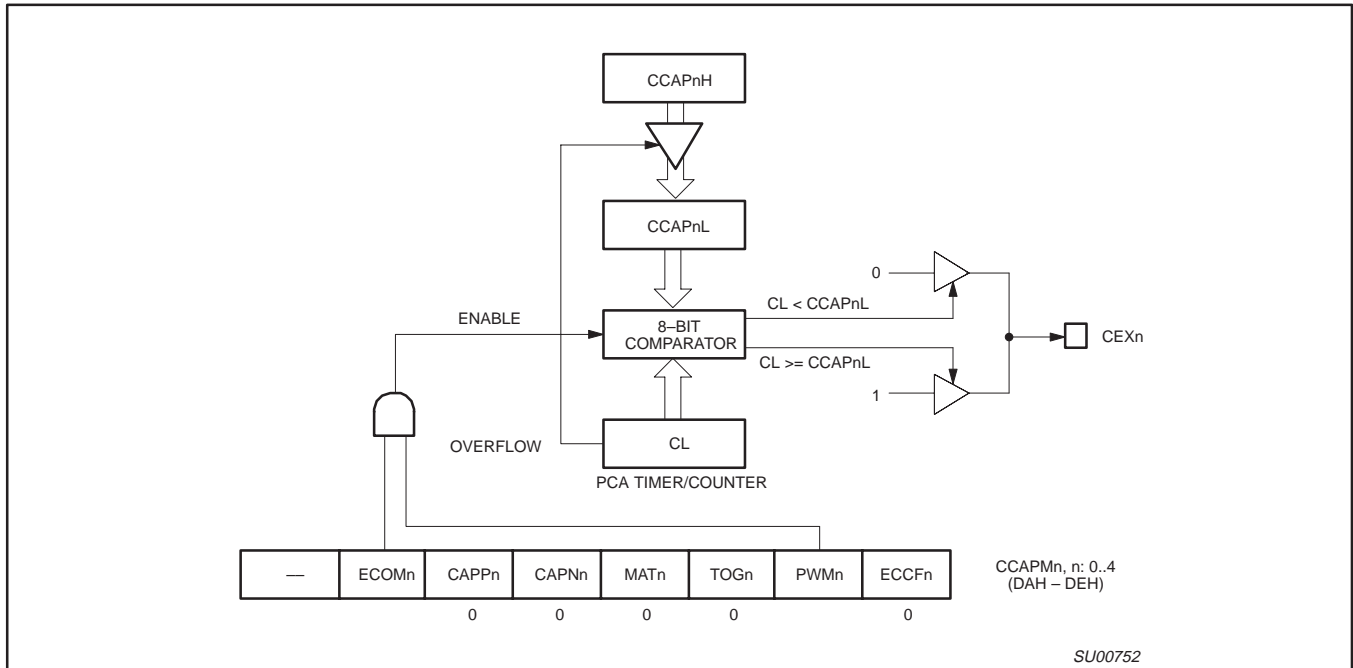


Figure 12. PCA PWM Mode

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

WATCHDOG TIMER

The watchdog timer is not directly loadable by the user. Instead, the value to be loaded into the main timer is held in an autoload register or is part of the mask ROM programming. In order to cause the main timer to be loaded with the appropriate value, a special sequence of software action must take place. This operation is referred to as feeding the watchdog timer.

To feed the watchdog, two instructions must be sequentially executed successfully. No intervening instruction fetches are allowed, so interrupts should be disabled before feeding the watchdog. The instructions should move A5H to the WFEED1 register and then 5AH to the WFEED2 register. If WFEED1 is correctly loaded and WFEED2 is not correctly loaded, then an immediate underflow will occur.

The watchdog timer subsystem has two modes of operation. Its principal function is a watchdog timer. In this mode it protects the system from incorrect code execution by causing a system reset when the watchdog timer underflows as a result of a failure of software to feed the timer prior to the timer reaching its terminal count. If the user does not employ the watchdog function, the watchdog subsystem can be used as a timer. In this mode, reaching the terminal count sets a flag. In most other respects, the timer mode possesses the characteristics of the watchdog mode. This is done to protect the integrity of the watchdog function.

The watchdog timer subsystem consists of a prescaler and a main counter. The prescaler has 8 selectable taps off the final stages and the output of a selected tap provides the clock to the main counter. The main counter is the section that is loaded as a result of the software feeding the watchdog and it is the section that causes the system reset (watchdog mode) or time-out flag to be set (timer mode) if allowed to reach its terminal count.

Programming the Watchdog Timer

Both the EPROM and ROM devices have a set of SFRs for holding the watchdog autoload values and the control bits. The watchdog time-out flag is present in the PCON register and operates the same in all versions. In the EPROM device, the watchdog parameters (autoload value and control) are always taken from the SFRs. In the ROM device, the watchdog parameters can be mask programmed or taken from the SFRs. The selection to take the watchdog parameters from the SFRs or from the mask programmed values is controlled by EA (external access). When EA is high (internal ROM access), the watchdog parameters are taken from the mask programmed values. If the watchdog is mask programmed to the timer mode, then the autoload values and the pre-scaler taps are taken from the SFRs. When EA is low (external access), the watchdog parameters are taken from the SFRs. The user should be able to leave code in his program which initializes the watchdog SFRs even though he has migrated to the mask ROM part. This allows no code changes from EPROM prototyping to ROM coded production parts. The run control bit only functions in timer mode and does not require a feed sequence to modify.

Watchdog Detailed Operation

EPROM Device (and ROMless Operation: EA = 0)

In the ROMless operation (ROM part, EA = 0) and in the EPROM device, the watchdog operates in the following manner (see Figure 15).

Whether the watchdog is in the watchdog or timer mode, when external RESET is applied, the following takes place:

- Watchdog mode bit set to watchdog mode.
- Watchdog is running.
- Autoload register set to 00 (min. count).
- Watchdog time-out flag is unchanged.
- Prescaler is cleared.
- Prescaler tap set to the highest divide.
- Autoload takes place.

The watchdog can be fed even though it is in the timer mode.

Note that the operational concept is for the watchdog mode of operation, when coming out of a hardware reset, the software should load the autoload registers, set the mode to watchdog, clear the watchdog timeout flag, and then feed the watchdog (cause an autoload). The watchdog will now be starting at a known point.

If the watchdog is in the watchdog mode and running and happens to underflow at the time the external RESET is applied, the watchdog time-out flag will be set.

When the watchdog is in the watchdog mode and the watchdog underflows, the following action takes place (see Figure 17):

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.
- All other device action same as external reset.

Note that if the watchdog underflows, the program counter will start from 00H as in the case of an external reset. The watchdog time-out flag can be examined to determine if the watchdog has caused the reset condition. The watchdog time-out flag bit must be cleared by software.

When the watchdog is in the timer mode and the timer software underflows, the following action takes place:

- Autoload takes place.
- Watchdog time-out flag is set
- Mode bit unchanged.
- Watchdog run bit unchanged.
- Autoload register unchanged.
- Prescaler tap unchanged.

Mask ROM Device (EA = 1)

In the mask ROM device, the watchdog mode bit (WDMOD) is mask programmed and the bit in the watchdog command register is read only and reflects the mask programmed selection. If the mask programmed mode bit selects the timer mode, then the watchdog run bit (WDRUN) operates as described under EPROM Device. If the mask programmed bit selects the watchdog mode, then the watchdog run bit has no effect on the timer operation (see Figure 16).

Watchdog Function

The watchdog consists of a programmable prescaler and the main timer. The prescaler derives its clock from the on-chip oscillator. The prescaler consists of a divide by 2 followed by a 13 stage upcounter with taps from stage 6 through stage 13. This is shown in Figure 18.

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

The tap selection is programmable. The watchdog main counter is a down counter clocked (decremented) each time the programmable prescaler overflows. The watchdog generates an underflow signal (and is autoloading) when the watchdog is at count 0 and the prescaler clock decrements the watchdog. The watchdog is 8 bits long and the autoloading value can range from 0 to FFH. (The autoloading value of 0 is permissible since the prescaler is cleared upon autoloading).

This leads to the following user design equations. Definitions: t_{OSC} is the oscillator period, N is the selected prescaler tap value, W is the main counter autoloading value, t_{MIN} is the minimum watchdog time-out value (when the autoloading value is 0), t_{MAX} is the maximum time-out value (when the autoloading value is FFH), t_D is the design time-out value.

$$t_{MIN} = t_{OSC} \times 2 \times 64$$

$$t_{MAX} = t_{MIN} \times 128 \times 256$$

$$t_D = t_{MIN} \times 2^{PRESCALER} \times (W + 1)$$

(where prescaler = 0, 1, 2, 3, 4, 5, 6, or 7)

Note that the design procedure is anticipated to be as follows. A t_{MAX} will be chosen either from equipment or operation considerations and will most likely be the next convenient value higher than t_D . (If the watchdog were inadvertently to start from 00H, an underflow would be guaranteed, barring other anomalies, to occur within t_{MAX}).

The software must be written so that a feed operation takes place every t_D seconds from the last feed operation. Some tradeoffs may need to be made. It is not advisable to include feed operations in minor loops or in subroutines unless the feed operation is a specific subroutine.

Watchdog Control Register (WDCON)

Address C4H

The following bits of this register are read only in the ROM part when \overline{EA} is high: WDMOD, DPD, OFRE, LVRE, PRE0, PRE1, and PRE2. That is, the register will reflect the mask programmed values. In the ROM part with \overline{EA} high, these bits are taken from mask coded bits and are not readable by the program. WDRUN is read only in the ROM part when \overline{EA} is high and WDMOD is in the watchdog mode. When WDMOD is in the timer mode, WDRUN functions normally.

The parameters written into WDMOD, DPD, OFRE, LVRE, PRE0, PRE1, and PRE2 by the program are not applied directly to the watchdog timer subsystem. The watchdog timer subsystem is directly controlled by a second register which stores these bits. The transfer of these bits from the user register to the second control register takes place when the watchdog is fed. This prevents random code execution from directly foiling the watchdog function. This does not affect the operation where these bits are taken from mask coded values.

The reset values of the WDCON and WDL registers will be such that the timer resets to the watchdog mode with a timeout period of $2 \times 64 \times 128 \times t_{OSC}$. The watchdog timer does not generate an interrupt.

Additional bits in WDCON are used to disable reset generation by the oscillator fail and low voltage detect circuits. WDCON can be written by software only by executing a valid watchdog feed sequence.

WDCON Register Bit Definitions

WDCON.7	PRE2	Prescaler Select 2, reset to 1
WDCON.6	PRE1	Prescaler Select 1, reset to 1
WDCON.5	PRE0	Prescaler Select 0, reset to 1
WDCON.4	LVRE	Low Voltage Reset Enable, reset to 1 (enabled)
WDCON.3	OFRE	Oscillator Fail Reset Enable, reset to 1 (enabled)
WDCON.2	DPD	Disable Power Down
WDCON.1	WDRUN	Watchdog Run, reset to 1 (enabled)
WDCON.0	WDMOD	Watchdog Mode, reset to 1 (watchdog mode)

Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 8XC576 UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 20). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 19.

The serial port transmitter data can be inverted by setting the TXI (AUXR.2) bit. For normal operation, the TXI bit should be cleared.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 21.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

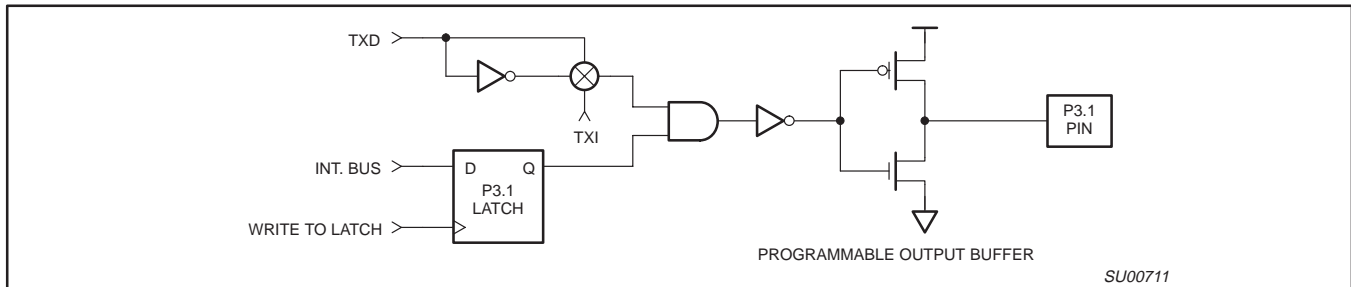


Figure 13. TXI (AUXR.2) Bit Inverts the TxD Pin (P3.1) When Set

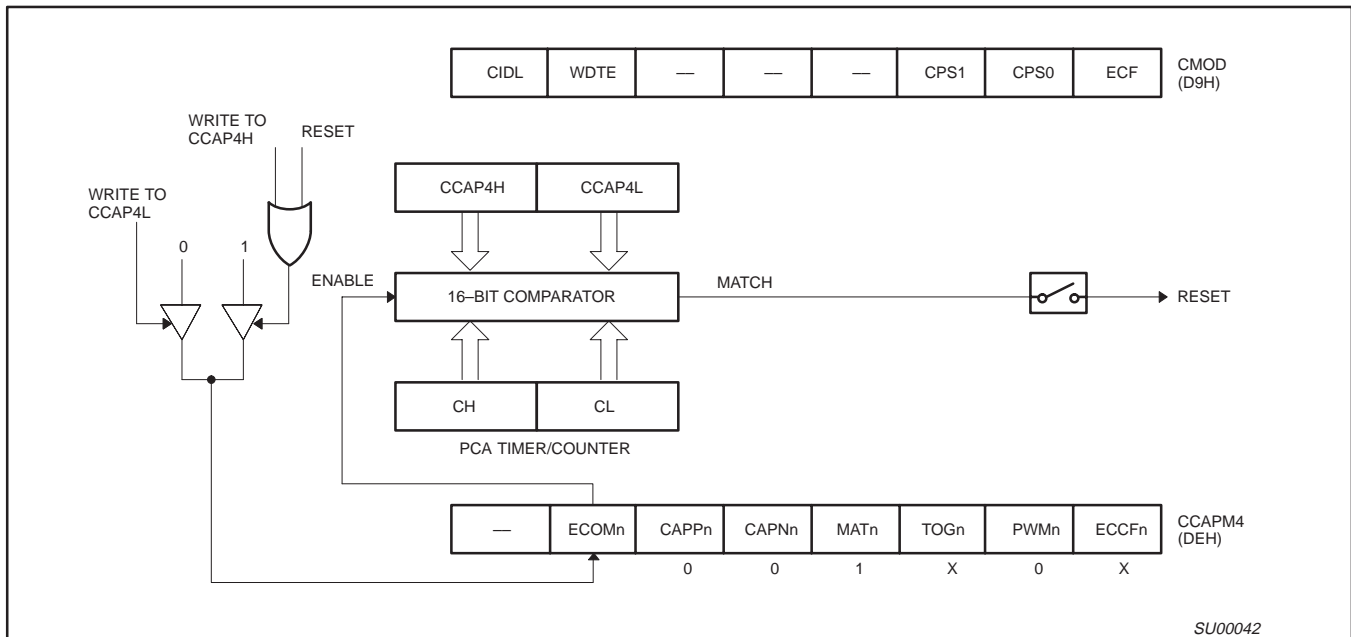


Figure 14. PCA Watchdog Timer

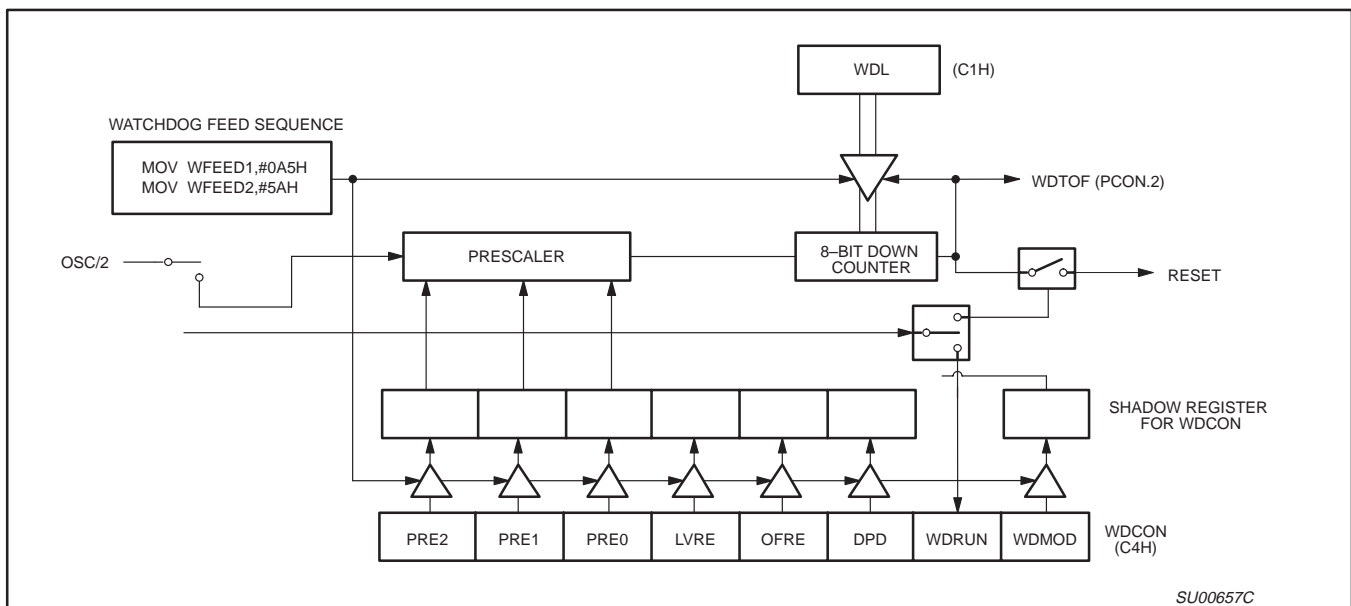


Figure 15. Watchdog Timer in 87C576 and 80C576 / 83C576 (EA = 0)

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 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

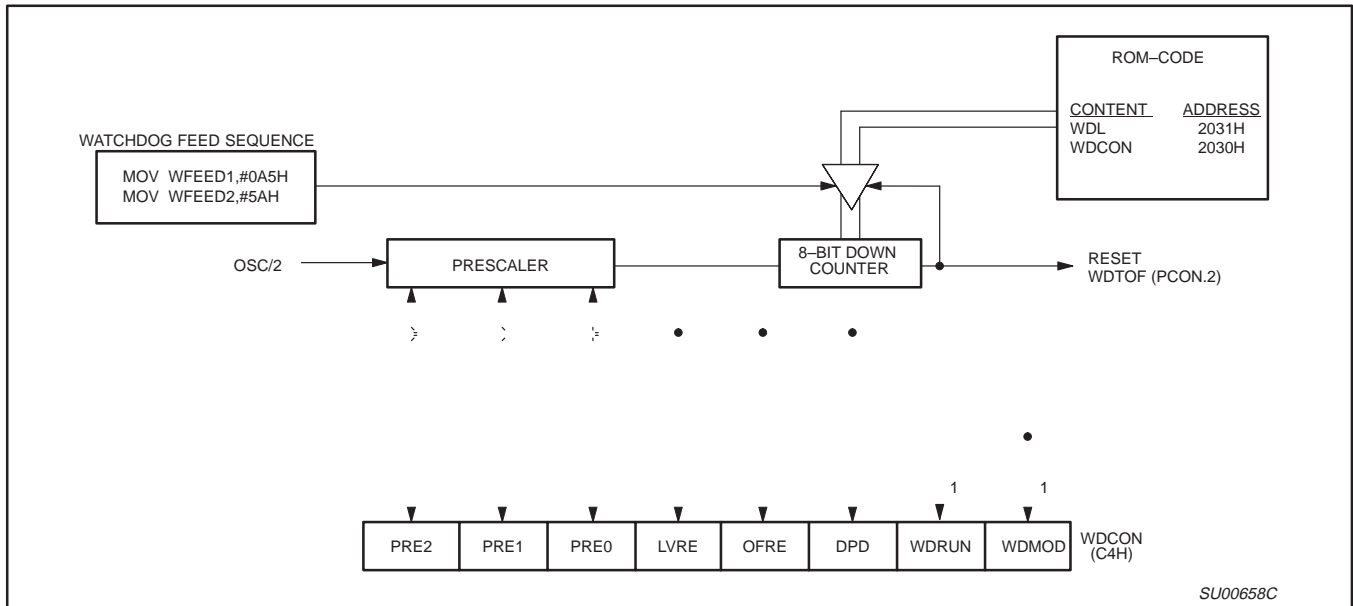


Figure 16. Watchdog Timer of 83C576 in Watchdog Mode ($\overline{EA} = 1$, WDMOD = 1)

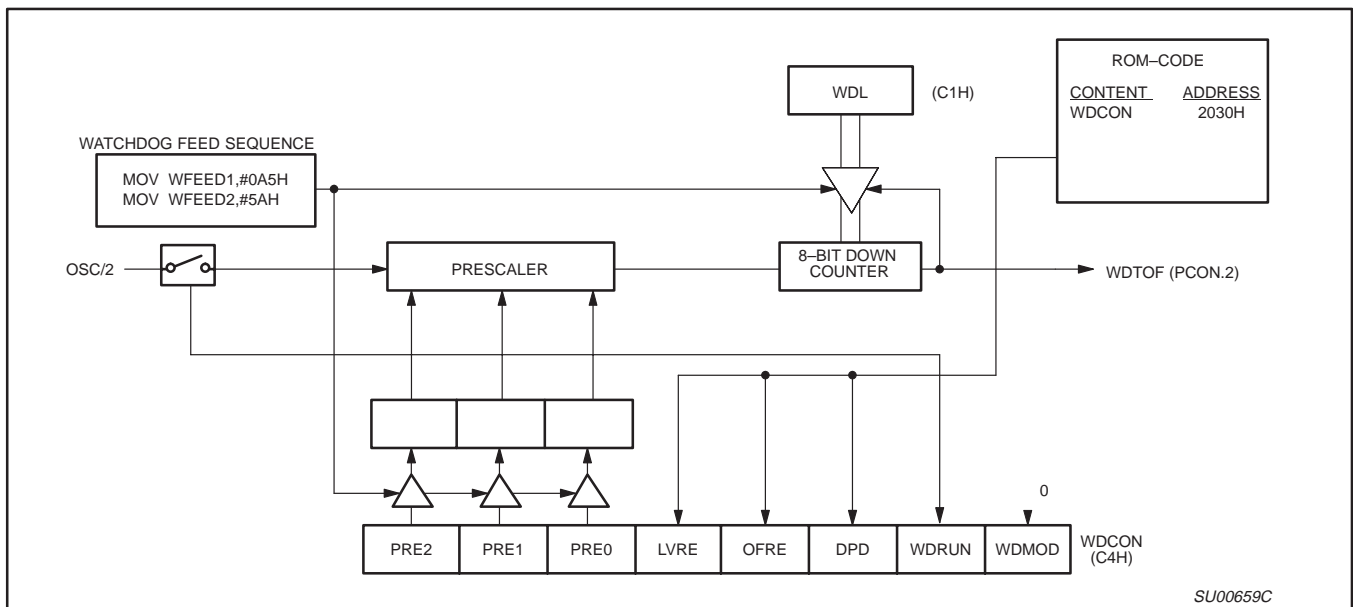


Figure 17. Watchdog Timer of 83C576 in Timer Mode ($\overline{EA} = 1$, WDMOD = 0)

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 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

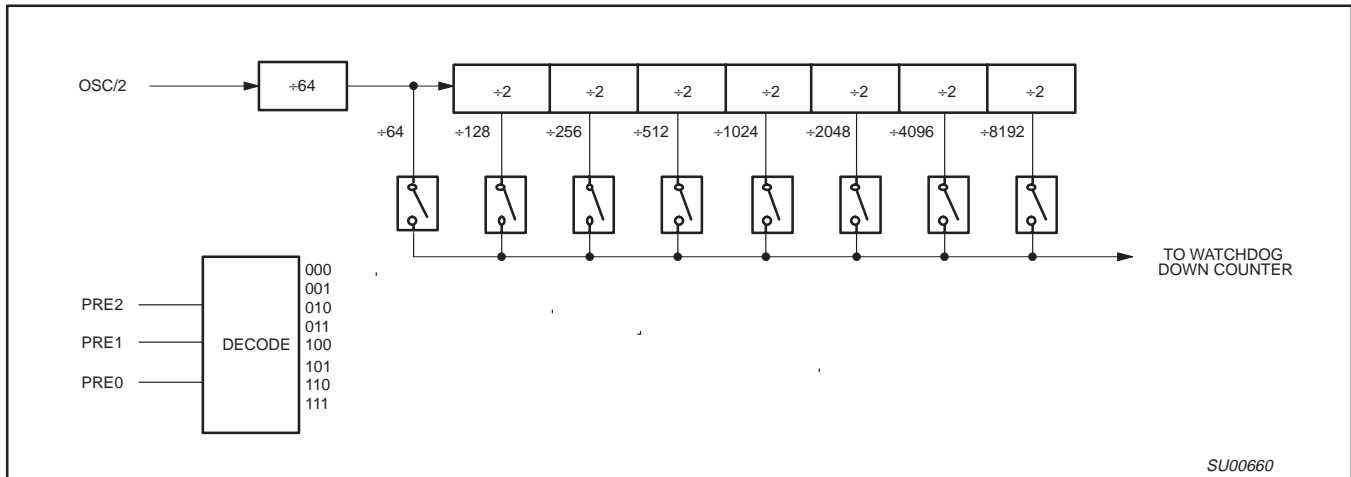


Figure 18. Watchdog Prescaler

SCON Address = 98H Reset Value = 0000 000B

Bit Addressable

	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
Bit:	7	6	5	4	3	2	1	0

(SMOD0/1)*

Symbol	Function			
FE	Framing Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit.			
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)			
SM1	Serial Port Mode Bit 1			
SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$f_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$
1	1	3	9-bit UART	variable
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.			
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.			
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.			
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.			
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.			
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.			

NOTE:
 *SMOD0/1 is located at PCON.6, PCON.7
 ** f_{OSC} = oscillator frequency

Figure 19. SCON: Serial Port Control Register

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

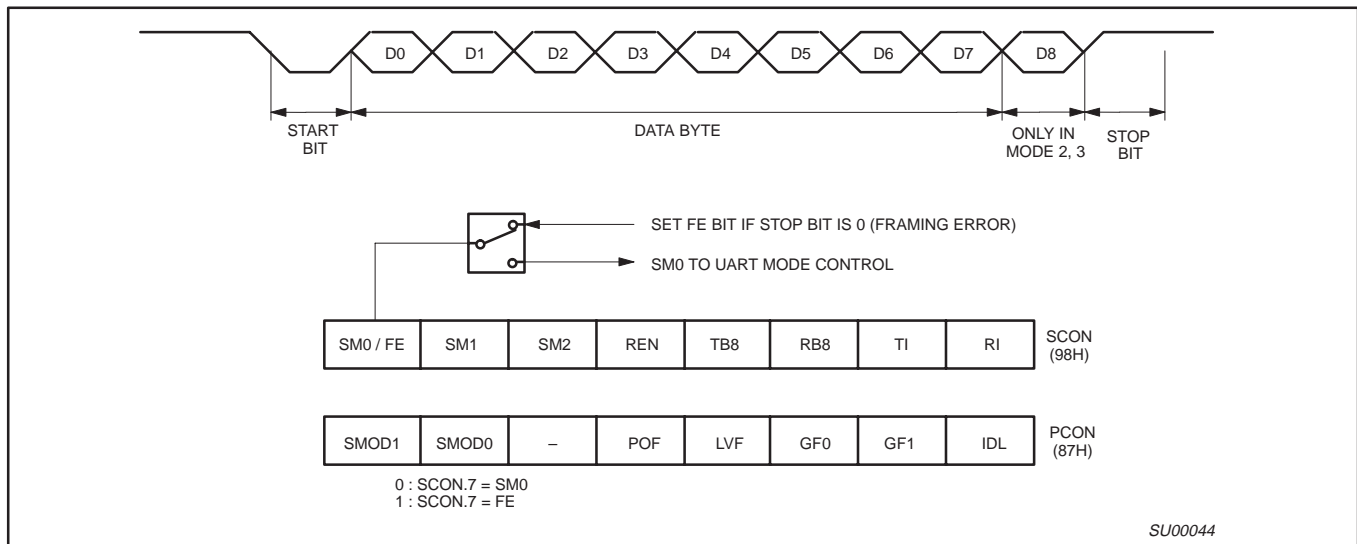


Figure 20. UART Framing Error Detection

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1101</u>
	Given =	1100 00X0
Slave 1	SADDR =	1100 0000
	SADEN =	<u>1111 1110</u>
	Given =	1100 00XX

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0	SADDR =	1100 0000
	SADEN =	<u>1111 1001</u>
	Given =	1100 0XX0

Slave 1	SADDR =	1110 0000
	SADEN =	<u>1111 1010</u>
	Given =	1110 0X0X
Slave 2	SADDR =	1110 0000
	SADEN =	<u>1111 1100</u>
	Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

Analog Comparators

Four analog comparators are provided on chip. Three comparators have a common negative reference CMPR- and independent positive inputs CMP1+, CMP2+, CMP3+ on port 3. The fourth comparator has independent positive and negative inputs CMP0+ and CMP0- on port 2. The CMP register contains an output and enable bit for each comparator. Figure 22 shows the connection of the comparators.

When the comparator is enabled, the port should be configured by the user as high impedance.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

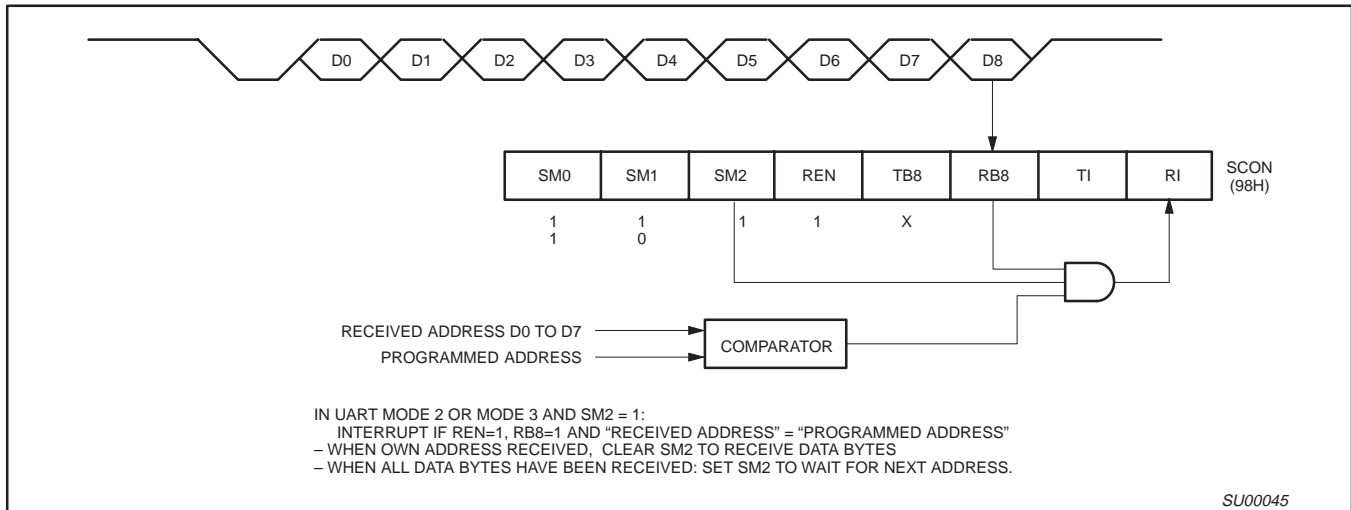


Figure 21. UART Multiprocessor Communication, Automatic Address Recognition

CMP Register Bit Definitions

- CMP.7 enable comparator 3
- CMP.6 enable comparator 2
- CMP.5 enable comparator 1,
- CMP.4 enable comparator 0
- CMP.3 comparator 3 output (read only)
- CMP.2 comparator 2 output (read only)
- CMP.1 comparator 1 output (read only)
- CMP.0 comparator 0 output (read only)

All comparators are disabled automatically in power down mode. In idle mode unused comparators should be disabled by software to save power. A comparator can generate an interrupt that will terminate idle mode when used to drive a PCA capture input.

The CMPE register contains bits to enable each comparator to drive external output pins or internal PCA capture inputs. When the comparator is configured for external output, the user must also configure the output port in one of its output modes. The comparator output is wire-ORed with the corresponding port SFR bit, so the SFR bit must also be set by software to enable the output.

CMPE Register Bit Definitions

- CMPE.7 enables comparator 3 to drive CEX3
- CMPE.6 enables comparator 2 to drive CEX2
- CMPE.5 enables comparator 1 to drive CEX1
- CMPE.4 enables comparator 0 to drive CEX0
- CMPE.3 enables comparator 3 output on P2.3
- CMPE.2 enables comparator 2 output on P2.2
- CMPE.1 enables comparator 1 output on P2.1
- CMPE.0 enables comparator 0 output on P2.0

When 1s are written to CMPE bits 7-4, the comparator outputs will drive the corresponding capture input. When 1s are written to CMPE bits 3-0 the comparator output will also drive the corresponding port 2 pin. If the comparator's enabled to drive the capture input but not the port pin, then the port pin can be used for general purpose I/O. When a comparator output is enabled, the user will need to configure the port for one of its output modes.

There are two special function registers associated with the comparators. They are CMP which contains the comparator enables

and a bit that can be read by software to determine the state of each comparator's output, and CMPE which controls whether the output from each comparator drives the associated output pin or a capture input associated with one of the PCA modules.

The CMP registers bits 0-3 can be read by software to determine the state of the output of each comparator. To do this the associated comparator must be enabled but the output in port 2 can be disabled. This allows easy polling of the comparator output value without the need to use up a port pin.

The CMPE register allows the comparator to drive the associated PCA module capture input, so that on compare a capture can be generated in the PCA. Bits 0-3 of this register enable the comparator output to drive the associated port 2 output circuitry. Used as a comparator output, the output mode for this port must be configured for output by the user and the port output SFR bit latch must be set. If the comparator is not enabled to drive the port 2 circuitry, the associated port 2 pin can be used for other I/O. This includes when a comparator is enabled to drive the capture input to a PCA module.

Reduced EMI Mode

There are two bits in the AUXR register that can be set to reduce the internal clock drive and disable the ALE output. AO (AUXR.0) when set turns off the ALE output. LO (AUXR.1) when set reduces the drive of the internal clock circuitry. Both bits are cleared on Reset. With LO set the 8XC576 will still operate at 12MHz, and will have reduced EMI in the range above 100MHz.

8XC576 Reduced EMI Mode

AUXR (0X8E)

—	—	—	—	RST	TXI	LO	AO
---	---	---	---	-----	-----	----	----

- AO: Turns off ALE output.
- LO: Reduces drive of internal clock circuitry. 8XC576 spec'd to 12MHz when LO set.
- TXI: Inverts TxD when set.
- RST: Software reset.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

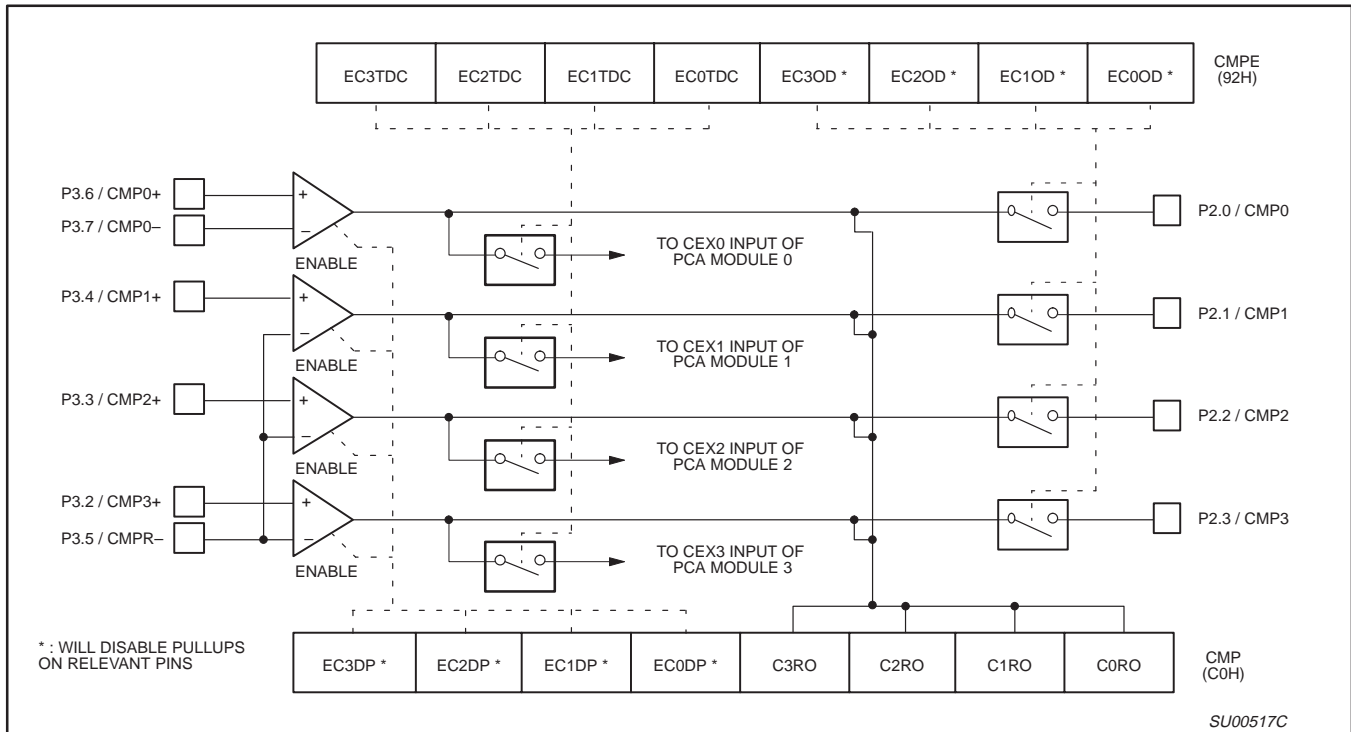


Figure 22. Analog Comparators

INTERNAL RESET

Internal resets (see Figure 1) generated by the power on, low voltage, software (SRST), watchdog and oscillator fail detect circuits are self timed to guarantee proper initialization of the 8XC576. Reset will be held approximately 24 oscillator periods after normal conditions are detected by all enabled detect circuits. Internal resets do not drive RST but will cause missing pulses on ALE.

Analog to Digital Converter

The 8XC576 has a 6 channel 10 bit successive approximation A/D converter with separate result registers for each channel. Operating modes are provided for single or multiple channel conversions and multiple conversions of a single channel without software intervention. The ADC can also be operated in 8 bit mode with faster conversion times. Registers ADC0H–ADC5H contain the MSBs and ADC0L–ADC5L bits 6 and 7 contain the 2 LSBs of the conversion result for each channel. The ADCS register determines which channels are converted in multiple channel modes. If the ADCS bit corresponding to a channel is set, that channel is converted, else if the bit is clear the channel is skipped.

A/D Channel Select (ADCS) Register (Reset Value = 00H)

- ADCS5 ADCS.5 – A/D channel 5 select bit
- ADCS4 ADCS.4 – A/D channel 4 select bit
- ADCS3 ADCS.3 – A/D channel 3 select bit
- ADCS2 ADCS.2 – A/D channel 2 select bit
- ADCS1 ADCS.1 – A/D channel 1 select bit
- ADCS0 ADCS.0 – A/D channel 0 select bit

A/D Control (ADCON) Register (Reset Value = 00H)

- ADF ADCON.7 – A/D conversion complete flag
- ADCE ADCON.6 – A/D conversion enable
- AD8M ADCON.5 – A/D 8-bit mode

- AMOD1 ADCON.4 – A/D mode select bit 1
- AMOD0 ADCON.3 – A/D mode select bit 0
- ASCA2 ADCON.2 – A/D channel address bit 2
- ASCA1 ADCON.1 – A/D channel address bit 1
- ASCA0 ADCON.0 – A/D channel address bit 0

AMOD1 AMOD0

0	0	Single Conversion Mode – channel selected by bits ASCA2..0 in ADCON is converted, the result placed in the associated result registers; ADF is set on completion.
0	1	Multiple Channel Scan Mode – all channels selected in the ADCS register are converted starting with the channel addressed by bits ASCA2..0 in ADCON, conversion results are placed in the corresponding result registers for each channel. ADF is set when the last conversion is completed.
1	0	Single Channel Multiple Conversion – channel selected by bits ASCA2..0 in ADCON is converted 6 times and all 6 results are saved in ADC0H–ADC5H and ADC0L–ADC5L, ADF is set when all conversions are complete.
1	1	Multiple Channel Continuous – same as Multiple Channel Scan mode but repeats as long as ADCE=1, ADF is set when all channels have been converted once. Hardware will prevent the ADC from writing to the result registers while they are being read.

Flag ADF is set upon completion of a conversion, if the ADC interrupt enable bit EAD is set, the program will vector to the ADC interrupt location when ADF is set.

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

PWMs

The pulse width modulator system of the 8XC576 contains two PWM output channels. These channels generate pulses of programmable length and interval. The prescaler and counter are common to both PWM channels.

The prescaler is loaded with the complement of the PWMP register during counter overflow, internal reset, and when EN/CLR# = 0. The repetition frequency is defined by the 8-bit prescaler which clocks the counter. The prescaler division factor = PWMP+1. Reading the PWMP gives the current reload value. The actual count of the prescaler cannot be read.

The 8-bit counter counts from 0–254 inclusive. The value of the counter is compared to the contents of the compare registers PWM0 and PWM1. When the counter compares to the compare register, that register's output goes LOW. When the counter reaches zero the output is set HIGH unless PWMn = 00H. The duty cycle of each channel is defined by the contents of its compare register and is in the range of 0 to 1, programmed in increments of 1/255.

The outputs can be set continuously low by loading PWMn with 00H and continuously high by loading with FFH.

The PWM counter is enabled with bit EN/CLR# of the PWCON register. Output to the port pin is separately enabled by setting the PWEn bits in the PWCON register. The counter remains active if EN/CLR# is set even if both PWEn bits are reset. The PWM function is reset by a chip reset. In idle mode, the PWM will function as configured by PWCON. In power-down the state of the PWM will freeze when the internal clock stops. If the chip is awakened with an external interrupt, the PWM will continue to function from its state when power-down was entered. The EN/CLR# bit of PWCON will clear the counter and load the contents of the PWMP into the prescaler when set LOW. If PWEn is set at this time the output will go HIGH unless PWMn is 00H.

The repetition frequency is given by:

$$f_{\text{PWM}} = \frac{f_{\text{osc}}}{(510 \times (1 + \text{PWMP}))}$$

An oscillator frequency of 12MHz results in a repetition range of 92Hz to 23.5KHz.

The high/low ratio of PWMn is PWMn/(255–PWMn) for PWMn values except 255. A PWMn value of 255 results in a high PWMn output.

In order for the PWMn output to be used as a standard I/O pin, PWMn must be reset. The PWM counter can still be used as an internal timer by setting EN/CLR#.

Pulse Width Modulator Control Register Bit Definitions (PWCON = BCH)

PWMP	PWCON.3	Counter overflow flag, must be cleared by software
EN/CLR	PWCON.2	Counter enable and counter/prescaler reset when Low
PWE1	PWCON.1	PWM1 output to P2.7 pin enable
PWE0	PWCON.0	PWM0 output to P2.6 pin enable

Auxiliary Register Bit Definitions (AUXR = 8EH)

RST	AUXR.3	Software reset bit
TXI	AUXR.2	SIO TxD invert
LO	AUXR.1	Low Speed, reduces internal clock drive
AO	AUXR.0	ALE Off, when set turns off ALE

Interrupt Enable 0 (IE0) Register

EA	IE0.7	Enable all interrupts
EC	IE0.6	Enable PCA interrupt
ET2	IE0.5	Enable Timer 2 interrupt
ES	IE0.4	Enable Serial I/O interrupt
ET1	IE0.3	Enable Timer 1 interrupt
EX1	IE0.2	Enable External interrupt 1
ET0	IE0.1	Enable Timer 0 interrupt
EX0	IE0.0	Enable External interrupt 0

Interrupt Enable 1 (IE1) Register

EOB	IE1.7	Enable OBE interrupt
EIB	IE1.6	Enable IBF interrupt
EAD	IE1.5	Enable ADC interrupt
EC4	IE1.4	Enable PCA module 4 interrupt
EC3	IE1.3	Enable PCA module 3 interrupt
EC2	IE1.2	Enable PCA module 2 interrupt
EC1	IE1.1	Enable PCA module 1 interrupt
EC0	IE1.0	Enable PCA module 0 interrupt

Interrupt Priority 0 (IP0) Register

	IP0.7	(reserved)
PPC	IP0.6	PCA interrupt priority
PT2	IP0.5	Timer 2 interrupt priority
PS	IP0.4	Serial I/O interrupt priority
PT1	IP0.3	Timer 1 interrupt priority
PX1	IP0.2	External interrupt 1 priority
PT0	IP0.1	Timer 0 interrupt priority
PX0	IP0.0	External interrupt 0 priority

Interrupt Priority 1 (IP1) Register

POB	IP1.7	OBE interrupt priority
PIB	IP1.6	IBF interrupt priority
PAD	IP1.5	ADC interrupt priority
PC4	IP1.4	PCA module 4 interrupt priority
PC3	IP1.3	PCA module 3 interrupt priority
PC2	IP1.2	PCA module 2 interrupt priority
PC1	IP1.1	PCA module 1 interrupt priority
PC0	IP1.0	PCA module 0 interrupt priority

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

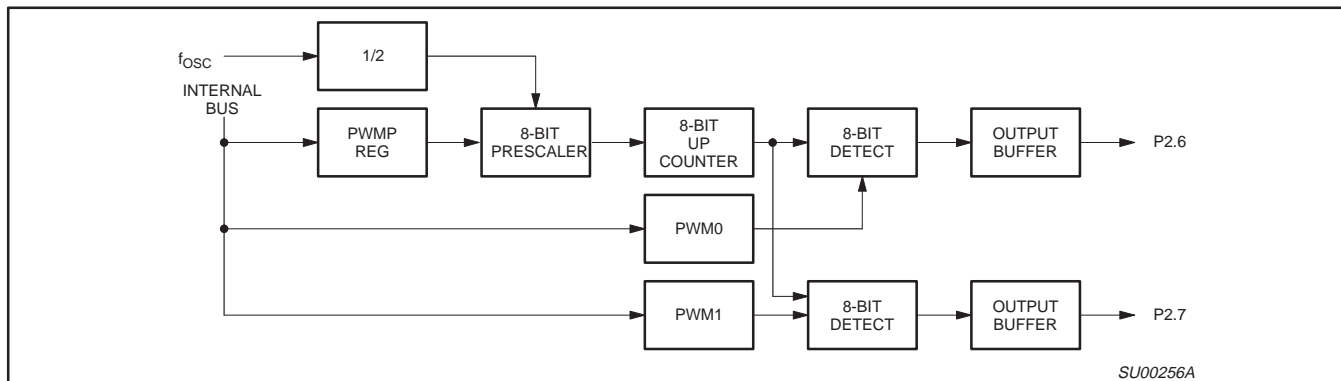


Figure 23. Block Diagram of PWMs

PCA Interrupt System

The PCA on most 80C51 family devices provides a single interrupt source, EC (IE.6). The 8xC576 expands the flexibility of the PCA by providing additional interrupt sources for each of the five PCA modules, EC0 (IE1.0) through EC4 (IE1.4), in addition to the original interrupt source EC (IE.6). Any of these sources can be enabled at any time. It is possible for both a module source (EC0 through EC4) to be enabled at the same time that the single source, EC, is enabled. In this case, a module event will generate an interrupt for both the module source and the single source, EC.

Priority	Source	Flag	Vector	
1	INT0	IE0	03H	highest priority
2	ADC	ADF	3BH	
3	TIMER 0	TF0	0BH	
4	INT1	IE1	13H	
5	TIMER 1	TF1	1BH	
6	SERIAL	RI, TI	23H	
7	PCA0	CC0	43H	
8	PCA1	CC1	4BH	
9	PCA2	CC2	53H	
10	PCA3	CC3	5BH	
11	PCA4	CC4	63H	
12	PCA	ECF	33H	
13	TIMER 2	TF2/EXF2	2BH	
14	UPI	IBF	6BH	
15	UPI	OBE	73H	lowest priority

Power Control (PCON) Register

SMOD1	PCON.7	double baud rate bit
SMOD0	PCON.6	SCON.7 access control
OSF	PCON.5	oscillator fail flag
POF	PCON.4	power off flag
LVF	PCON.3	low voltage flag
WDT0F	PCON.2	watchdog timeout flag
PD	PCON.1	power down mode bit
IDL	PCON.0	idle mode bit

UNIVERSAL PERIPHERAL INTERFACE

UPI mode allows the 8XC576 to function as a slave processor connected to a host CPU bus via port 0. The interface consists of port 0 input and output buffer registers and the UPI control/status register (UCS). UPI mode is enabled by setting the UPI enable bit (UE) in the UCS. When operating in UPI mode, port 0 pins should be programmed to High-Z (P0M1=1 and P0M2=0) by user firmware. Access to port 0 is controlled by inputs \overline{WR} , \overline{RD} , \overline{CS} , and A0. \overline{RD} and \overline{WR} are the external read and write strobes controlled by the host CPU. \overline{CS} is the chip select input, normally a decoded address

from the host CPU bus, which qualifies \overline{RD} and \overline{WR} (these pins have no effect when $\overline{CS}=1$). The A0 pin is an address input from the host CPU which selects either the port 0 output buffer or the UCS register to be output during a read operation. During a write operation, the value of the A0 pin is latched in the AF flag in the UCS register. The following is a summary of the UPI data control inputs:

\overline{CS}	\overline{RD}	\overline{WR}	A0	
0	0	1	0	read port 0 output buffer, clear OBF/set OBE
0	0	1	1	read UPI control/ status register
0	1	0	0	write data to input buffer set IBF, clear AF
0	1	0	1	write command to input buffer set IBF, AF
1	x	x	x	disable input/output

UPI Control Status Register (UCS, Reset value = 00H)

UCS.7	ST7	User defined status bit
UCS.6	ST6	User defined status bit
UCS.5	ST5	User defined status bit
UCS.4	ST4	User defined status bit
UCS.3	UE	UPI Enable bit – if UE=1, UPI is enabled (read only AF, IBF, and OBE/OBF), if UE=0, UPI is disabled and port 0 functions normally.
UCS.2	AF	Address Flag – contains status of the A0 (address) pin during the last write. If A0=0, the input buffer should be interpreted as data by the 8XC576 software, if A0=1, the input buffer should be interpreted as a command.
USC.1	IBF	Input Buffer Full flag – set by hardware on trailing (rising) edge of \overline{WR} when $\overline{CS}=0$, cleared by hardware when port 0 SFR is read (by the 8XC576 software).
USC.0	OBE/OBF	Output Buffer Full flag – set by hardware during writes (by 8XC576 software) to the port 0 SFR, set/cleared by hardware on the trailing (rising) edge of \overline{RD} when $\overline{CS}=0$ and A0=0.

NOTE: This bit is defined as OBE (1=empty) when read by the MCU, and, as OBF (—full) when read by the external host.

The IBF and OBF flag bits reflect the status of the input/output buffers. The host CPU writes to the 8XC576 by driving data on the external bus connected to port 0 and strobing the \overline{WR} pin while $\overline{CS}=0$. The \overline{WR} strobe latches port 0 data in the input buffer and sets the IBF flag on the trailing (rising) edge. When the 8XC576 reads from port 0 in UPI mode, it reads from the input buffer and

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

clears the IBF. When the 8XC576 writes to port 0 in UPI mode, it writes to the output buffer which sets the OBF and clears the OBE flag. The host CPU can read the output buffer or the UCS register enabling the port 0 drivers, the OBF flag is cleared and the OBE flag is set when the output buffer is read.

When the UPI is enabled, the AF, IBF, and OBE/OBF flags are read-only, and thus can only be modified by specific hardware events.

The UPI runs in idle mode. It can interrupt the part out of Idle mode for all UPI write and data read operations. It will not interrupt out of idle mode for a UCS register read operation.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol, page 4.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the

idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset. Also see UPI section.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. The control bits for the reduced power modes are in the special function register PCON. Power-down mode can be terminated with either a hardware reset or external interrupt. With an external interrupt INT0 or INT1 must be enabled and configured as level sensitive. Holding the pin low restarts to oscillator and bringing the pin back high completes the exit.

Power-down mode can be disabled by the DPD bit in the WDCON register. Reset and waking up from power-down will also enable the DPD bit, therefore, the DPD bit must be cleared again before the power-down mode.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} must come up with \overline{RST} low for a proper start-up.

Table 2 shows the state of I/O ports during low current operating modes.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

ABSOLUTE MAXIMUM RATINGS^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Voltage on \overline{EA}/V_{PP} pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	-0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C, } -40^{\circ}\text{C to } +85^{\circ}\text{C, and } -40^{\circ}\text{C to } +125^{\circ}\text{C; } V_{CC} = 5\text{V} \pm 10\%, V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
V_{IL}	Input low voltage (except Port 1, \overline{EA})		-0.5		$0.2V_{CC}-0.1$	V
V_{IL1}	Input low voltage (\overline{EA})		-0.5		$0.2V_{CC}-0.45$	V
V_{IL2}	Input low voltage (Port 1)		-0.5		$0.3V_{CC}$	V
V_{IH}	Input high voltage (except Port 1, XTAL1, RST)	$I_{IH} < 2\text{mA}$	$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage (XTAL1, RST, Port 1)	$I_{IH} < 2\text{mA}$	$0.7V_{CC}$		$V_{CC}+0.5$	V
HYS	Hysteresis voltage (Port 1)		200			mV
V_{OL}	Output voltage low (Ports 1, 2, 3)	$I_{OL} = 1.6\text{mA}$			0.45	V
V_{OL1}	Output voltage low (Ports 0, ALE, \overline{PSEN})	$I_{OL} = 3.2\text{mA}$			0.45	V
V_{OH}	Output voltage high (Ports 1, 2, 3 in push-pull mode)	$I_{OH} = -1.6\text{mA}$	$V_{CC}-1.0$			V
V_{OH1}	Output voltage high (Port 0, ALE, \overline{PSEN})	$I_{OH} = -3.2\text{mA}$	$V_{CC}-0.7$			V
V_{OH2}	Output voltage high in weak pullup mode (Port 0, 2, 3)	$I_{OH} = -10\mu\text{A}$	$V_{CC}-1.0$			V
V_{IO}	Offset voltage comparator inputs		-35		+35	mV
V_{CR}	Common mode range comparator inputs		0		V_{CC}	V
I_{IL}	Logical 0 input current (Ports 0, 2, 3) (weak pull-up)	$V_{IN} = 0.45\text{V}$			-250	μA
I_{IH}	Input pulldown current (Port 0, Port2 in open drain mode)	$0.45 < V_{IN} < V_{CC}$	2		40	μA
I_{L2}	Input leakage current (\overline{EA} , P0. 2. 3 High-Z)	$0.45 < V_{IN} < V_{CC}$	-10		+10	μA
I_{LA}	Input leakage current comparator/ADC inputs	$0 < V_{IN} < V_{CC}$	-1.0		+1.0	μA
I_{CC}	Power supply current: ⁷ Active mode @ 16MHz ⁵ Idle mode @ 16MHz Power-down mode	See note 6		20 8 5	30 12 75	 mA mA μA
R_{RST}	Internal reset pull-up resistor	$V_{IN} = 0\text{V}$	50		200	k Ω
V_{LOW}	Low V_{CC} detect voltage		3.75		4.25	V
C_{IO}	Pin capacitance ⁹	$f = 1\text{MHz}$			15	pF

NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and \overline{PSEN} to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is between V_{IH} and V_{IL} .
- I_{CCMAX} at other frequencies can be determined from Figure 33.
- See Figures 34 through 37 for I_{CC} test conditions.
- Load capacitance for port 0, ALE, and \overline{PSEN} = 100pF, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	10mA
Maximum I_{OL} per 8-bit port:	26mA
Maximum total I_{OL} for all outputs:	71mA

 If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- 20pF MAX for CERDIP package; 15pF MAX for all other packages.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

A/D CONVERTER DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C, } -40^{\circ}\text{C to } +85^{\circ}\text{C, and } -40^{\circ}\text{C to } +125^{\circ}\text{C; } V_{CC} = 5\text{V } \pm 10\%, V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
Static Characteristics					
R	Resolution	Monotonic with no missing codes	10		Bits
IL _e	Integral non-linearity error ^{2, 5, 8}			±2	LSB
DL _e	Differential non-linearity error ^{2, 3, 4, 7, 8}			±1	LSB
FS _e	Full Scale error ^{2, 8}			±3	LSB
OS _e	Offset error ^{2, 6, 8}			±2	LSB
Dynamic Characteristics					
t _{ADC}	Conversion time (including sampling time)			48t _{CY}	μs
t _{ADS}	Sampling time			8t _{CY}	μs
Analog Input Characteristics					
AV _{IN}	Analog input voltage		AV _{SS} - 0.2	AV _{DD} + 0.2	V
C _{IA}	Analog input capacitance			15	pF
M _{CTC}	Channel-to-channel matching ⁷			±1	LSB
C _t	Crosstalk between inputs of port 1 ⁷	0–100kHz		-60	dB
Power Requirements					
AV _{CC} /V _{REF+}	Analog supply and reference voltage	AV _{CC} = V _{CC} ± 0.2	4.0	6.0	V
AI _{CC}	Analog supply current: operating: (16MHz)	AV _{CC} = 6.0V		1.2	mA

NOTES:

- The following condition must not be exceeded: $V_{DD} - 0.2\text{V} < AV_{DD} < V_{DD} + 0.2\text{V}$.
- Conditions: AV_{SS} = 0V; AV_{CC} = 4.997V; V_{CC} = 5.0V.
- The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. (See Figure 24).
- The ADC is monotonic; there are no missing codes.
- The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 24).
- The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 24).
- Guaranteed by design.
- To meet Error Specification, analog input voltage must be less than 1V/ms.

$$\text{Slew Rate}_{\text{MAX}} = \frac{(AV_{CC}/1023) \times 1000}{4 \times (12/\text{Osc Freq (MHz)})} \quad (\text{V/ms})$$

For 16MHz @ 5.0V slew rate = 1.6V/ms.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

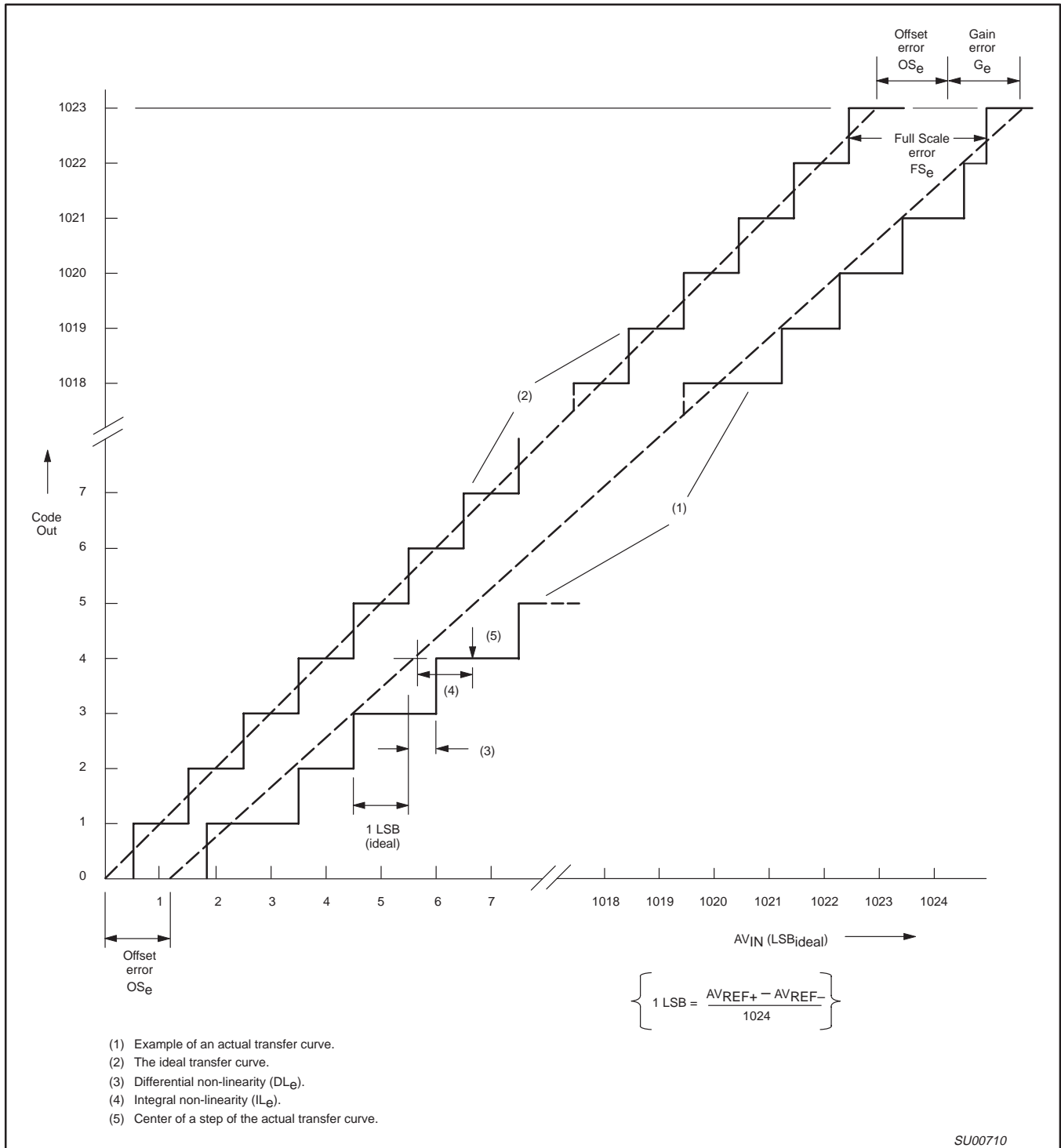


Figure 24. ADC Conversion Characteristic

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, -40°C to $+85^{\circ}\text{C}$, and -40°C to $+125^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}^{1, 2}$

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK		UNIT
			MIN	MAX	
$1/t_{CLCL}$	25	Oscillator frequency: Speed Version 8XC576 E	6	16	MHz
OSCF		Oscillator fail detect frequency	0.6	5.5	MHz
TR		Comparator response time		10	μs
t_{LHLL}	25	ALE pulse width	$2t_{CLCL}-40$		ns
t_{AVLL}	25	Address valid to ALE low	$t_{CLCL}-40$		ns
t_{LLAX}	25	Address hold after ALE low	$t_{CLCL}-30$		ns
t_{LLIV}	25	ALE low to valid instruction in		$4t_{CLCL}-100$	ns
t_{LLPL}	25	ALE low to $\overline{\text{PSEN}}$ low	$t_{CLCL}-30$		ns
t_{PLPH}	25	$\overline{\text{PSEN}}$ pulse width	$3t_{CLCL}-45$		ns
t_{PLIV}	25	$\overline{\text{PSEN}}$ low to valid instruction in		$3t_{CLCL}-105$	ns
t_{PXIX}	25	Input instruction hold after $\overline{\text{PSEN}}$	0		ns
t_{PXIZ}	25	Input instruction float after $\overline{\text{PSEN}}$		$t_{CLCL}-25$	ns
t_{AVIV}	25	Address to valid instruction in		$5t_{CLCL}-105$	ns
t_{PLAZ}	25	$\overline{\text{PSEN}}$ low to address float		10	ns
Data Memory					
t_{RLRH}	26, 27	$\overline{\text{RD}}$ pulse width	$6t_{CLCL}-100$		ns
t_{WLWH}	26, 27	$\overline{\text{WR}}$ pulse width	$6t_{CLCL}-100$		ns
t_{RLDV}	26, 27	$\overline{\text{RD}}$ low to valid data in		$5t_{CLCL}-165$	ns
t_{RHDX}	26, 27	Data hold after $\overline{\text{RD}}$	0		ns
t_{RHDZ}	26, 27	Data float after $\overline{\text{RD}}$		$2t_{CLCL}-60$	ns
t_{LLDV}	26, 27	ALE low to valid data in		$8t_{CLCL}-150$	ns
t_{AVDV}	26, 27	Address to valid data in		$9t_{CLCL}-165$	ns
t_{LLWL}	26, 27	ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	26, 27	Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low	$4t_{CLCL}-130$		ns
t_{QVWX}	26, 27	Data valid to $\overline{\text{WR}}$ transition	$t_{CLCL}-50$		ns
t_{WHQX}	26, 27	Data hold after $\overline{\text{WR}}$	$t_{CLCL}-50$		ns
t_{RLAZ}	26, 27	$\overline{\text{RD}}$ low to address float		0	ns
t_{WHLH}	26, 27	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock					
t_{CHCX}	29	High time	20		ns
t_{CLCX}	29	Low time	20		ns
t_{CLCH}	29	Rise time		20	ns
t_{CHCL}	29	Fall time		20	ns
Shift Register					
t_{XLXL}	28	Serial port clock cycle time	$12t_{CLCL}$		ns
t_{QVXH}	28	Output data setup to clock rising edge	$10t_{CLCL}-133$		ns
t_{XHQX}	28	Output data hold after clock rising edge	$2t_{CLCL}-60$		ns
t_{XHDX}	28	Input data hold after clock rising edge	0		ns
t_{XHDV}	28	Clock rising edge to input data valid		$10t_{CLCL}-133$	ns

NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and $\overline{\text{PSEN}} = 100\text{pF}$, load capacitance for all other outputs = 80pF .
- Interfacing the 83C576/87C576 to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

UPI AC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C, } -40^{\circ}\text{C to } +85^{\circ}\text{C, and } -40^{\circ}\text{C to } +125^{\circ}\text{C; } V_{CC} = 5\text{V } \pm 10\%, V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AR}	\overline{CS} , A setup to \overline{RD}	0		ns
t_{RA}	\overline{CS} , A hold after \overline{RD}	35		ns
t_{RR}	\overline{RD} pulse width	35		ns
t_{AD}	\overline{CS} , A to data out delay		45	ns
t_{RD}	\overline{RD} to data out delay		35	ns
t_{DF}	\overline{RD} to data float delay (guaranteed by design)		30	ns
t_{AW}	\overline{CS} , A setup to \overline{WR}	0		ns
t_{WA}	\overline{CS} , A hold after \overline{WR}	15		ns
t_{WW}	\overline{WR} pulse width	45		ns
t_{DW}	Data setup to \overline{WR}	5		ns
t_{WD}	Data hold after \overline{WR}	25		ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal.

The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE

- P – \overline{PSEN}
- Q – Output data
- R – \overline{RD} signal
- t – Time
- V – Valid
- W – \overline{WR} signal
- X – No longer a valid logic level
- Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
 t_{LLPL} = Time for ALE low to \overline{PSEN} low.

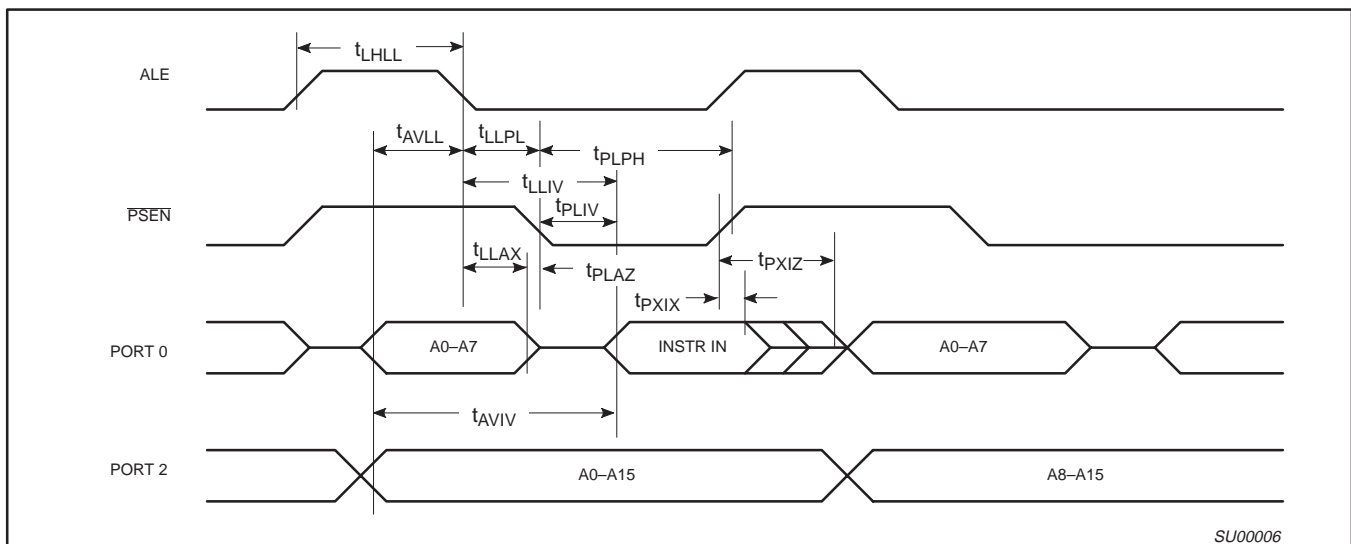


Figure 25. External Program Memory Read Cycle

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80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

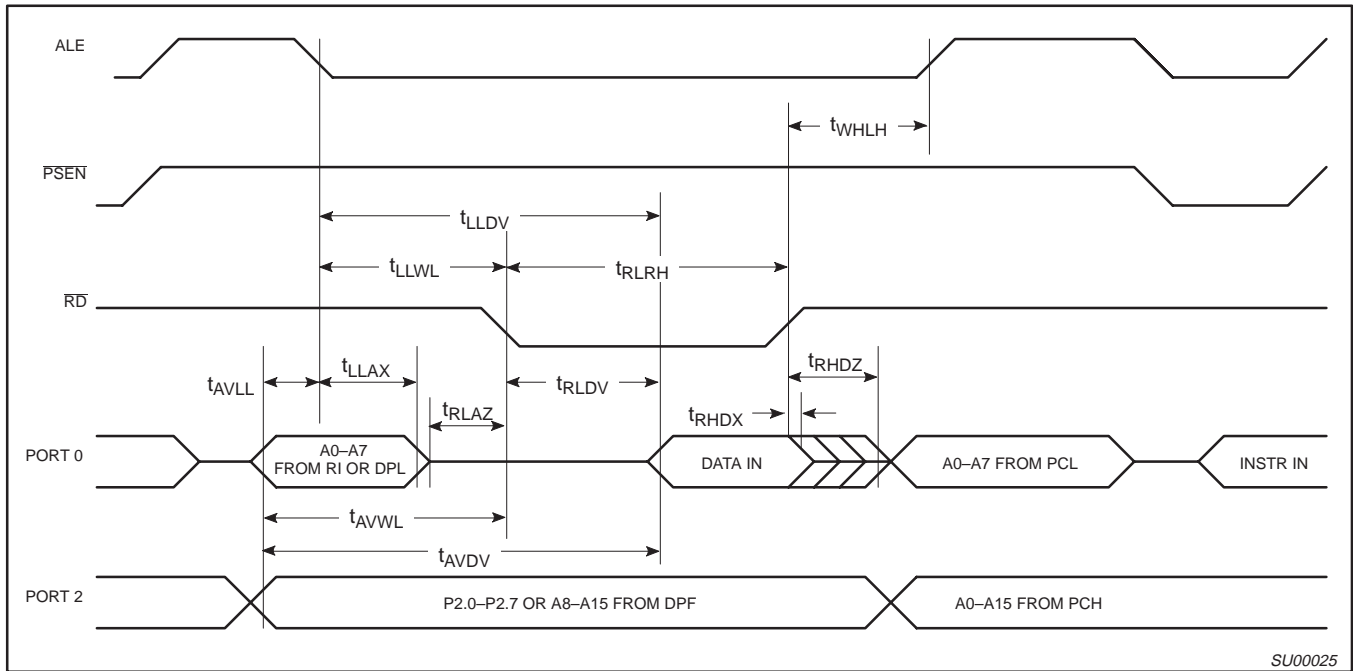


Figure 26. External Data Memory Read Cycle

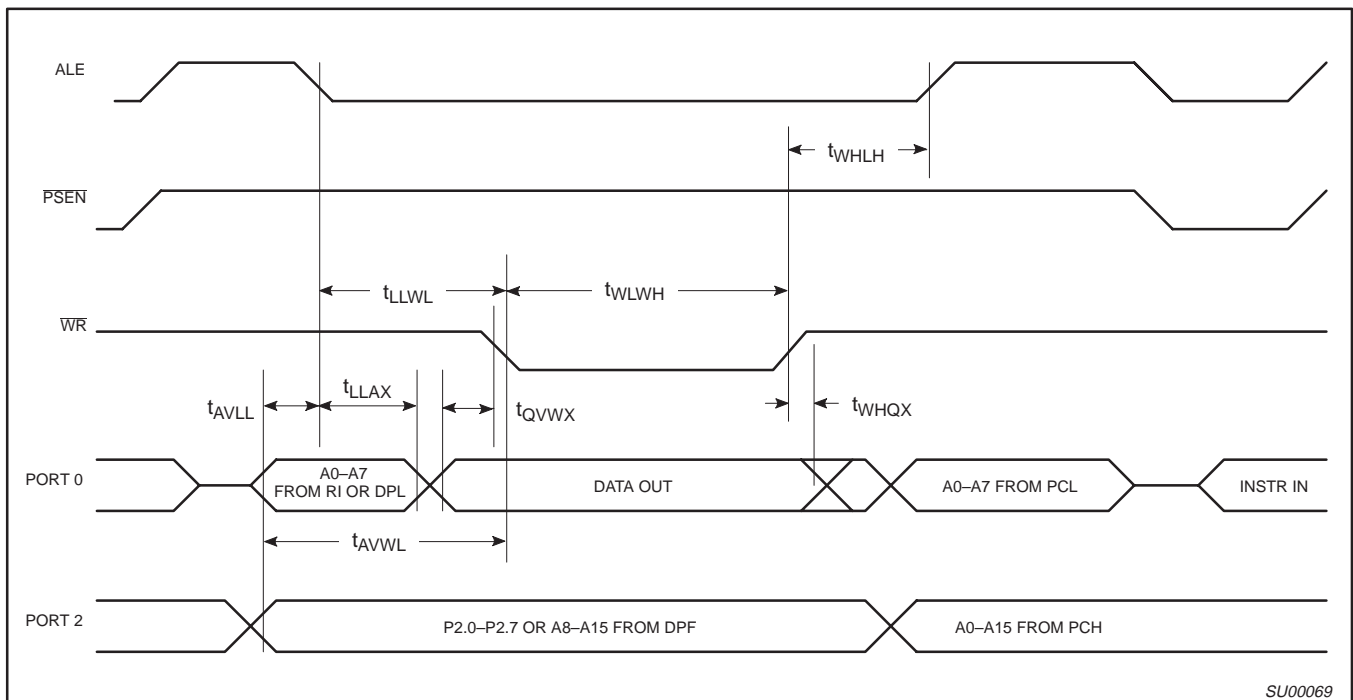


Figure 27. External Data Memory Write Cycle

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

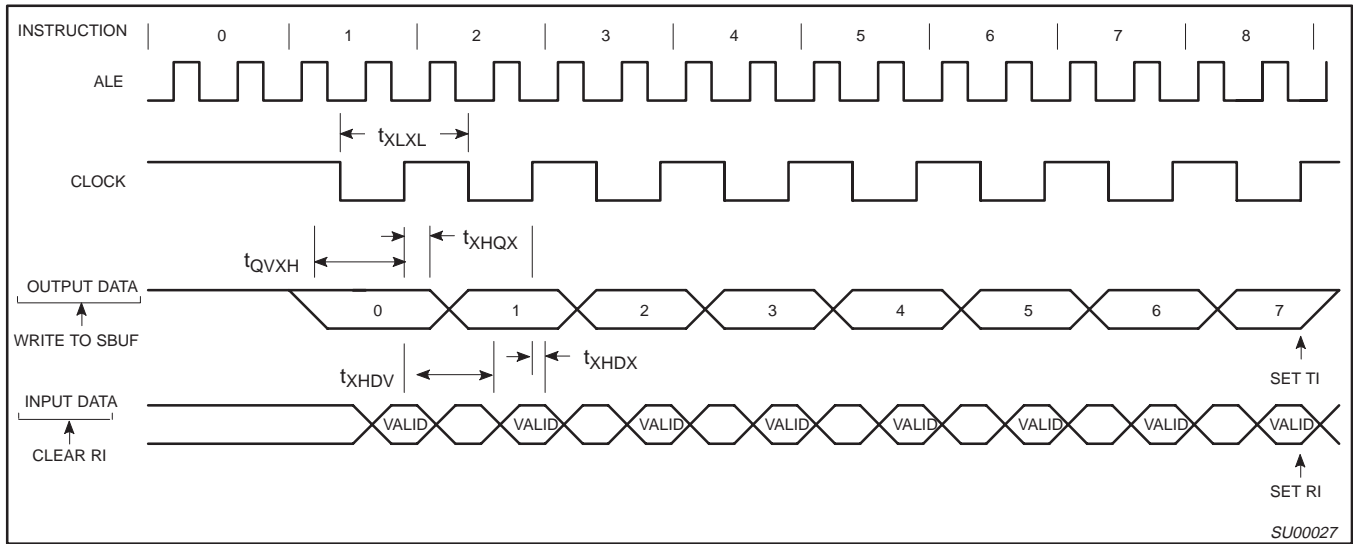


Figure 28. Shift Register Mode Timing

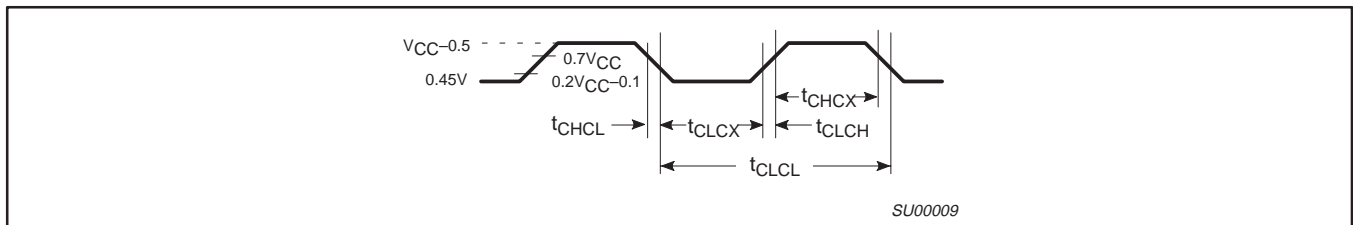


Figure 29. External Clock Drive

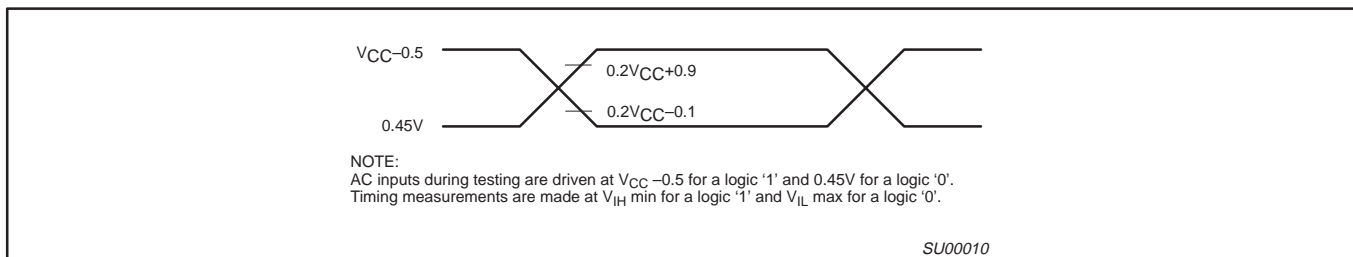


Figure 30. AC Testing Input/Output

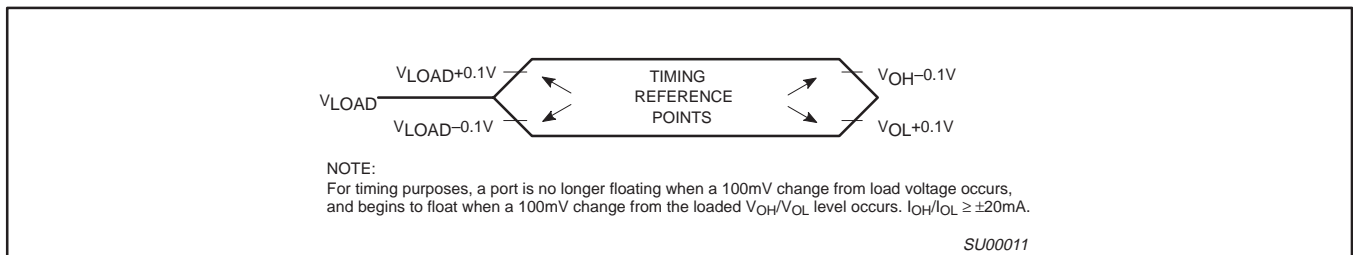


Figure 31. Float Waveform

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

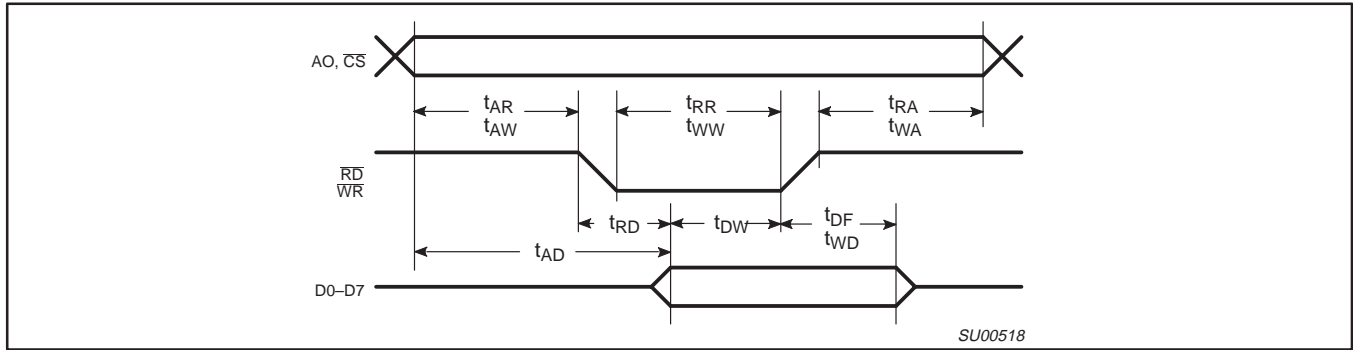


Figure 32. UPI Read/Write Cycles

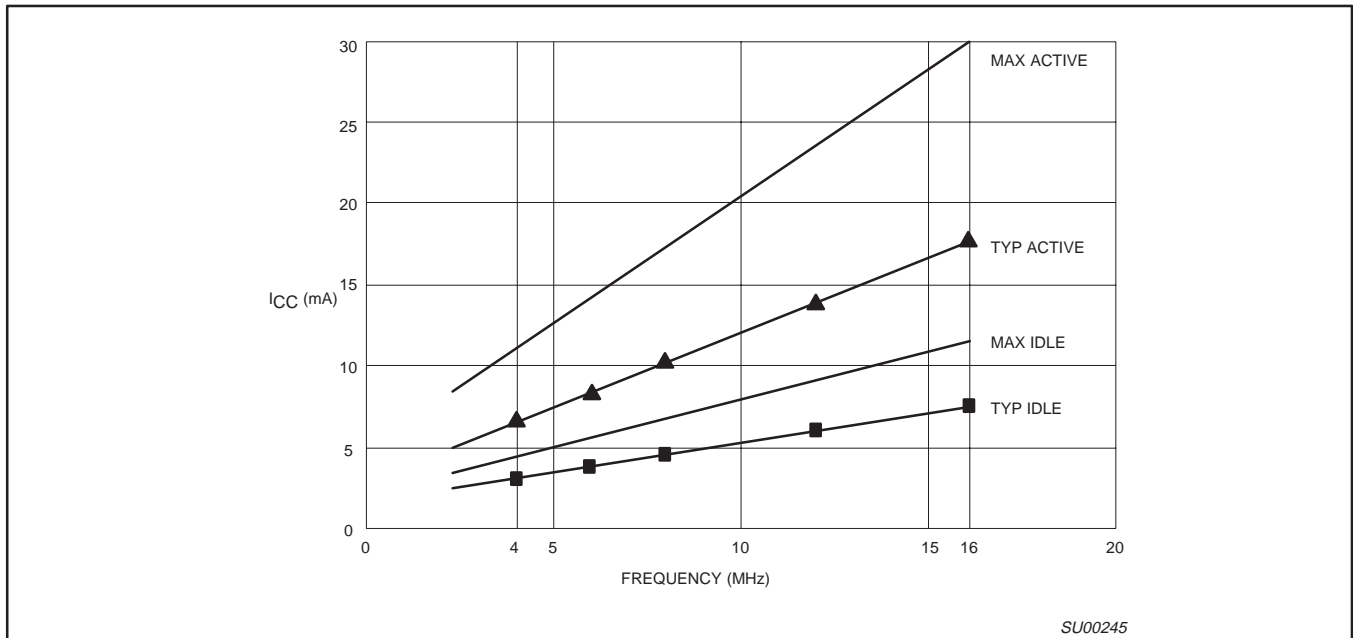


Figure 33. I_{CC} vs. FREQ

Valid only within frequency specifications of the device under test

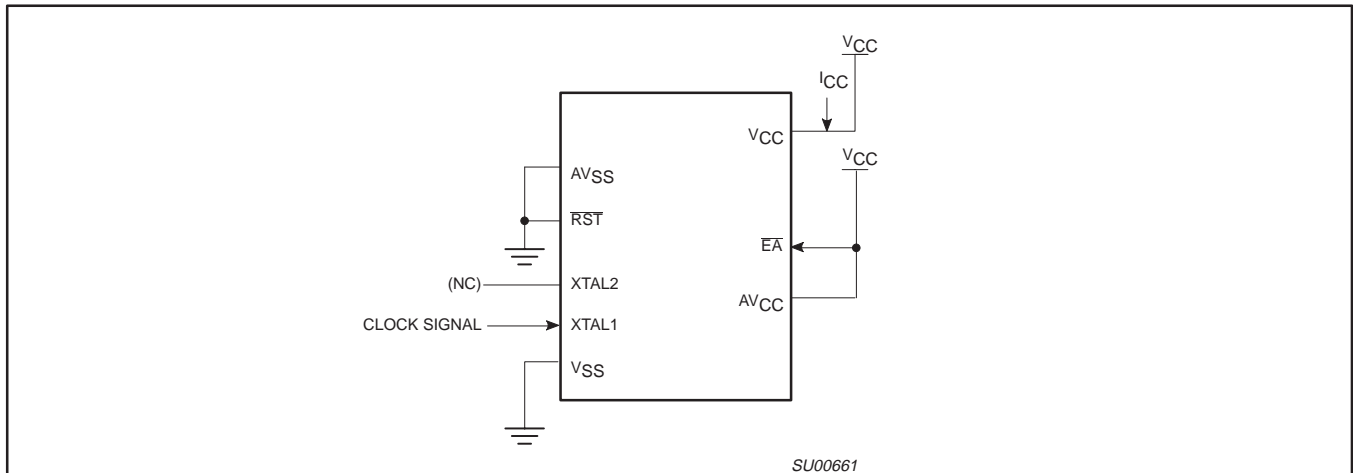


Figure 34. I_{CC} Test Condition, Active Mode
 All other pins are disconnected

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

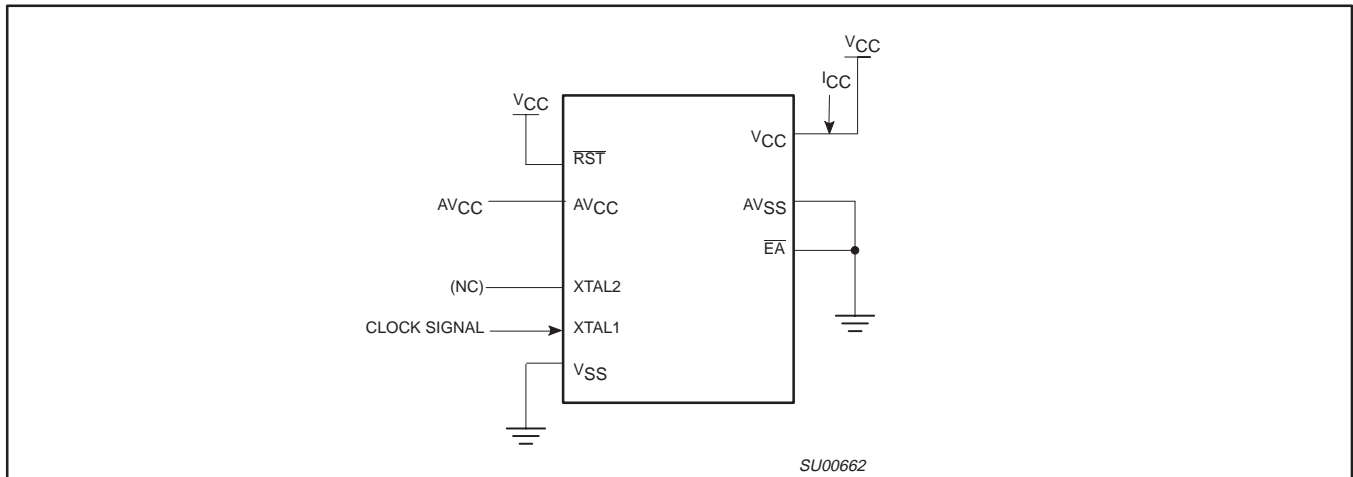


Figure 35. I_{CC} Test Condition, Idle Mode
 All other pins are disconnected

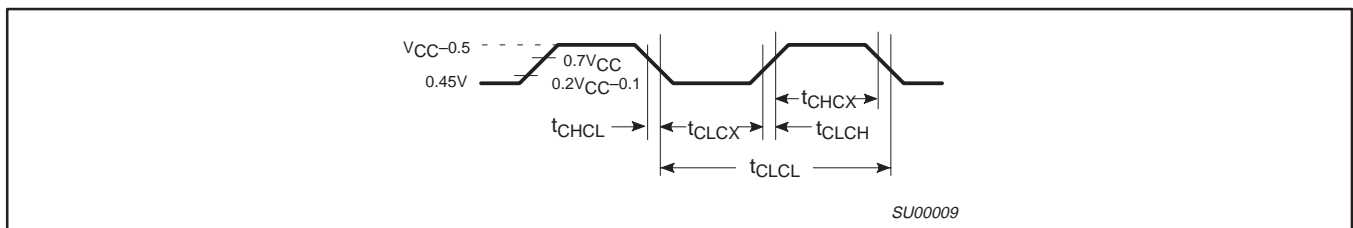


Figure 36. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

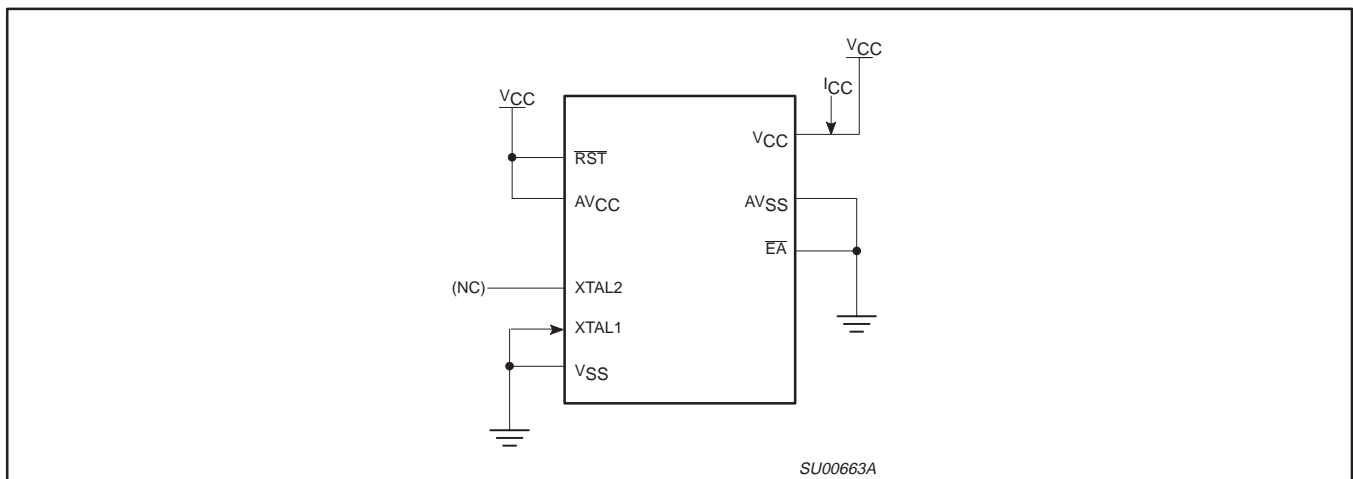


Figure 37. I_{CC} Test Condition, Power Down Mode
 All other pins are disconnected. $V_{CC} = 2\text{V to } 5.5\text{V}$

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

EPROM CHARACTERISTICS

To put the 87C576 in the parallel EPROM programming mode, PSEN must be held high during power up, then driven low with reset active. The 87C576 is programmed by using a modified Quick-Pulse Programming™ algorithm.

The 87C576 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C576 manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 38 and 39. Figure 40 shows the circuit configuration for normal program memory verification.

On-Board Programming (OBP)

The On-Board Programming facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the 87C576 through the serial port.

The OBP function is invoked by having the \overline{EA}/V_{PP} pin at the V_{PP} voltage level at the time that the part exits reset. The OBP function only requires that the TxD, RxD, V_{SS} , V_{CC} , and V_{PP} pins be connected to an external circuit in order to use this feature.

The OBP feature provides for the use of a wide range of baud rates independent of the oscillator frequency used. It is also adaptable to a wide range of oscillator frequencies. The OBP facility provides for both auto-echo and no-echo of received characters. The OBP feature requires that an initial character, an uppercase U, be sent to the 87C576 to establish the baud rate to be used.

Once baud rate initialization has been performed, the OBP facility only accepts Intel Hex records. The record-type field of these hex records are used to indicate either commands or data for the OBP facility. The maximum number of data bytes in a record is limited to 16 (decimal). These commands/data are summarized below:

Record Type	Command/Data Function
00	Data record, programs the part with data indicated in record starting with load address in the record
01	EOF record, no operation
02	Specify timing parameters <ul style="list-style-type: none"> – rec length = 3 bytes – load address = 0000 – 1st byte = timer count for 50µs programming pulse – 2nd byte = timer count for 10µs delay between pulses – 3rd byte = 0AH
03	Program security bits <ul style="list-style-type: none"> – rec length = 1 byte – load address = 0000 – 1st byte = sec bit values (xxxx xxB2B1)
04	Display contents of USER EPROM array <ul style="list-style-type: none"> – rec length = 00 – load address = 0000
05	Verify security bit status <ul style="list-style-type: none"> – rec length = 00 – load address = 0000

Quick-Pulse Programming (Parallel)

The setup for microcontroller quick-pulse programming is shown in Figure 38. Note that the 87C576 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 3 and 2, as shown in Figure 38. The code byte to be programmed into that location is applied to port 0. RST, \overline{PSEN} and pins of ports 2 and 1 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/ \overline{PROG} is pulsed low 25 times as shown in Figure 39.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the \overline{EA}/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 3 and 2 as shown in Figure 40. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P1.0 and P1.1 need to be pulled to a logic low. The values are:
(030H) = 15H indicates manufactured by Philips
(031H) = B6H indicates 87C576

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

™Trademark phrase of Intel Corporation.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.7	P2.6	P1.1	P1.0
Read signature	0	0	1	1	0	0	0	0
Program code data	0	0	0*	V _{PP}	1	0	1	1
Verify code data	0	0	1	1	0	0	1	1
Pgm encryption table	0	0	0*	V _{PP}	1	0	1	0
Pgm security bit 1	0	0	0*	V _{PP}	1	1	1	1
Pgm security bit 2	0	0	0*	V _{PP}	1	1	0	0

NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.

2. V_{PP} = 12.75V ±0.25V.

3. V_{CC} = 5V±10% during programming and verification.

* ALE/PROG receives 5 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 50µs (±10µs) and high for a minimum of 10µs.

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

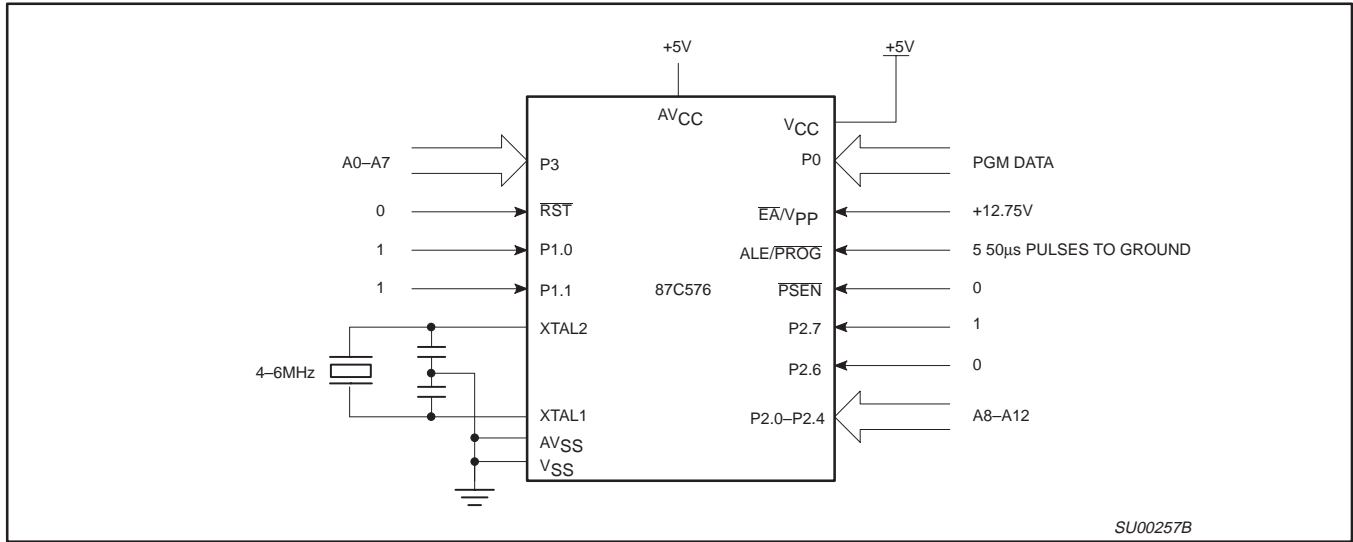


Figure 38. Programming Configuration

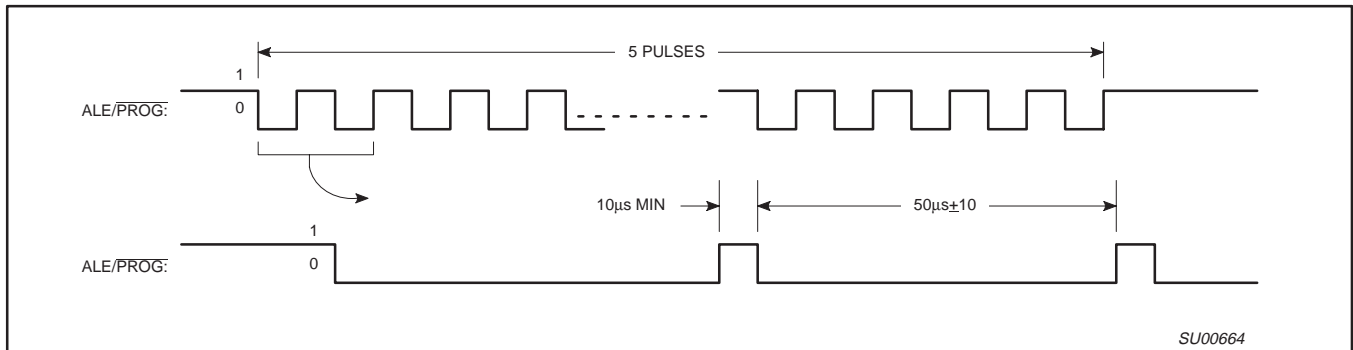


Figure 39. PROG Waveform

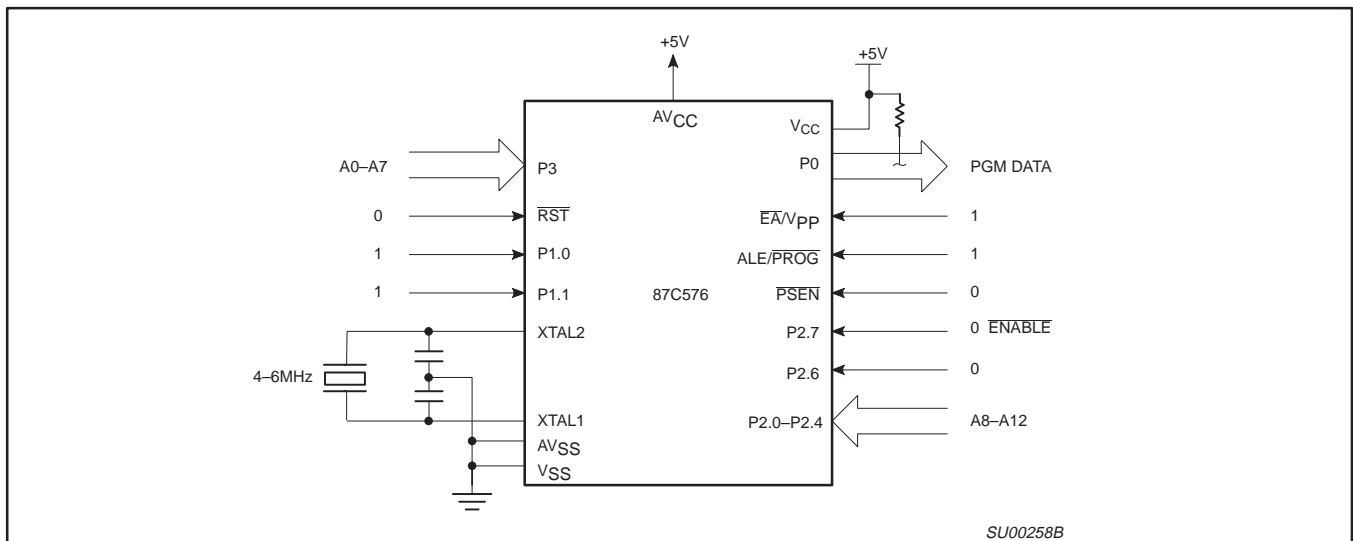


Figure 40. Program Verification

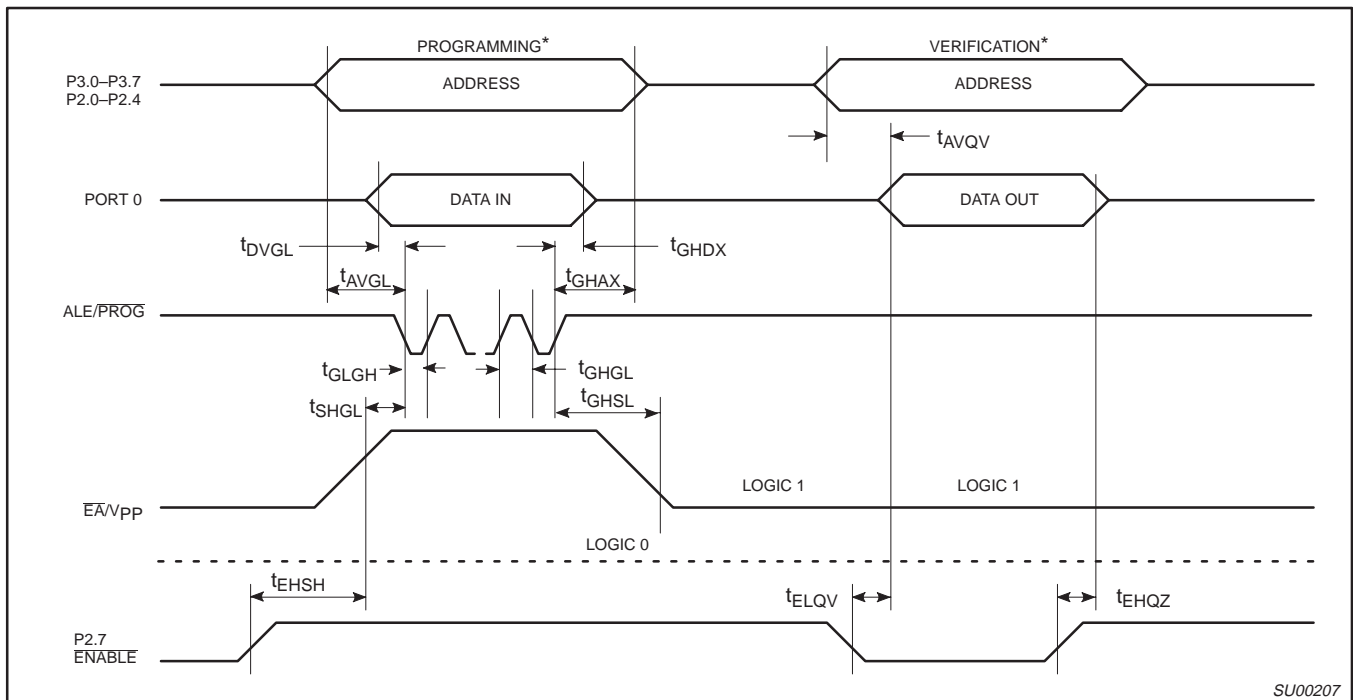
80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (See Figure 41)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V _{PP}	Programming supply voltage	12.5	13.0	V
I _{PP}	Programming supply current		50	mA
1/t _{CLCL}	Oscillator frequency	4	12	MHz
t _{AVGL}	Address setup to $\overline{\text{PROG}}$ low	48t _{CLCL}		
t _{GHAX}	Address hold after $\overline{\text{PROG}}$	48t _{CLCL}		
t _{DVGL}	Data setup to $\overline{\text{PROG}}$ low	48t _{CLCL}		
t _{GHDx}	Data hold after $\overline{\text{PROG}}$	48t _{CLCL}		
t _{EHS}	P2.7 ($\overline{\text{ENABLE}}$) high to V _{PP}	48t _{CLCL}		
t _{SHGL}	V _{PP} setup to $\overline{\text{PROG}}$ low	10		μs
t _{GHSL}	V _{PP} hold after $\overline{\text{PROG}}$	10		μs
t _{GLGH}	$\overline{\text{PROG}}$ width	40	60	μs
t _{AVQV}	Address to data valid		48t _{CLCL}	
t _{ELQZ}	$\overline{\text{ENABLE}}$ low to data valid		48t _{CLCL}	
t _{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48t _{CLCL}	
t _{GHGL}	$\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low	10		μs



* FOR PROGRAMMING VERIFICATION SEE FIGURE 38.
 FOR VERIFICATION CONDITIONS SEE FIGURE 40.

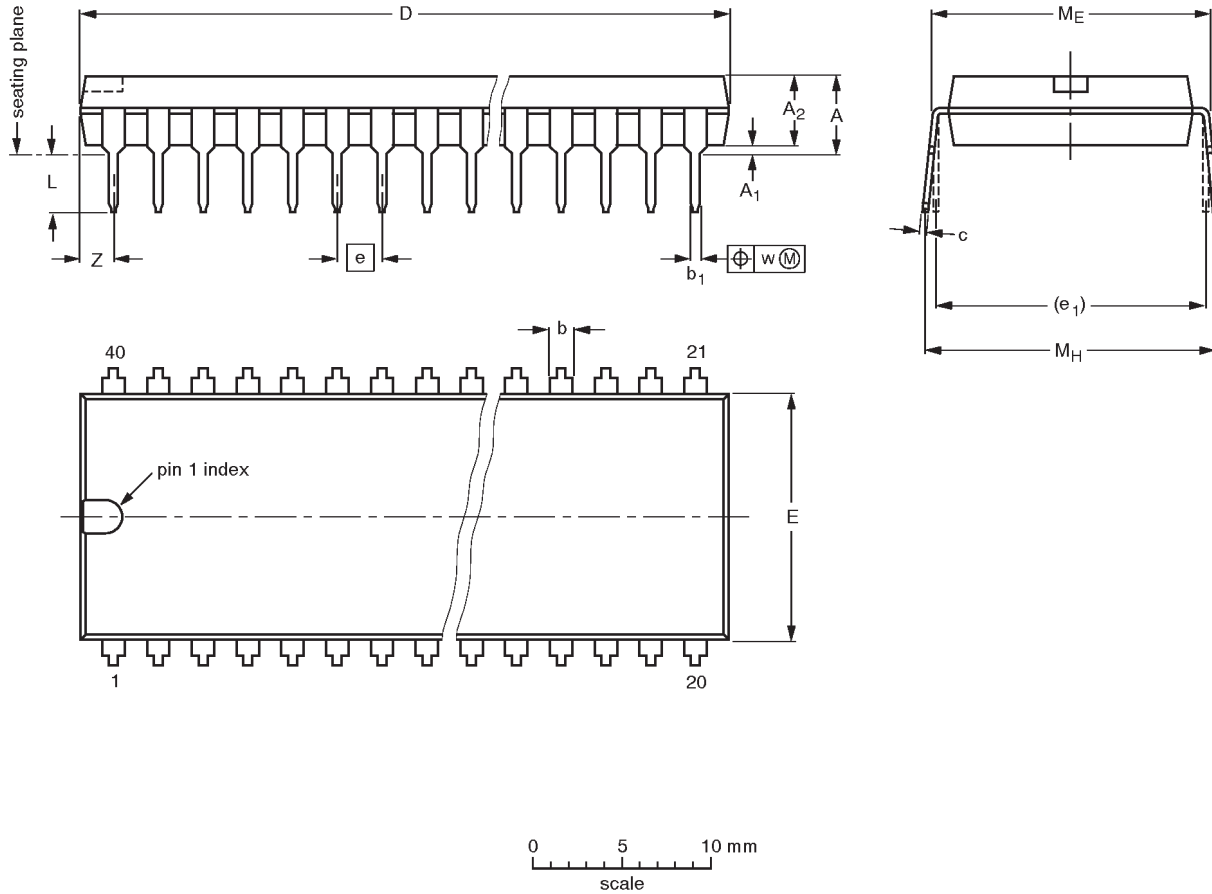
Figure 41. EPROM Programming and Verification

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

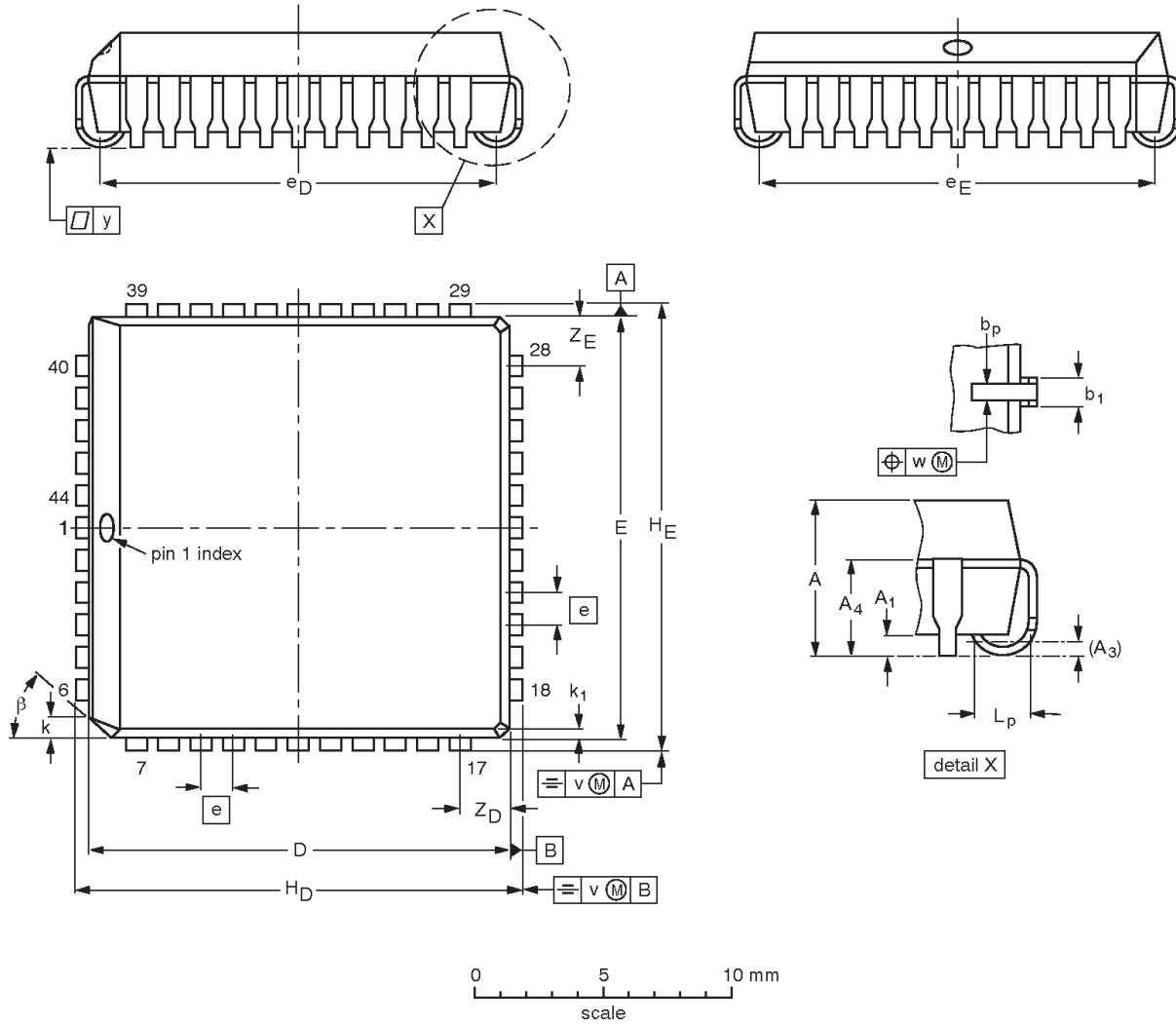
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				92-11-17 95-01-14

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

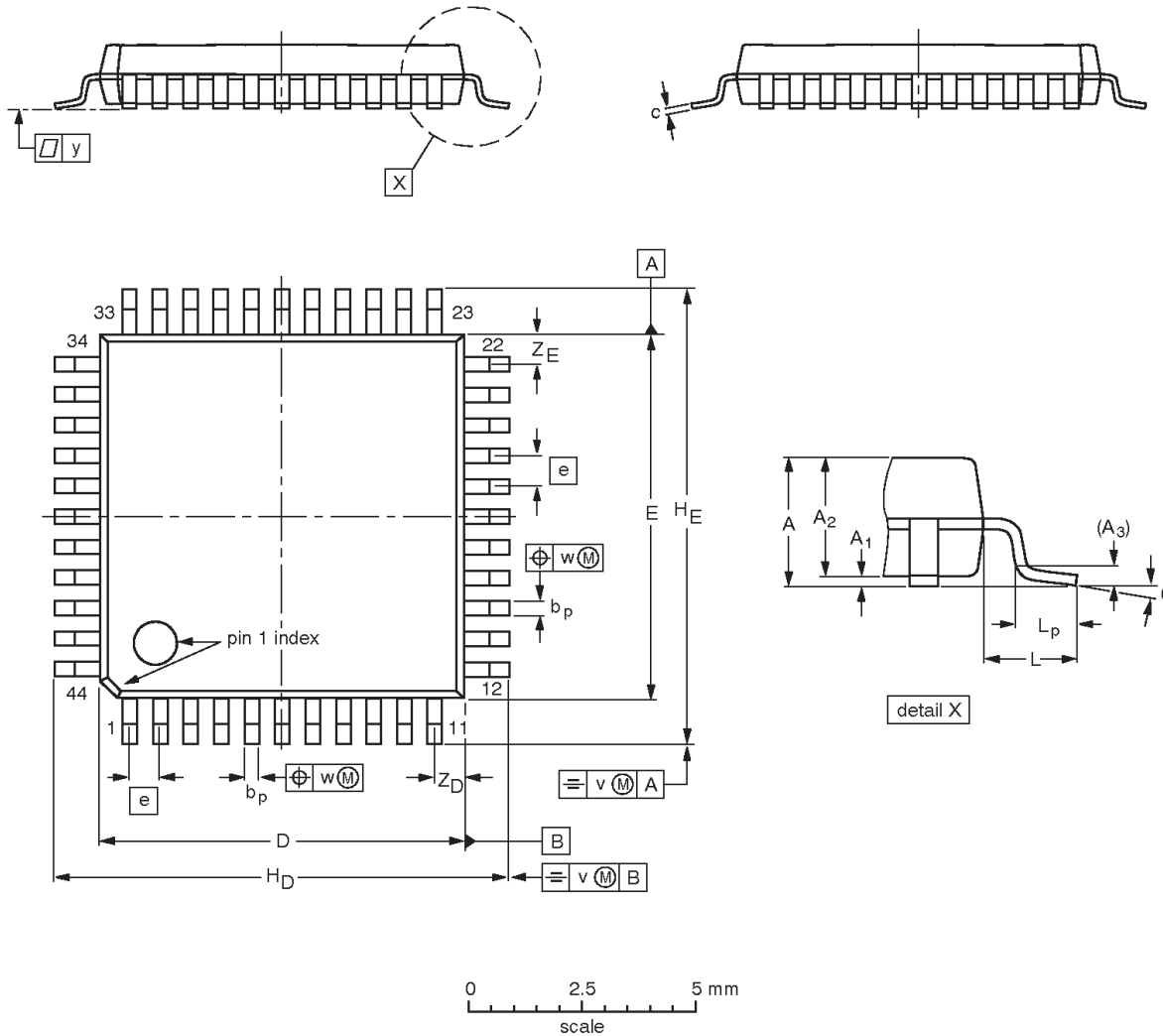
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				95-02-25 97-12-16

80C51 8-bit microcontroller family
 8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
 failure detect circuitry, watchdog timer

83C576/87C576

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						95-02-04 97-08-01

80C51 8-bit microcontroller family
8K/256 OTP/ROM, 6 channel 10-bit A/D, 4 comparators,
failure detect circuitry, watchdog timer

83C576/87C576

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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