CML Microcircuits

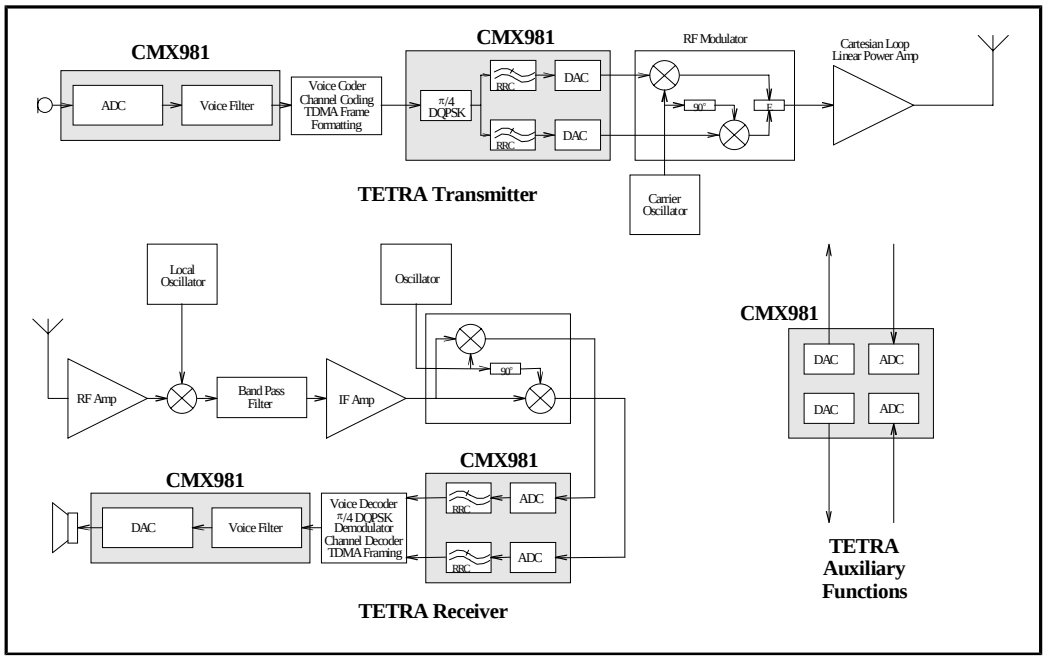
COMMUNICATION SEMICONDUCTORS

CMX981
Advanced Digital Radio Baseband Processor

D/981/4 September 2004 Provisional Issue

Features

- **Programmable Digital Tx and Rx Filters**
- **High Performance Codecs**
  - **Radio Rx: 2 x 16-Bit Sigma Delta ADC**
  - **Radio Tx: 2 x 14-Bit Sigma Delta DAC**
  - **Auxiliary: 6 x 10-Bit ADC**
  - **Auxiliary: 4 x 10-Bit DAC**
  - **Voice: 14-Bit Linear with Digital Filter**
- **π/4 DQPSK and Other Modulations**
- **Full Duplex Operation**
- **C-BUS and 3 Fast Serial Bus Interfaces**
- **Low Power for Portable Terminals**
- **2.5V Supply With 3.3V Tolerant I/O**
- **130mW Speaker Amplifier (8Ω load)**
- **16.5mW Earpiece Amplifier (32Ω load)**



1. Brief Description

The CMX981 Advanced Digital Radio Baseband Processor is a combination codec/processor that interfaces analogue and digital sections of a Digital Radio System and performs critical DSP-intensive functions. The device supports portable, mobile and base station TErrestrial Trunked RAdio (TETRA) system applications and is also sufficiently flexible for use in other demanding digital radio systems.

The CMX981 transmit path comprises all functions required to convert digital 'symbol' data into suitably filtered analogue I and Q signals for external up-conversion and transmission. This includes digital control of output amplitudes and offsets and fully programmable digital filters. Default coefficients provide the root raised cosine (RRC) response required for TETRA.

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(Continued from front page)

The CMX981 receive path accepts differential analogue baseband I/Q signals, samples them and performs digital channel select filtering to simplify host processing and data extraction. Internal digital offset correction and the digital filters are fully programmable. Default coefficients provide the RRC response required for TETRA.

Auxiliary DAC and ADC functions are included for the control and measurement of the radio system RF section. This may include AFC, AGC, RSSI, or part of the control system for a Cartesian loop.

The voice codec converts voice signals to and from digital form and can be configured to apply a digital voice filter with a frequency response suitable for specification G.712. The encode path accepts a differential analogue audio input signal, converts it to digital form and applies digital voice filtering to produce a processed digital stream. The decode path accepts a digital stream written to the serial interface, applies digital voice filtering, converts the result to an analogue signal, and presents the signal at differential speaker or single-ended earphone analogue driver outputs. This path also includes sidetone addition and a ring tone generator.

CONTENTS

It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

2. Block Diagram

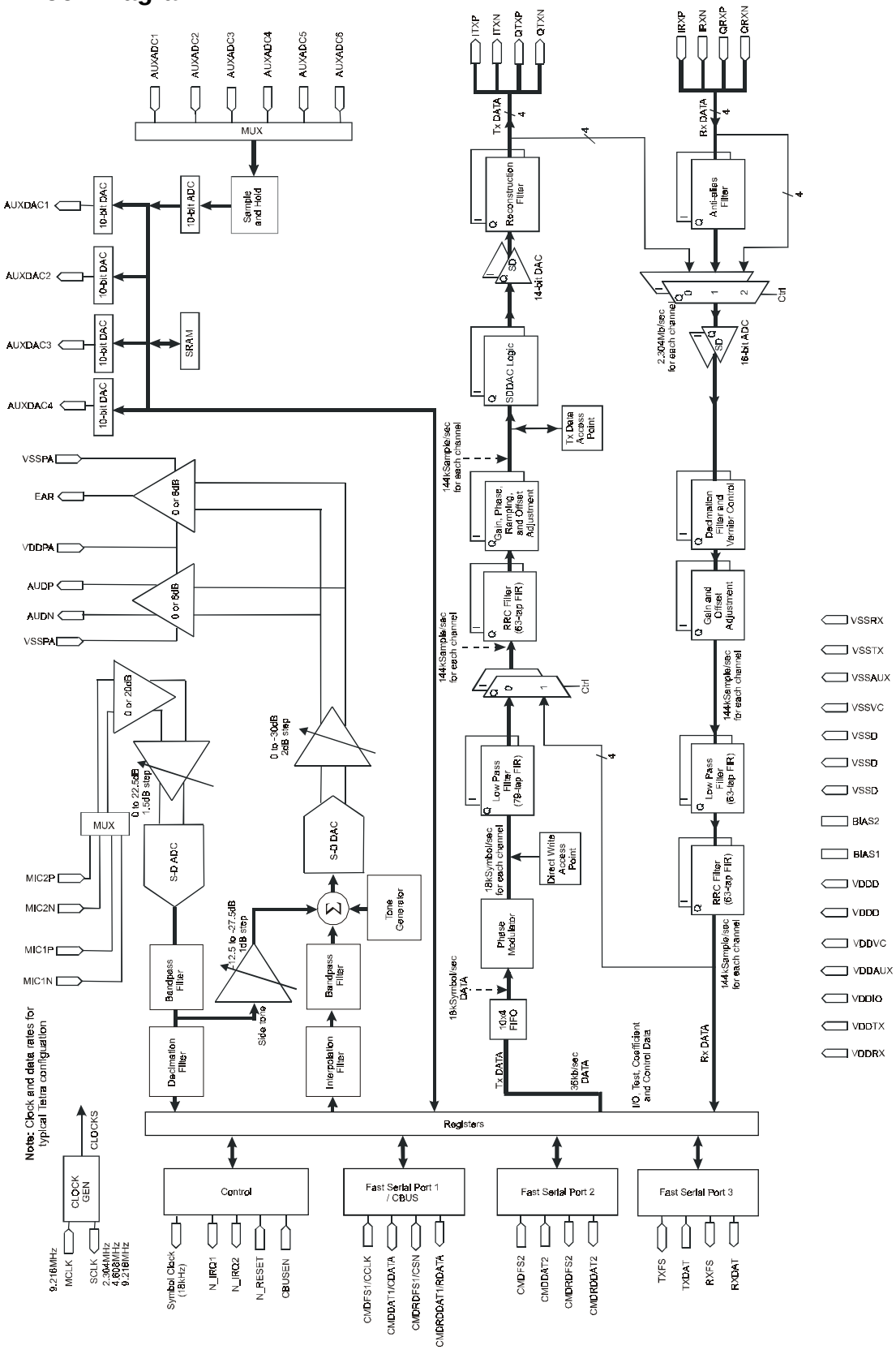


Figure 1 Block Diagram

3. Signal List

Q1 Package 64-pin VQFN	Signal		Description
Pin No.	**Name**	**Type**	
34	MCLK	I/P	Master clock input (typically 9.216MHz)
33	SCLK	O/P	Serial interface clock
46	CBUSEN	I/P	C-BUS / FSB select
35	CMDFS1/CCLK	I/P	Command port 1 serial interface frame sync C-BUS clock
37	CMDDAT1/CDATA	BI	Command port 1 serial interface data C-BUS command data
38	CMDRDFS1/CSN	BI	Command port 1 serial interface read frame sync C-BUS chip select
36	CMDRDDAT1/RDATA	O/P	Command port 1 serial interface read data C-BUS read data
50	CMDFS2	I/P	Command port 2 serial interface frame sync
49	CMDDAT2	I/P	Command port 2 serial interface data
48	CMDRDFS2	O/P	Command port 2 serial interface read frame sync
47	CMDRDDAT2	O/P	Command port 2 serial interface read data
43	TXFS	BI	Transmit port serial interface frame sync
44	TXDAT	I/P	Transmit port serial interface data
41	RXFS	O/P	Receive port serial interface frame sync
40	RXDAT	O/P	Receive port serial interface data
30	SYMCLOCK	O/P	Internal symbol clock
31	N_IRQ1	O/P	Interrupt request 1. This pin has a low impedance pulldown to V_{SSD} when active and a high impedance when inactive. An external pullup resistor is required.
32	N_IRQ2	O/P	Interrupt request 2. This pin has a low impedance pulldown to V_{SSD} when active and a high impedance when inactive. An external pullup resistor is required.
22	ITXP	O/P	Transmit "I" channel, positive output
23	ITXN	O/P	Transmit "I" channel, negative output
26	QTXP	O/P	Transmit "Q" channel, positive output
25	QTXN	O/P	Transmit "Q" channel, negative output

Q1 Package 64-pin VQFN	Signal		Description
Pin No.	**Name**	**Type**	
13	IRXP	I/P	Receive "I" channel, positive input
14	IRXN	I/P	Receive "I" channel, negative input
17	QRXP	I/P	Receive "Q" channel, positive input
16	QRXN	I/P	Receive "Q" channel, negative input
29	N_RESET	I/P	Chip reset
55	MIC1P	I/P	Microphone 1, positive input
53	MIC1N	I/P	Microphone 1, negative input
56	MIC2P	I/P	Microphone 2, positive input
52	MIC2N	I/P	Microphone 2, negative input
62	EAR	O/P	Voice codec earpiece, positive output
58	AUDP	O/P	Voice codec speaker driver, positive output
60	AUDN	O/P	Voice codec speaker driver, negative output
2	AUXDAC1	O/P	Auxiliary DAC channel 1
1	AUXDAC2	O/P	Auxiliary DAC channel 2
64	AUXDAC3	O/P	Auxiliary DAC channel 3
63	AUXDAC4	O/P	Auxiliary DAC channel 4
28	~	I/P	For manufacturers use only. Connect this pin to V_{SSD}
10	AUXADC1	I/P	Auxiliary ADC channel 1
9	AUXADC2	I/P	Auxiliary ADC channel 2
8	AUXADC3	I/P	Auxiliary ADC channel 3
6	AUXADC4	I/P	Auxiliary ADC channel 4
5	AUXADC5	I/P	Auxiliary ADC channel 5
4	AUXADC6	I/P	Auxiliary ADC channel 6
20	BIAS1	BI	Analogue bias level. This pin should be decoupled to V_{SSRX}
19	BIAS2	BI	DAC reference level. This pin should normally be connected to V_{SSTX}
15	VDDRX	Power	Rx analogue positive supply rail. This pin should be decoupled to V_{SSRX}
27	VDDTX	Power	Tx analogue positive supply rail. This pin should be decoupled to V_{SSTX}

Q1 Package 64-pin VQFN	Signal	Description

Pin No.	Name	Type	
21	VDDIO	Power	I/O positive supply rail. This pin should be decoupled to V_{SSD}
3	VDDAUX	Power	Auxiliary analogue positive supply rail. This pin should be decoupled to V_{SSAUX}
54	VDDVC	Power	Voice codec analogue positive supply rail. This pin should be decoupled to V_{SSVC}
59	VDDPA	Power	Power amplifier positive supply rail. This pin should be decoupled to V_{SSPA}
42, 12	VDDD	Power	Digital positive supply rail. This pin should be decoupled to V_{SSD}
18	VSSRX	Ground	Rx analogue negative supply rail.
24	VSSTX	Ground	Tx analogue negative supply rail.
7	VSSAUX	Ground	Auxiliary analogue negative supply rail.
51	VSSVC	Ground	Voice codec analogue negative supply rail.
57, 61	VSSPA	Ground	Power amplifier negative supply rail.
39, 45, 11	VSSD	Ground	Primary digital negative supply rail.
CENTRAL METAL PAD	SUB	NC	Leave unconnected..

Notes:

I/P	=	Input
O/P	=	Output
BI	=	Bidirectional
T/S	=	3-state Output
NC	=	No Connection

4. External Components

Rx Inputs

When using the internal anti-alias filter, the following is recommended:

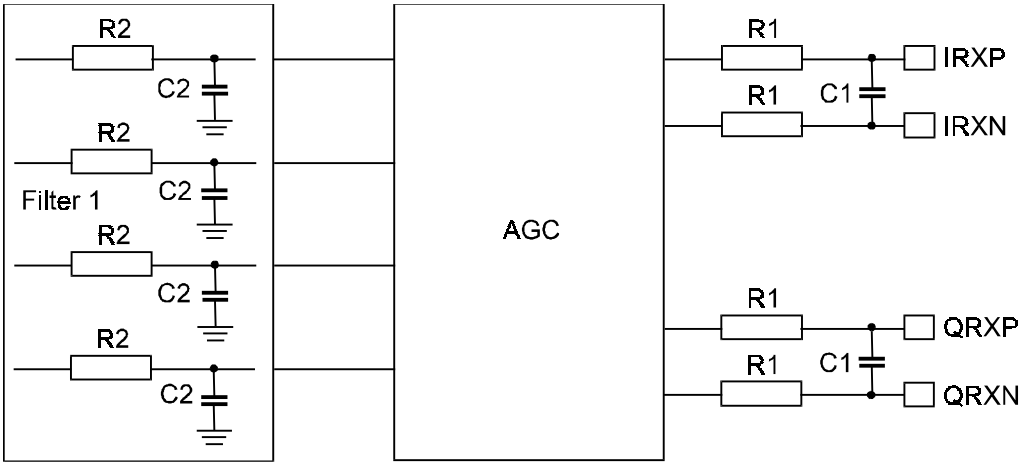


Figure 2a Recommended External Components - Rx Inputs

Example values (MCLK = 9.216MHz):

R1 = 220Ω C1 = 1.5nF (R1, C1 precise values are not critical) (-3dB at 241kHz)
R2 = 1.2kΩ C2 = 3.9nF (R2 x C2 time constant should give -3dB at 34kHz ±10%

The RC stage formed by R2 and C2 combined with the internal anti alias filter and Rx FIRs gives a good approximation to the desired filter characteristics and near-constant group delay over the passband. When not using the internal anti alias filter, it is suggested that the user should follow the guidelines in Section 5.4.1. In both cases, there should be at least one filter pole close to the chip inputs.

Tx Outputs

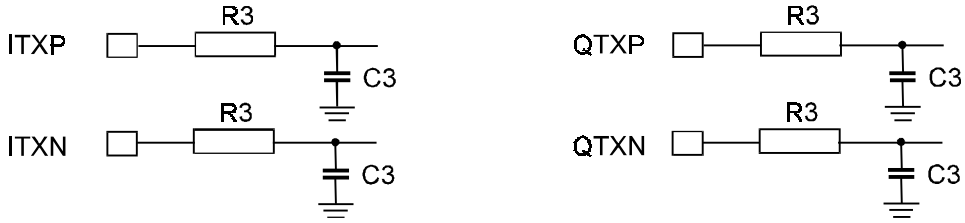


Figure 2b Recommended External Components - Tx Outputs

Example values (MCLK = 9.216MHz):

R3 = 6.2kΩ C3 = 1nF (R3 x C3 time constant should give -3dB at 26kHz ±10%.

The RC stage formed by R3 and C3 combined with the internal reconstruction filter and the Tx FIRs gives a good approximation to the desired filter characteristics and near-constant group delay over the passband. When the default master clock frequency is not used the R2 x C2 and R3 x C3 products may be scaled with MCLK, but care should be taken to ensure that the FIR filter coefficients are designed to compensate for any amplitude and phase distortion due to both on and off-chip filter components. This compensation is included in the default filter coefficients. See section 6.3 for further details.

Voice Codec Encoder Inputs

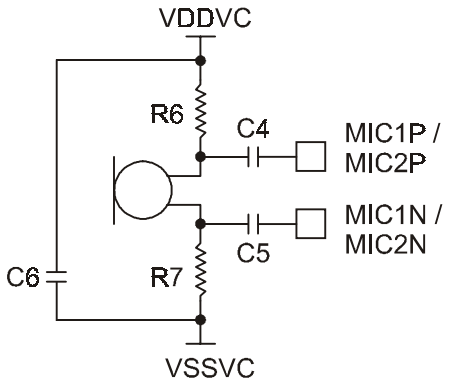


Figure 2c Recommended External Components - Codec Encoder Inputs

C4 = C5 = 0.47µF.
C6 = 1.0µF.
R6 = R7 = 1.0kΩ.

Voice Codec Decoder Outputs

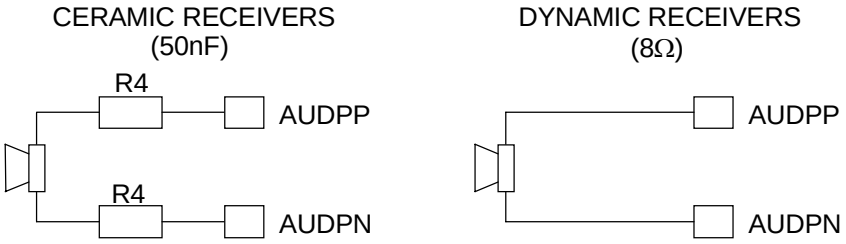


Figure 2d Recommended External Components - Codec Speaker Outputs

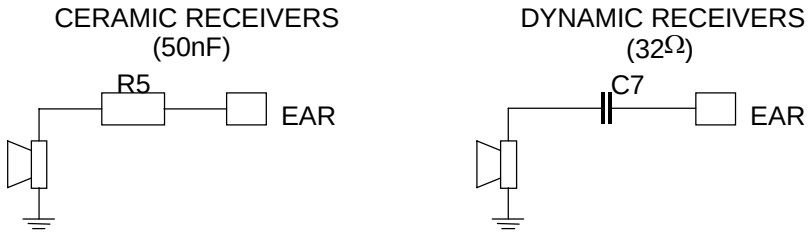


Figure 2e Recommended External Components - Codec Earpiece Output

R4 > 50Ω.
R5 > 50Ω.
C7 = 100µF.

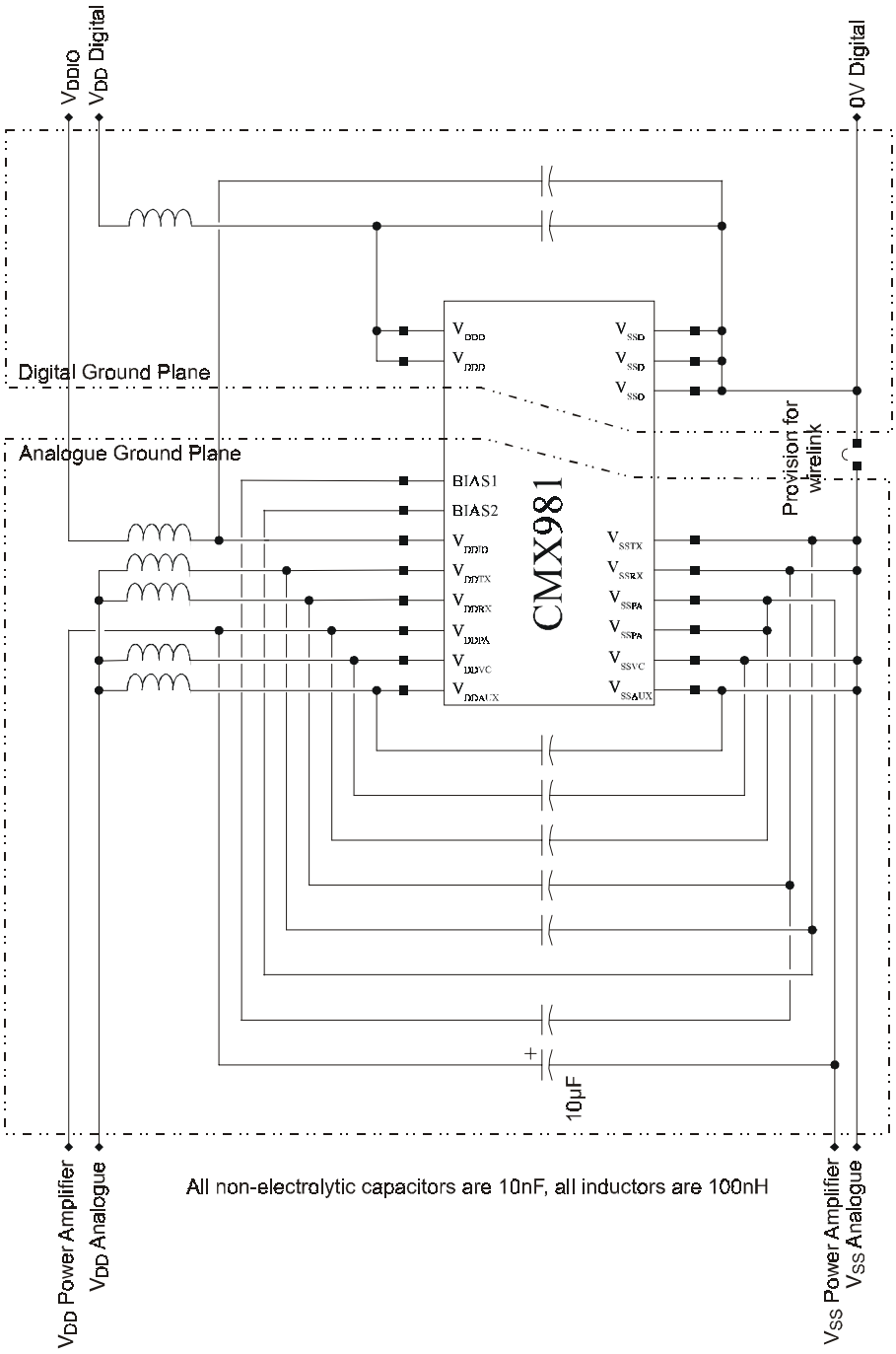


Figure 2 Recommended External Components

To achieve good noise performance, V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that the printed circuit board be laid out with a ground plane in the CMX981 area to provide a low impedance connection between the V_{SS} pins and the V_{DD} and V_{BIAS} decoupling capacitors. It is also important to achieve a low impedance connection between the Xtal capacitors and the ground plane. Also note that the power amplifier supplies should be provided from a separate low impedance source to prevent cross-talk into the TX channels. To obtain best performance from the auxiliary ADCs, input signals should be referenced to the local V_{SSAUX} supply.

5. General Description

Tx Functions

- Four word deep FIFO
- Bypassable π/4 DQPSK modulator
- Programmable FIR filters
- Transmit ramping function
- Gain, phase and offset adjustment
- 2 x 14-bit resolution sigma delta DAC converters
- Programmable sample rate

Rx Functions

- 2 x 16-bit resolution sigma delta ADC converters
- Anti-alias and decimation filter with adjustable sampling point
- Gain and offset adjustment
- Programmable FIR filters
- Programmable sample rate

Auxiliary Functions

- A 6-input 10-bit ADC converter with internal sample and hold
- 4 x 10-bit DAC converters
- RAM driven DAC mode

Voice Codec Functions

- 14-bit resolution sigma delta ADC and DAC converters
- 130mW into 8Ω load differential speaker amplifier
- 16.5mW into 32Ω load earpiece amplifier
- Ring tone generator
- Sidetone addition

Serial Interface

- Three DSP compatible serial ports
- One serial port can be configured as a C-BUS interface
- Selectable serial clock rate up to MCLK
- Bidirectional mode
- Hardware interlock modes
- Auto power save mode

5.1 Programmable FIR Filter Architecture

A common FIR filter architecture is employed within both the transmit and receive data paths. The filters use a small local static RAM for efficient data and coefficient storage during filter operations, together with a dedicated hardware multiplier and accumulator for each filter.

On reset, the coefficient RAMs are loaded with default values that provide the required response to meet the needs of a TETRA baseband system (this takes 1 sample period). In the default modes the dynamic range of arithmetic units are sufficient for all normal input data levels without causing overflows. Each filter has an odd number of default coefficients, which are symmetrical, giving a linear phase response. These coefficients may be overwritten to adapt to other systems or compensate for deficiencies outside the device. However the user is then responsible for ensuring that supplied values do not cause arithmetic overflows to occur within an accumulation cycle. Overflow logic within each filter can detect such events and cause interrupts to be generated under user control.

The data RAMs store the filter input data samples and operate upon these values to provide the general FIR transfer function:

$$y(k) = \sum_{n=1}^{n=FL} A_n.D_{(n-k)}$$

where: FL is the filter tap length,
A_n is the nth filter coefficient,
$D_{(n-k)}$ is the data sample supplied to the filter n-k samples previously

When a filter is deactivated, coefficient RAMs retain their state, while the data RAMs are reset to zero. This ensures that the filters start from a quiescent state and prevents filter "memory" from a previous data frame. Asserting the N_RESET pin will cause all programmable filter coefficients to return to default values. Alternatively, the Tx and Rx path filter coefficients may be reset independently from each other by use of a control bit. The data RAMs, unlike the coefficient RAMs, are not directly accessible to the user.

To overwrite the default coefficients, the user should first ensure that the Rx and/or TX path is inactive as appropriate and that the clocks are not stopped for that channel. Bit 0 in the **ConfigCtrl2** register must then be asserted. Setting this bit high resets the coefficient pointer to the first coefficient. The most significant bits (eight for the Rx filters, four for the Tx filters) must then be written to the appropriate coefficient address ($19, $1B, $1D or $1F). Writing the eight least significant bits to the appropriate coefficient address ($18, $1A, $1C or $1E) will increment the coefficient pointer to the next location. This process is repeated until all 63 (40 for the 79-tap filter) locations have been programmed. To program the next filter, bit 0 in the **ConfigCtrl2** register must be cleared and re-asserted.

All filters, except the 79-tap filter, allow access to the complete coefficient set, although the default values are symmetrical about (FL+1)/2. This will enable users to realise non-symmetrical filter functions should this be required.

All filters can be effectively bypassed by setting any single coefficient to unity (2^{11}-1 in the Tx and 2^{15}-1 in Rx) and all others to zero. The chosen positions of the "unity" coefficient will vary the internal group delay, thus this feature should be used with care. For example, the Tx ramping feature has a built in delay that defaults to the expected group delay for the Tx filter path. Ramp delay may be varied, if necessary, by use of the **RampCtrl** register. The default group delay can be retained by choosing the central coefficient as "unity". The 79-tap filter has only one half of the coefficient RAM available, so can only implement symmetrical (linear phase) filter responses. Thus, when accessing this filter, only locations A1-A40 are valid. In addition, to bypass this filter, the central coefficient (A40) should be chosen as "unity" since this is the only unique coefficient.

5.2 Programmable Sample Rates

The sample rates of the Tx, Rx and Codec sections can be independently programmed by the **ClkDiv1** and **ClkDiv2** registers. The values in these registers determine the MCLK divide ratio that is used to generate the sample clock for each section. The divide ratios are 16 times the register values for the Tx and Rx sections, and 128 times the register value for the Codec. The default value (for TETRA) for the Tx and Rx paths is 4 (divide by 64), giving a sample rate of 144kHz and a symbol rate of 18kHz with a 9.216MHz crystal. The default value for the Codec is 9 (divide by 1152), giving a sample rate of 8kHz with a 9.216MHz crystal.

5.3 Tx Data Path

5.3.1 FIFO

Symbol data is written to a 4-word deep FIFO. The status of the FIFO can be monitored by the **Status1** register. This register can be used to issue an interrupt once a certain number of full or empty locations exist within the FIFO. When the serial clock stop mode is enabled, writing data to the FIFO will stop the serial clock once the FIFO is full. Words written to the FIFO can contain either one or four symbols to be transmitted. Absolute constellation positions can also be written, by bypassing the symbol modulator.

5.3.2 Modulator

This takes the 2-bit symbols, performs a Gray code conversion and uses a recursive adder to generate a 3-bit code representing the eight possible phase states. A look up table provides the digitally encoded I and Q values for each phase state.

5.3.3 Filters

Digital filtering is applied to the data by two FIR filters. The first has 79 taps and provides stop band rejection and sampling correction. This filter takes data from the modulator at the symbol rate (18kHz for Tetra) and interpolates by 8 to the sample rate (144kHz for Tetra). The CMX981 has a mode that allows data to be written directly to this filter at either rate. The second filter has 63 taps and provides the primary Root Raised Cosine (RRC) shaping with a roll-off factor (α) of 0.35. These filters contain default coefficients at power up, but can be overwritten via the serial interface.

5.3.4 Gain Control

The amplitude of each channel can be adjusted independently. The gain multiplier provides a resolution of 11 bits; i.e. the gain is adjustable in steps of 1/2048 of the maximum level. Additional logic allows a mode of operation that will enable ramping up to the set signal level, stay at this value while instructed by the user, then ramp down to zero.

5.3.5 Phase Pre-distortion

A further feature allows the user to compensate for non-orthogonal carrier phase in the external quadrature modulator by adding a programmable fraction of up to 1/8 of the filtered I and Q channel signals to each other immediately prior to the DAC input.

5.3.6 Offset Adjustment

Offset registers allow any offsets introduced in the analogue sections of the transmit path to be corrected digitally via the serial interface. The offset adjust is independently applied to each of the I and Q channel. The adjustment range is plus and minus full scale. Thus care must be exercised by the user to avoid excessive offsets being applied to the sigma-delta DAC.

5.3.7 Output Ramping

A facility is provided to allow ramping of the outputs in two modes. When enabled by the user, the signal from the gain multiplier stage is multiplied by an envelope value. This value increments or decrements at a rate programmed by the user. The ramping envelope can be selected by the user to be linear or sigmoidal. A sigmoidal ramp will minimise spectrum spread while fast ramping is in progress.

5.3.8 Sigma-Delta D-A Converters and Reconstruction Filters

The converters are designed to have low distortion and >80dB dynamic range. These 2nd order converters operate at a frequency of 128x symbol rate so as to over-sample the data at their inputs a further 16 times. The reconstruction filters are 3rd order, switched capacitor, low pass filters designed to work in conjunction with an external RC.

5.4 Rx Data Path

5.4.1 Anti-Alias Filtering and Sigma-Delta A-D Converters

The sampling frequency of the Sigma-Delta A-D is 128x symbol rate. The high over-sampling rate relaxes the design requirements on the anti-alias filter. However, to achieve optimum performance, the anti-alias filter must reject the sampling frequency to about -110dB, of which at least 30dB must be provided externally. Additionally, in order to ease the complexity of the subsequent digital filters, there is a further requirement that the external anti-alias filter suppress 8x symbol rate to about -13dB. The on-chip anti-alias filter can be by-passed and powered down, although external anti-aliasing must then be provided. The fourth-order Sigma-Delta A-D converters are designed to have low distortion and >90dB dynamic range. The baseband I and Q channels must be provided as differential signal; this minimises in-band pick up both on and off the chip.

Both I and Q Sigma-Delta converters produce a single bit output sampled at MCLK/4. This data is passed to a non-programmable decimation FIR filter, which is sampled at MCLK/4 and gives sufficient rejection at 8x symbol rate (MCLK/64) to permit decimation to that frequency. Note that around -30dB is provided by the primary anti-alias filters.

5.4.2 Rx FIR Filters

Digital filtering is applied to the data from the Sigma-Delta A-D converter decimation filter by two 63-tap FIR filters in cascade. The default coefficients are set to give a RRC response with α of 0.35. The first filter is used to enhance stop-band rejection, while the second filter provides the primary shaping requirement for RRC response.

5.4.3 I and Q Channel Gain

Programmable gain modules are provided in both I and Q channels. These blocks allow the user to adjust the dynamic range of the received data within the digital filters, thus optimising the filter signal to noise performance for a range of levels at the Rx input pins. In the receive section the gain multiplier sign bit is user accessible, therefore phase inversion in each channel is possible by programming negative numbers into the gain registers.

The two channels are independently programmable. This enables differential gain corrections to be made within the digital domain.

5.4.4 Offset Registers

System generated offsets may be removed by control of the offset register via the serial interface.

5.5 Auxiliary Circuits

5.5.1 10-bit DACs

Four 10-bit DACs are provided to assist in a variety of control functions. The DACs are designed to provide an output as a proportion of the supply voltage, depending on the digital input. They are monotonic with an absolute accuracy of better than 1%. Control and data for these come via the serial interface.

5.5.2 10-bit ADC

A 10-bit ADC is provided to assist in a variety of measurement and control functions. The ADC includes an internal sample and hold circuit and is designed to produce a digital output proportional to the input voltage, full scale being the positive supply. It is monotonic with an absolute accuracy of about 1%. An input multiplexer allows the input to be selected from one of six sources. Control and digital data output is via the serial interface.

5.5.3 Power Ramping and Control

One of the DACs has an additional feature that enables a set of values to be sequenced out at a pre-selected frequency. This is aimed at enabling power ramping of a RF output with a suitable profile. The sequence may be reversed for power down. The sequence of values is stored in a dedicated RAM, which can be loaded via the serial interface.

5.6 Voice Codec

5.6.1 Data Interface

Data is read from and written to the voice codec at the codec sample clock (8kHz). This clock signal can be routed to either the *SymbolClock* or *N_IRQ2* pins by programming the **IRQCtrl** register. It is also possible to set this signal as a latched interrupt in the **Status2** register. When the sample clock goes high or the codec data ready interrupt is generated, the codec has read transmit data from the **CodecData** register and written receive data to it. This data must be read and new data written before the next codec sample clock.

5.6.2 Microphone Inputs

The analogue input amplifier selects between two differential microphone sources. This amplifier has a selectable 20dB gain and a mute option.

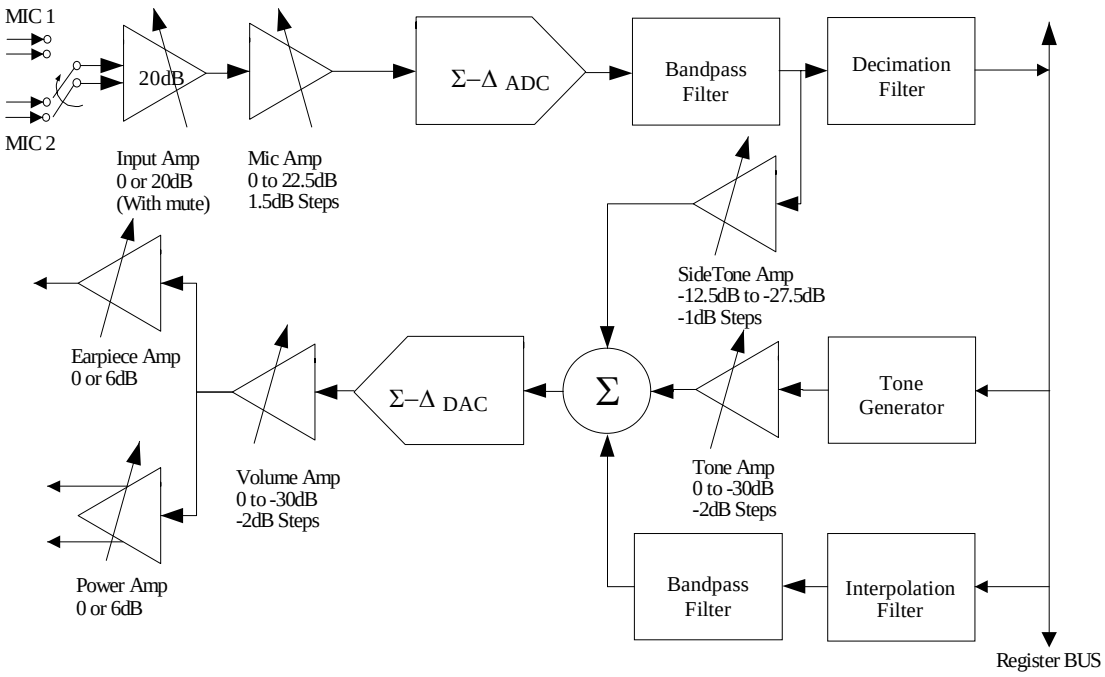


Figure 3 Voice Codec Block Diagram

5.6.3 Microphone Amplification

The microphone input signal is passed through a variable gain amplifier. The gain of this amplifier is selectable between 0 and 22.5dB in 1.5dB steps via the **CodecGain1** register.

5.6.4 Encoder Filtering

The analogue input signal is passed through an ADC and then a digital bandpass filter. The highpass function of this filter is selectable. The filtered signal is then decimated to 8kHz, and can be read via the serial interface. See figure 4.

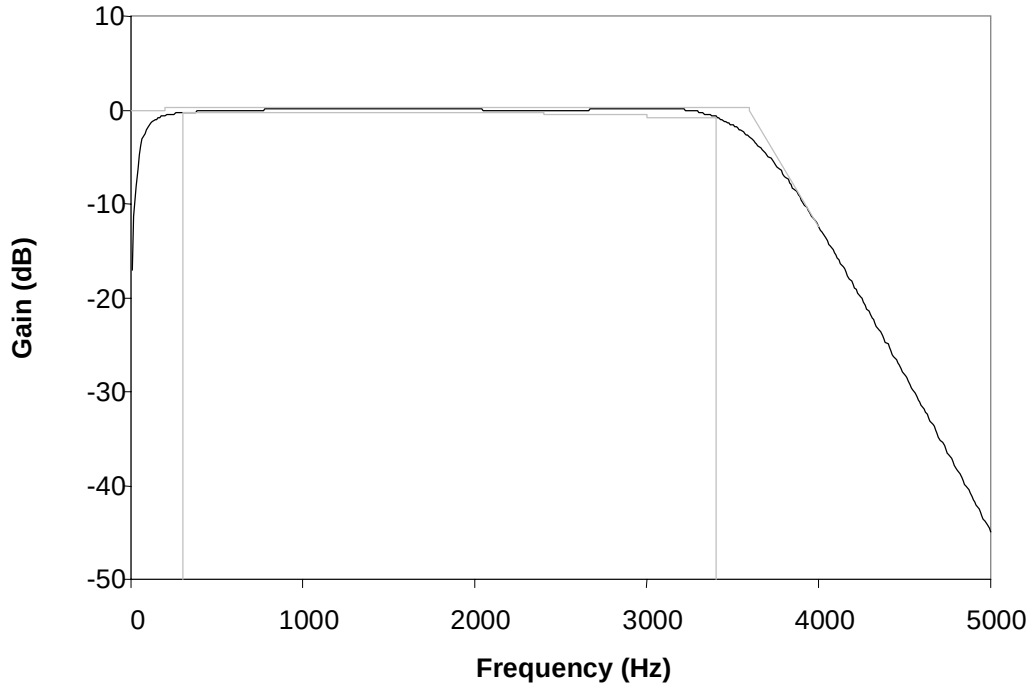


Figure 4 Voice Codec Filter Response

5.6.5 Tone Generator

The tone generator can be enabled by setting bit 1 of the **CodecSetup2** register. The frequency of the tone is controlled by the **CodecToneFreq** register, and is variable from 0 to 4kHz in approximately 0.5Hz increments.

5.6.6 Decoder Filtering

The data written via the serial interface is interpolated to 32kHz, and passed through the same filter as described in section 5.6.4. The sidetone and ring tone are added to the decoder signal. The decoder signal can be disabled at this point.

5.6.7 Output Amplification

The decoded signal is converted to an analogue signal using a sigma delta converter. The output of this converter is passed through a variable gain amplifier. The gain of this amplifier is selectable between 0 and -30dB in -2dB steps via the **CodecGain1** register.

5.6.8 Output Drivers

The decoded analogue signal is driven off the CMX981 via either a differential speaker driver or a single-ended earpiece driver. The integrated speaker driver is capable of driving 130mW into an 8Ω load and the integrated earpiece driver is capable of driving 16.5mW into a 32Ω load.

Note that due to the low operating voltage and high currents when driving 130mW, care should be taken to minimise the resistance in the CMX981 to speaker connections in order to achieve full rated power.

5.7 Serial Interface

All digital data I/O and control functions for the CMX981 are via the serial interface. The device has three serial interface ports. Two of these are dedicated fast serial buses (FSBs), the other is selectable between an FSB and C-BUS interface, under control of the CBUSEN pin.

Cmd1 (*CmdFS1/CCLK*, *CmdDat1/CDATA*, *CmdRdFS1/CSN*, *CmdRdDat1/RDATA* pins)

FSB mode (CBUSEN held low)

Read and write commands can be issued on this port using the CmdFS1 and CmdDat1 pins. Read data is returned on the CmdRdFS1 and CmdRdDat1 pins. The CmdDat1 pin can be configured as an open drain bi-directional I/O pin for reading.

C-BUS mode (CBUSEN held high)

Read and write commands can be issued on this port using the CCLK, CDATA and CSN pins. Read data is returned on the RDATA pin.

Cmd2 (*CmdFS2*, *CmdDat2*, *CmdRdFS2*, *CmdRdDat2* pins)

Read and write commands can be issued on this port using the CmdFS2 and CmdDat2 pins. Read data is returned on the CmdRdFS2 and CmdRdDat2 pins.

TxRx (*TxFS*, *TxDat*, *RxFS*, *RxDat* pins)

Only write commands can be issued on this port using the TxFS and TxDat pins. The RxFS and RxDat pins normally issue receive data, but can be configured to return read data requested from Cmd1 and Cmd2. It is envisaged that this port will be used for writing Tx data to the FIFO and reading Rx data.

FSB Operation

The three interfaces share a common serial clock pin. The serial clock rate is selectable between MCLK, MCLK/2 and MCLK/4 in the ConfigCtrl1 register.

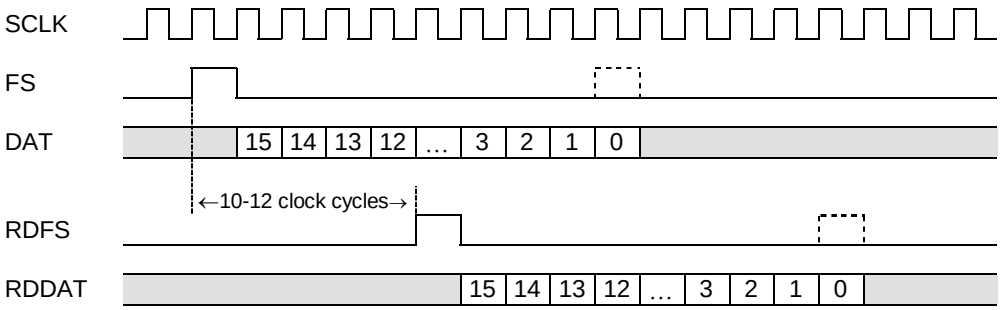


Figure 5 FSB Operation

Write commands (CmdDat1, CmdDat2 and TxDat pins)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	Address							Write data							

Read commands (CmdDat1 and CmdDat2 pins)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Normal mode	0	Address							Ignored bits							
CmdDat1 in bidirectional mode	0	Address							Read data							

Response to read command (CmdRdDat1, CmdRdDat2 and RxDat pins)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Address							Read data							

Write commands are issued by setting the first bit transmitted high (bit 15). All three ports can write to any address (except read only locations). Write commands issued on the Tx port will be executed before Cmd1 port commands, which will be executed before Cmd2 port commands, if more than one write command is issued simultaneously.

Read commands are issued by setting the first bit transmitted low (bit 15). Read commands issued by the Tx port are ignored. Read commands issued on the Cmd1 port will be executed before Cmd2 port commands, if two read commands are issued simultaneously.

The Rx port is used mainly for the output of I and Q received data. When data reception is enabled, I and Q received data will be output at 8x the symbol rate. If the serial clock rate is set to MCLK/4 and RxClkDivRate<8, data will be output at 4x the symbol rate. In this mode, alternate samples are discarded. 16-bit data words are output from alternate channels (I channel first). To facilitate channel identification of the serial data, should initial synchronisation be lost, the CMX981 has an I/Q channel identification mode, which is controlled by setting bit 5 in the RxSetup1 register. Enabling this mode causes the LSB of the Q channel to be a logic "1", while the LSB of the I channel is a logic "0" for seven samples out of eight. The eighth sample is a logic "1" and coincides with the internal symbol clock. Note that if the sample rates of the receive and transmit paths are different, the LSB of the I channel will always be a logic "0".

C-BUS Operation

When the CBUSEN pin is set high, Cmd port 1 is configured as a C-BUS interface.

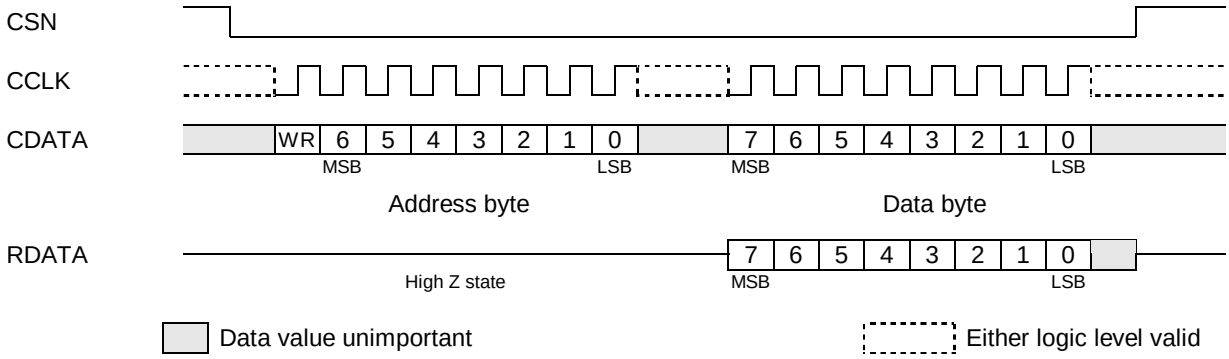


Figure 6 C-BUS Operation

Notes:

1. The CDATA and RDATA lines are never active at the same time. The WR bit determines the data direction for each C-BUS transfer - high being a write transaction, low being a read transaction.
2. The CCLK input can be high or low at the start and end of each C-BUS transaction.
3. The gap shown between the address and data bytes is optional. The user may insert gaps or concatenate the data as required.

Data on the CDATA line is clocked into the CMX981 on the rising edge of the CCLK input. The reply data sent from the CMX981 is valid when the CCLK input is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common μC serial interfaces and may also be easily implemented with general purpose μC I/O pins controlled by a simple software routine.

5.8 Interrupt Function

Two interrupt request (IRQ) pins (N_IRQ1 and N_IRQ2) are provided for asynchronous communication with an external processor. Some examples of operation that may generate an interrupt are:

1. An attempt is made by the user to write to the Tx FIFO when it is full.
2. An internal arithmetic overflow has occurred in an FIR filter.
3. The voice codec has just written a new output sample and requires a new input sample.

The IRQ feature may also be used to establish the phasing of the received I and Q channel data from the Rx serial port should synchronisation be lost for any reason.

In order for these pins to generate interrupts, the user must first program which status register(s) will cause interrupts on which pin(s). This is done using the **IRQCtrl** register. Each status register has an associated mask register, which is used to select which bits of each register causes interrupt. The cause of an IRQ can be obtained by reading the status registers. All possible causes of an interrupt are masked on reset. Mask status can be altered by writing to the IRQ mask register.

5.9 Transmission of Data

The eight points in the DQPSK constellation each have a magnitude of 1 and are spaced at 45° intervals around the unit circle. The default operating mode modulates two bit symbols into the TETRA constellation by representing each symbol as a phase change, according to the following mapping, where the left hand bit is considered as the first bit of the symbol and corresponds to bit 0, 2, 4 or 6 of the data word written to the FIFO.

Symbol		Phase change
Bit 0, 2, 4 or 6	Bit 1, 3, 5 or 7	
1	1	-135°
0	1	+135°
0	0	+45°
1	0	-45°

When writing to the FIFO with the symbol modulator active, bit 8 of the data word controls the format of the word. If this bit is set low, the symbol modulator will encode one symbol per word written to the FIFO. Therefore, data words are read from the FIFO at 18kHz. If the bit is set high, the symbol modulator encodes four symbols per word, and data words are read from the FIFO at 4.5kHz.

If the symbol modulator is bypassed, the FIFO word is interpreted as an absolute constellation position given by the table below.

Bit code	000	001	010	011	100	101	110	111
I	1	0.7071	0	-0.7071	-1	-0.7071	0	0.7071
Q	0	0.7071	1	0.7071	0	-0.7071	-1	-0.7071

Bit 9 of each data word (regardless of whether the modulator is bypassed or not) controls the initiation, ramp up, ramp down and termination of a transmission frame. The user initiates a transmit frame by enabling bit 3 in the **TxSetup** register. However, internal transmission of the data will not occur until a data word is read from the FIFO with the ramp up bit set (bit 9). This read occurs at the symbol clock. The symbol clock can be automatically adjusted to the next sample clock by setting bit 7 in the **TxSetup** register when enabling the transmit path. This effectively allows transmission to start on the next sample clock. Therefore, there is a variable delay between enabling the transmit data path and transmission starting. The user may poll the transmit path enabled bit in the **Status1** register to establish when transmission has started. The ramping feature has a built in delay equal to the latency of the default FIR filter coefficients. This delay can be varied by use of the **RampCtrl** register.

To relieve the user of polling overheads when waiting for Tx frame completion, an interrupt can be set up to occur when the transmit path is disabled.

Data Interlock Mechanisms

There are four possible transmission data interlock mechanisms. It is recommended that the user always uses one of these methods.

- Software polling
- Serial clock when ready
- Interrupt data demand
- Internally generated frame sync

Software polling requires the user to first check that the FIFO is not full before writing each TxData word. This may be accomplished by inspecting the relevant FIFO status bits before writing one or more data words.

The *serial clock when ready* mode is a hardware interlock mechanism. This mechanism allows the user to write data words without doing any FIFO checks: the hardware handshake is implemented by stopping the serial port clock when the FIFO is full. This mechanism should be used with care, because stopping the clock will freeze all other serial port transfers, including access to the voice codec, auxiliary data converters and receive data. Note that since the C-BUS interface is driven from an external clock, it can still be used to access the CMX981.

Interrupt data demand is used to request data when the FIFO has reached a defined level. An interrupt can be generated when the data in the FIFO reaches the level specified in the **Status1** register.

The *internally generated frame sync* mode configures the TxFS pin as an output. Frame sync pulses will appear on this pin while the transmit path is enabled and the FIFO is not full. In this way, a hardware interlock mechanism is implemented without having to stop the serial clock. The user must respond to a TxFS signal by supplying TXDAT data to the timings given in section 7.1.3. Should a frame sync pulse be generated by the CMX981 before the user has data ready to transmit to the FIFO, a dummy read operation should be issued on the Tx serial port (MSB set low). This will prevent a possible spurious write operation as no action is taken for Tx serial port reads.

5.9.1 Direct Write to 79-tap Filter Mode

The FIFO and DQPSK modulator may be bypassed, allowing the user direct access to the Tx filter chain input. The 79-tap filter is normally used to interpolate from the symbol rate to the sample rate. However, in direct write mode, the user may select the input rate of the filter as either symbol or sample rate.

5.9.2 Test Access to DAC Input

A mechanism to allow read and write access to DAC input data is provided for use in testing or in other systems where the modulator and filter blocks are not required. Data written to the access points will be transferred to the DAC logic at the next internal sample clock after the data is written to the register. Write operations to the upper and lower byte register of I and Q channels must be synchronised in phase by the user to the internal sample clock. This is to avoid splitting the I and Q channel or upper and lower bytes into different samples. The internal sample clock can be programmed to appear on either the *SymbolClock* or *N_IRQ1* pins by programming the **ConfigCtrl1** and **IRQCtrl** registers.

Note that data input at this point will have to be pre-filtered to compensate for the reconstruction filter droop (approximately 2dB at MCLK/1024), which is normally compensated by the internal FIR default coefficients.

5.10 Symbol Clock Phase Adjustment

In order to comply with the Tetra requirement to maintain the phase error between the mobile station (MS) and the base station (BS) symbol clocks to less than 1/4 symbol time, a mechanism to allow phase adjustment of the CMX981 symbol clock is provided.

This phase adjustment is achieved by writing a command to the **SymClkPhase** register, which will adjust the symbol clock phase from -4/8 to +3/8 of a symbol period. It is intended that the user determines the symbol clock phase of the BS after clock recovery has been performed on the received data. Then, allowing for the fixed Tx path delay, the CMX981 phase can be advanced or retarded so that it is within the specified error limit. The internal symbol clock phase is normally output on the SymClock pin, but can also be output on the N_IRQ1 and N_IRQ2 pins if required by unmasking the symbol clock enable interrupt in the **Mask2** register. Alternatively, the I/Q channel identification mode can be used (see section 5.7). This places the symbol clock in the Rx I channel LSB. Thus via hardware or software means the internal Tx symbol clock reference time can be determined and the phase with respect to the BS adjusted.

5.11. Auto Power Save Mode

By setting bit 1 of the **ClkStopCtrl** register, the serial interface will enter an automatic power down mode. In this mode, if no serial port activity on any input frame sync pin is detected after a time out (TMO) period the serial interface will enter a standby state. In this state all master clock activity within the interface is stopped (to reduce power to a minimum) and the SCLK pin stops in the high state. It will remain in this state until the user asserts a frame sync pin for at least one MCLK cycle time, when normal serial port activity will recommence and serial port operation can continue as normal. Subsequent periods of TMO without frame sync activity will cause the serial interface to enter the power down mode again. The use of this mode does not affect C-BUS operations.

The time out period TMO is between 6 and 7 Tx symbol periods (333 and 389μs with an 18kHz symbol clock).

When in the power down state and the SCLK pin is high, frame syncs may be asserted asynchronously, but when the SCLK restarts, subsequent frame sync strobes must respect the timing constraints given in the timing section of this document. The serial interface is stopped in the state where it tests the frame sync pins for a high state, so restarting from this point by asserting a frame sync pin will begin a serial operation cycle in the interface logic.

Applying global reset whilst in the power down state will return the device to normal serial mode.

The use of this mode is only available in low data rate mode (SCLK = MCLK/4), as this mode is envisaged for use in low speed/power applications. However, systems that use higher data rates can make use of this facility by setting a low data rate before enabling this mode, then returning to the higher data rate after powering up the serial interface again.

5.12 Software Description

		Control and Set-up Registers	
$00	ConfigCtrl1	Configuration control register 1	Read/Write
$01	ConfigCtrl2	Configuration control register 2	Read/Write
$02	IRQCtrl	Interrupt control register	Read/Write
$03	TxSetup	Transmit set-up register	Read/Write
$04-$07	TxData	Transmit data FIFO register	Write only
$08	RxSetup1	Receive set-up register 1	Read/Write
$09	RxSetup2	Receive set-up register 2	Read/Write
		Status and Interrupt Registers	
$0A	Status1	Status register 1	Read only
$0B	Mask1	Interrupt mask register 1	Read/Write
$0C	Status2	Status register 2	Read only
$0D	Mask2	Interrupt mask register 2	Read/Write
$0E	Status3	Status register 3	Read only
$0F	Mask3	Interrupt mask register 3	Read/Write
		Miscellaneous Registers	
$10	SymClkPhase	Symbol clock phase adjustment register	Read/Write
$11	ClkStopCtrl	Clock stop control register	Read/Write
$12	PowerDownCtrl	Power down control register	Read/Write
$13	LoopBackCtrl	Loop back control register	Read/Write
$14	RamDacCtrl	Auxiliary RAM DAC control register	Read/Write
$15	AuxAdcCtrl1	Auxiliary ADC control register 1	Read/Write
$16	AuxAdcCtrl2	Auxiliary ADC control register 2	Read/Write
$17	RampCtrl	Transmit path ramping delay register	Read/Write
$18-$1F	CoeffRamData	Coefficient memory I/O access addresses	Read/Write
		Transmit Path Set-up Registers	
$20-$21	TxIPhase	Transmit I channel phase register	Read/Write
$22-$23	TxIGain	Transmit I channel gain register	Read/Write
$24-$25	TxIOffset	Transmit I channel offset register	Read/Write
$26-$27	TxQPhase	Transmit Q channel phase register	Read/Write
$28-$29	TxQGain	Transmit Q channel gain register	Read/Write
$2A-$2B	TxQOffset	Transmit Q channel offset register	Read/Write
$2C-$2D	TxRampUpInc	Transmit ramp up increment register	Read/Write
$2E-$2F	TxRampDnDec	Transmit ramp down decrement register	Read/Write

		Receive Path Set-up Registers	
$30-$31	RxIGain	Receive I channel gain register	Read/Write
$32-$33	RxIOffset	Receive I channel offset register	Read/Write
$34-$35	RxQGain	Receive Q channel gain register	Read/Write
$36-$37	RxQOffset	Receive Q channel gain register	Read/Write
		Data Access Points	
$38-$39	RxDPIData	Receive I channel data access point	Read/Write
$3A-$3B	RxDPQData	Receive Q channel data access point	Read/Write
$3C-$3D	TxDPIData	Transmit I channel data access point	Read/Write
$3E-$3F	TxDPQData	Transmit Q channel data access point	Read/Write
		Auxiliary Data Registers	
$40-$4B	AuxAdcData	Auxiliary ADC data registers	Read only
$4C-$4F	AuxRamData	Auxiliary DAC memory I/O access addresses	Read/Write
$50-$57	AuxDacData	Auxiliary DAC data registers	Write only
		Voice Codec Registers	
$58	CodecSetup1	Voice codec set-up register 1	Read/Write
$59	CodecSetup2	Voice codec set-up register 2	Read/Write
$5A	CodecGain1	Voice codec gain register 1	Read/Write
$5B	CodecGain2	Voice codec gain register 2	Read/Write
$5C-$5D	CodecToneFreq	Voice codec tone frequency register	Read/Write
$5E-$5F	CodecData	Voice codec transmit/receive data register	Read/Write
		Clock Division Registers	
$60	ClkDiv1	Clock division control register 1	Read/Write
$61	ClkDiv2	Clock division control register 2	Read/Write
		Direct Write Data Registers	
$60-$6F	DirectWrite79tapI	Transmit I channel direct write data register	Write only
$70-$7F	DirectWrite79tapQ	Transmit Q channel direct write data register	Write only

Unless otherwise stated, all register bits are set low on reset.

5.12.1 $00 ConfigCtrl1 Configuration Control Register 1

Bit	7	6	5	4	3	2	1	0
	Serial Clock Rate		Enable bidirectional mode	*SymClock* pin source select		Disable read port 1	Disable read port 2	Disable rx port

Bits 7 and 6 control the frequency of the serial clock. If the SCLK rate is insufficient to transmit all pairs of I/Q samples (SCLK = MCLK/4 and Rx sample rates higher than MCLK/128), the receive port will transmit every other pair of I/Q samples. Odd or even sample pairs may be selected via the **RxSetup1** register. Note: when these bits are changed, the serial clock frequency will not change until the next sample clock.

Bit 7	Bit 6	Frequency
0	0	MCLK/4
0	1	MCLK/2
1	0	MCLK
1	1	Reserved

Bit 4	Bit 3	Signal (default rate at MCLK=9.216MHz)
0	0	Symbol Clock (18kHz)
0	1	Tx Sample Clock (144kHz)
1	0	Codec Sample Clock (8kHz)
1	1	Rx Sample Clock (144kHz)

Bit 5 will enable the bidirectional mode on port 1. This will cause read data requested by port 1 to be returned on the *CmdDat1* pin when port1 is configured as a fast serial bus.

Bits 4 and 3 select which signal is present on the *SymClock* pin. Note that the codec sample clock is only active when the codec is enabled.

Bits 2 to 0 will tristate the frame sync and data pins of each data port when selected.

5.12.2 $01 ConfigCtrl2 Configuration Control Register 2

Bit	7	6	5	4	3	2	1	0
	Bypass Rx delay	Enable clock stop interlock mode	Enable frame sync interlock mode	Active low frame syncs	Increment Aux RAM pointer on read	Enable Aux RAM access	Increment coefficient RAM on read	Enable coefficient RAM access.

Setting bit 7 high will bypass the 1/32 symbol delay on the receive data path.

Bit 6 will enable the clock stop hardware interlock mode, stopping the serial clock when the transmit path is enabled and the FIFO is full.

Setting bit 5 high will enable the frame sync hardware interlock mode, generating frame sync signals on the TXFS pin until the FIFO is full.

Bit 4 changes the polarity of the frame sync output pins.

Setting bit 3 high will cause read operations to the auxiliary RAM to increment the address pointer. Setting this bit low causes write operations to increment the address pointer.

Bit 2 enables access to the auxiliary RAM.

Setting bit 1 high will cause read operations to the filter coefficient RAMs to increment the address pointer. Setting this bit low causes write operations to increment the address pointer.

Bit 0 enables access to the filter coefficient RAMs.

5.12.3 $02 IRQCtrl Interrupt Control Register

Bit	7	6	5	4	3	2	1	0
	Codec sample clock to *N_IRQ2*	**Status3** to *N_IRQ2*	**Status2** to *N_IRQ2*	**Status1** to *N_IRQ2*	Tx Sample clock to *N_IRQ1*	**Status3** to *N_IRQ1*	**Status2** to *N_IRQ1*	**Status1** to *N_IRQ1*

Setting bit 7 high will cause the codec sample clock to appear on the *N_IRQ2* pin. Note that the codec sample clock is only active when the codec is enabled.

Bits 6 to 4 enable interrupts generated by the status registers to appear on the *N_IRQ2* pin.

Setting bit 3 high will cause the internal transmit sample clock to appear on the *N_IRQ1* pin.

Bits 2 to 0 enable interrupts generated by the status registers to appear on the *N_IRQ1* pin.

5.12.4 $03 TxSetup Transmit Set-up Register

Bit	7	6	5	4	3	2	1	0
	Auto symbol clock adjust	Enable direct write access at sample rate	Enable direct write access	Bypass symbol modulator	Enable transmit data path	Select ramping mode	Enable ramping	Reset Tx filter coefficients

When bit 7 is set high, the internal symbol clock is adjusted to the next sample clock when the transmit path is enabled. This allows transmission of data to commence on the next sample clock. For this function to be useful, a data word must be written to the FIFO with the ramp up bit set before enabling the transmit data path.

Bit 6 will change the input sample rate of the transmit 79-tap FIR filter from the symbol rate to the sample rate for direct write access. This bit should be set low when direct write access is disabled.

Bit 5 will enable the transmit direct write access mode, allowing samples to be written directly to the transmit 79-tap FIR filter.

Bit 4 will bypass the transmit symbol modulator; thereby taking the 3 least significant bits of each transmit word written to the FIFO to represent an absolute constellation mapping.

Bit 3 enables the transmit data path, allowing transmission to start. This bit should only be cleared when the transmit path enable status bit in the **Status1** register has been cleared.

Bit 2 selects between linear ramping when set high, and sigmoidal ramping when set low.

Bit 1 enables transmit amplitude ramping (linear or sigmoidal). Setting this bit low causes the Ramp up bit of the **TxData** register to directly control the output amplitude (High meaning full amplitude, low meaning zero amplitude).

Setting bit 0 high will cause the transmit path filter coefficients to return to their default values. This bit should be set low while writing new coefficients.

5.12.5 $04-$07 TxData Transmit Data FIFO Register (Write only)

The two least significant bits of the address are used as bits 9 and 8 of the data word.

Bit	9	8	7	6	5	4	3	2	1	0
Symbol modulator not bypassed	Ramp up	Multi-symbol	Symbol 4		Symbol 3		Symbol 2		Symbol 1	
Symbol modulator bypassed	Ramp up	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	IQ Constellation point		

Bit 9 controls the ramping of the transmitted data. Setting this bit high will cause the output to ramp up to its full value. Setting this bit low will cause the output to ramp down to zero. Once the ramp down has been completed, the transmit path enable status bit in the **Status1** register is cleared, and the transmit path can be disabled.

Bit 8 controls whether one or four symbols are read from the transmit data word (when symbol modulator is not bypassed). When set high, the FIFO transmits all four symbols (starting with symbol 1). When set low, only symbol 1 is transmitted.

When in symbol modulator bypass mode, the three least significant bits directly represent which of 8 supported constellation points, all on a unit circle, is to be transmitted.

5.12.6 $08 RxSetup1 Receive Set-up Register 1

Bit	7	6	5	4	3	2	1	0
	Set Rx port 32-bit mode	Rx port sample select	Enable Rx port channel identity mode	Set Rx port LSB first	Enable receive path	Enable Rx port for read 2	Enable Rx port for read 1	Reset Rx filter coefficients

Bit 7 will cause the Rx data port to transmit 32-bit frames - I data in the MSB word, Q data in the LSB word.

Bit 6 is used to select which samples are transmitted when the serial clock is set to MCLK/4 and the Rx sample rate is greater than MCLK/128 (see **ConfigCtrl1** register description). When set high, odd numbered samples are selected (I_1, Q_1, I_3, Q_3). When set low, even numbered samples are selected (I_0, Q_0, I_2, Q_2).

Setting bit 5 causes the receive data to carry an identification bit in the LSB of the data word. The I channel is identified by a logic "0" and the Q channel by a logic "1". This therefore reduces the dynamic range of the receive data from 16 to 15 bits. See section 5.7.

Bit 4 will cause the receive path data sent by the Rx port to be sent least significant bit first.

Bit 3 enables the receive data path.

Bit 2 will enable read data requested by port 2 to be returned on the Rx port.

Bit 1 will enable read data requested by port 1 to be returned on the Rx port.

Setting bit 0 high will cause the receive path filter coefficients to return to their default values. This bit should be set low while writing new coefficients.

5.12.7 $09 RxSetup2 Receive Set-up Register 2

Bit	7	6	5	4	3	2	1	0
	Q channel decimation filter sample delay				I channel decimation filter sample delay			

These values control the sampling point in the receive decimation filter. The values are 4-bit 2's complement integers. The sampling point can therefore be adjusted by -8/16 to 7/16 of the sample clock period.

5.12.8 $0A Status1 Status Register 1 (Read only)

Bit	7	6	5	4	3	2	1	0
	Transmit path enable	FIFO under read	FIFO over write	FIFO not full	FIFO nearly full	FIFO nearly empty	FIFO empty	FIFO IRQ active

Bit 7 indicates that the transmit path is active. The transmit path enable bit in the TxSetup register should not be cleared until this bit is set low. An interrupt is generated when this bit is set low (if unmasked in the **Mask1** register).

Bit 6 is set high when a read occurs from an empty FIFO.

Bit 5 is set high when a write occurs to a full FIFO.

Bit 4 is set high when the FIFO contains one or more empty locations.

Bit 3 is set high when the FIFO contains three full locations and one empty location.

Bit 2 is set high when the FIFO contains one full location and three empty locations.

Bit 1 is set high when the FIFO is empty.

Bit 0 is set high when a status bit in this register causes an interrupt.

Some of these status conditions are caused by transitory events, therefore their active state (low for bit 7, high for bits 6 to 0) is latched. Reading this register resets the latches. Note that bits 7 and 4 to 1 are only latched if the corresponding bit in the **Mask1** register is unmasked.

5.12.9 $0B Mask1 Interrupt Mask Register 1

Bit	7	6	5	4	3	2	1	0
	Unmask transmit path enable	Unmask FIFO under read	Unmask FIFO over write	Unmask FIFO not full	Unmask FIFO nearly full	Unmask FIFO nearly empty	Unmask FIFO empty	Not used. Set low.

Setting any of these bits high will unmask the corresponding interrupts in the **Status1** register.

5.12.10 $0C Status2 Status Register 2 (Read only)

Bit	7	6	5	4	3	2	1	0
	Not used. Undefined on read.	Codec data ready	Transmit Q channel overflow	Transmit I channel overflow	Symbol clock enable	Transmit 63-tap filter overflow	Transmit 79-tap filter overflow	Transmit IRQ active

Bit 6 is set high when the voice codec writes a data sample to the **CodecData** register.

Bit 5 is set high when an overflow occurs in the gain, phase and offset adjustment block for the Q channel.

Bit 4 is set high when an overflow occurs in the gain, phase and offset adjustment block for the I channel.

Bit 3 is the internal symbol clock enable signal. When bit 3 in **Mask2** is set high, this signal is unmasked and appears on an interrupt pin.

Bit 2 is set high when an overflow occurs in the transmit 63-tap filter.

Bit 1 is set high when an overflow occurs in the transmit 79-tap filter.

Bit 0 is set high when a status bit in this register causes an interrupt.

These status conditions are caused by transitory events, therefore all bits (except bit 3) are latched in their active state until the register is read.

5.12.11 $0D Mask2 Interrupt Mask Register 2

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Unmask codec data ready	Unmask transmit Q channel overflow	Unmask transmit I channel overflow	Unmask symbol clock enable	Unmask transmit 63-tap filter overflow	Unmask transmit 79-tap filter overflow	Not used. Set this bit low.

Setting any of these bits high will unmask the corresponding interrupts in the **Status2** register.

5.12.12 $0E Status3 Status Register 3 (Read only)

Bit	7	6	5	4	3	2	1	0
	Not used. Undefined on read	Receive Q channel overflow	Receive I channel overflow	Decimation filter overflow	Rx low-pass filter overflow	Rx RRC filter overflow	Even sample phase	Rx IRQ active.

Bit 6 is set high when an overflow occurs in the gain and offset block for the Q channel.

Bit 5 is set high when an overflow occurs in the gain and offset block for the I channel.

Bit 4 is set high when an overflow occurs in the receive path decimation filter.

Bit 3 is set high when an overflow occurs in the receive path low-pass filter.

Bit 2 is set high when an overflow occurs in the receive path root-raised-cosine filter.

When bit 1 is high, the associated interrupt may be used to re-synchronise the Rx data if for any reason data synchronisation is lost. If the corresponding bit in **Mask3** is unmasked, an interrupt will be generated on the next I phase data. The next pulse on *RxFS* indicates the start of I channel data. This interrupt should then be masked to prevent continuous I phase interrupts.

Bit 0 is set high when a status bit in this register causes an interrupt.

These status conditions are caused by transitory events, therefore all bits are latched in their active state until the register is read.

5.12.13 $0F Mask3 Interrupt Mask Register 3

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Unmask Q channel overflow	Unmask I channel overflow	Unmask decimation filter overflow	Unmask Rx low-pass filter overflow	Unmask Rx RRC filter overflow	Unmask even sample phase	Not used. Set this bit low.

Setting any of these bits high will unmask the corresponding interrupts in the **Status3** register.

5.12.14 $10 SymClkPhase Symbol Clock Phase Adjustment Register

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low	Not Used. Set this bit low	Not Used. Set this bit low	Not Used. Set this bit low	Not Used. Set this bit low	Phase change		

Any write operation to this register will cause the symbol clock phase to change by the value written in bits 2 to 0. A read operation will return the last phase change value written to this register.

Bit 2	Bit 1	Bit 0	Phase change
0	0	0	No phase change
0	0	1	Retard 1/8 symbol
0	1	0	Retard 1/4 symbol
0	1	1	Retard 3/8 symbol
1	0	0	Advance 1/2 symbol
1	0	1	Advance 3/8 symbol
1	1	0	Advance 1/4 symbol
1	1	1	Advance 1/8 symbol

5.12.15 $11 ClkStopCtrl Clock Stop Control Register

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low	Not Used. Set this bit low	Set Tx auto clock stop mode	Enable FIFO clock	Stop receive port clock	Stop Aux clock	Set serial interface auto clock stop mode	Set Rx auto clock stop mode

Bit 5 will cause the transmit path enable bit (bit 3 of the **TxSetup** register) to gate the transmit path master clock.

Setting bit 4 high will disable the transmit FIFO clock, reducing power consumption. Ensure this bit is set low before commencing FIFO operations.

Bit 3 will power down the receive data port when the receive path is inactive.

Bit 2 will power down the auxiliary RAM DAC and the ADC.

Bit 1 will enable the serial interface auto clock stop mode. When set active the serial interface will power down if no frame sync activity is detected after 6-7 symbol periods. Asserting any frame sync input signal will restart the serial interface. Note: this mode is only available when the serial clock is set to MCLK/4

Bit 0 will cause the receive path enable bit (bit 3 of the **RxSetup1** register) to gate the receive path master clock.

5.12.16 $12 PowerDownCtrl Power Down Control Register

Bit	7	6	5	4	3	2	1	0
	Reserved. Set this bit low.	Reserved. Set this bit low.	Set pins fast	Enable analogue bias chain	Power up Aux DAC4	Power up Aux DAC3	Power up Aux DAC2	Power up Aux DAC1

Setting bit 5 high will speed up the digital outputs, reducing rise and fall times, but increasing power consumption and ground bounce.

Setting bit 4 high will enable the analogue bias chain. This bit should be set high at least 2ms before enabling the Aux ADC, Tx, Rx or codec sections.

Setting any of bits 3 to 0 high will power up the appropriate section of the device.

5.12.17 $13 LoopBackCtrl Loop Back Control Register

Bit	7	6	5	4	3	2	1	0
	Bypass Rx ADC passive filter	Reserved. Set this bit low.	Bypass IIR	Enable codec analogue loop back	Enable analogue loop back	Enable receive data path access	Enable transmit data path access	Enable digital loop back

Setting bit 7 high will bypass the Rx ADC passive filter.

Bit 5 will bypass the voice codec IIR filter allowing direct access to the ADC/DAC. This option will also increase the codec sample clock to 32kHz and configure the **CodecData** register as a 16-bit interface.

Setting bit 4 high will connect the output of the codec DAC to the input of the codec ADC.

Setting bit 3 high will connect the output of the Tx DAC to the input of the Rx ADC, thus passing transmit constellation data through a raised cosine filter and allowing the resultant data samples to be monitored digitally at the Rx output.

Bit 2 will enable write access to the receive path data access point.

Bit 1 will enable write access to the transmit path data access point.

Setting bit 0 high will connect the output of the Tx path data operator to the Rx port. Data is taken from the I and Q channels alternately. Note that, as in normal non-loopback mode, I and Q data is output at 4 times the symbol rate (every other sample) when SCLK is set to MCLK/4.

5.12.18 $14 RamDacCtrl Auxiliary RAM DAC Control Register

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	RAM DAC scan rate			Scan direction	Enable auto cycle scan	Enable RAM DAC

Bits 5 to 3 control the rate at which the RAM DAC address pointer changes.

Bit 5	Bit 4	Bit 3	Rate of change
0	0	0	MCLK/512
0	0	1	MCLK/256
0	1	0	MCLK/128
0	1	1	MCLK/64
1	0	0	MCLK/32
1	0	1	MCLK/16
1	1	0	MCLK/8
1	1	1	MCLK/4

Bit 2 controls the direction of the memory scan operation. Setting this bit high will cause the memory address pointer to increment to the top location. Setting this bit low will cause the memory address pointer to decrement to the bottom location. If this bit is changed while the memory is being scanned, the current scan will complete before the new state of this bit takes effect.

When bit 1 is set high, the memory address pointer continuously increments to the top location and then decrements to the bottom location.

Bit 0 controls whether the DAC1 is driven by the RAM (when set high) or the AuxDacData1 register (when set low).

5.12.19 $15 AuxAdcCtrl1 Auxiliary ADC Control Register 1

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Enable ADC 6	Enable ADC 5	Enable ADC 4	Enable ADC 3	Enable ADC 2	Enable ADC 1

This register controls which ADC channels are converted. These bits may be changed at any time, but will only update the active state of the ADC channel for the next time it is converted.

5.12.20 $16 AuxAdcCtrl2 Auxiliary ADC Control Register 2

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Select conversion rate	Enable continuous conversion	Start conversion

Bit 2 selects the conversion rate of the ADC. If set low, the ADC will be clocked at MCLK/8, giving a conversion time of 88 MCLK periods per enabled channel. Setting this bit high halves the ADC clock rate and doubles the conversion time.

Setting bit 1 high will cause each enabled channel to be converted continuously.

Setting bit 0 high will cause a single conversion of all enabled channels. This bit is automatically set low when the conversion has been completed. Note that this bit only has an effect when bit 1 is set low.

The auxiliary ADC automatically powers down when inactive. When enabled, the ADC requires two conversion periods to power up.

5.12.21 $17 RampCtrl Transmit Path Ramping Delay Register

Bit	7	6	5	4	3	2	1	0
	Disable default delay	Number of samples delay time						

When bit 7 is set low, the default ramp delay time is used (75 samples). When bit 7 is set high, the number stored in bits 6 to 0 is used.

5.12.22 $18-$1F CoeffRamData Coefficient Memory I/O Access Addresses

$18

Bit	7	6	5	4	3	2	1	0
	Transmit RRC Filter Coefficient [7:0]							

$19

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit RRC Filter Coefficient [11:8]			

$1A

Bit	7	6	5	4	3	2	1	0
	Transmit 79-tap Filter Coefficient [7:0]							

$1B

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit 79-tap Filter Coefficient [11:8]			

$1C

Bit	7	6	5	4	3	2	1	0
	Receive RRC Filter Coefficient [7:0]							

$1D

Bit	7	6	5	4	3	2	1	0
	Receive RRC Filter Coefficient [15:8]							

$1E

Bit	7	6	5	4	3	2	1	0
	Receive Low Pass Filter Coefficient [7:0]							

$1F

Bit	7	6	5	4	3	2	1	0
	Receive Low Pass Filter Coefficient [15:8]							

Setting bit 0 in the **ConfigCtrl2** register enables access to the coefficient RAMs, and resets the coefficient pointer to the first location. In order to program new coefficients, the most significant bits of each word must be written first ($19, $1B, $1D, $1F). When the least significant bits of each word are written, the whole word is stored in the RAM and the coefficient pointer is incremented to the next location (if bit 1 in **ConfigCtrl2** is low).

5.12.23 $20-$21 TxIPhase Transmit I Channel Phase Register

For write access, the least significant bit of the address is used as bit 8 of the data word.

Bit	8	7	6	5	4	3	2	1	0
	Transmit I channel phase [8:0]								

The value written to this register controls the proportion of the Q channel amplitude that is added to the I channel:

$I_{out} = I_{in} + Q_{in} * [G_{val} / 2^{11}]$ where: I_{out} is the I channel output, I_{in} is the I channel input, Q_{in} is the Q channel input, and G_{val} is the register value.

This causes a phase change of:

$\phi = \tan^{-1} [G_{val} / 2^{11}]$ where: ϕ is the phase adjustment, and G_{val} is the register value.

The value of this register is in 2's complement format. A positive value in this register will cause the I channel phase to be advanced, while a negative value will cause the phase to be retarded.

For read access, two read commands must be issued.

$20

Bit	7	6	5	4	3	2	1	0
	Transmit I channel phase [7:0]							

$21

Bit	7	6	5	4	3	2	1	0
	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Transmit I channel phase [8]

5.12.24 $22-$23 TxIGain Transmit I Channel Gain Register

$22

Bit	7	6	5	4	3	2	1	0
	Transmit I channel gain [7:0]							

$23

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit I channel gain [11:8]			

The value written in this register is used to control the gain of the transmitted data. The equation for this is:

$D_{out} = D_{in} * [G_{val} / 2^{11}]$ where: D_{out} is the signal output, D_{in} is the signal input, and G_{val} is the register value.

The value of this register is in 2's complement format, allowing phase inversion.

5.12.25 $24-$25 TxIOffset Transmit I Channel Offset Register

$24

Bit	7	6	5	4	3	2	1	0
	Transmit I channel offset [7:0]							

$25

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit I channel offset [11:8]			

The value written in this register controls the signal offset. The equation for this is:

$$D_{out} = D_{in} + [N_{off} / 2^{11}]$$

where: D_{out} is the signal output.
D_{in} is the signal input, and
N_{off} is the register value.

The value of this register is in 2's complement format. Inappropriate values may cause arithmetic overflow.

5.12.26 $26-$27 TxQPhase Transmit Q Channel Phase Register

For write access, the least significant bit of the address is used as bit 8 of the data word.

Bit	8	7	6	5	4	3	2	1	0
	Transmit Q channel phase [8:0]								

The value written to this register controls the proportion of the I channel amplitude that is added to the Q channel to adjust the phase.

$$Q_{out} = Q_{in} + I_{in} * [G_{val} / 2^{11}]$$

where: Q_{out} is the Q channel output,
Q_{in} is the Q channel input,
I_{in} is the I channel input, and
G_{val} is the register value.

This causes a phase change of:

$$\phi = \tan^{-1} [- G_{val} / 2^{11}]$$

where: ϕ is the phase adjustment, and
G_{val} is the register value.

The value of this register is in 2's complement format. A positive value in this register will cause the Q channel phase to be retarded, while a negative value will cause the phase to be advanced.

For read access, two read commands must be issued.

$26

Bit	7	6	5	4	3	2	1	0
	Transmit Q channel phase [7:0]							

$27

Bit	7	6	5	4	3	2	1	0
	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Transmit Q channel phase [8]

5.12.27 $28-$29 TxQGain Transmit Q Channel Gain Register

$28

Bit	7	6	5	4	3	2	1	0
	Transmit Q channel gain [7:0]							

$29

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit Q channel gain [11:8]			

The value written in this register is used to control the gain of the transmitted data. The equation for this is:

$$D_{out} = D_{in} * [G_{val} / 2^{11}]$$

where: D_{out} is the signal output,
D_{in} is the signal input, and
G_{val} is the register value.

The value of this register is in 2's complement format, allowing phase inversion.

5.12.28 $2A-$2B TxQOffset Transmit Q Channel Offset Register

$2A

Bit	7	6	5	4	3	2	1	0
	Transmit Q channel offset [7:0]							

$2B

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit Q channel offset [11:8]			

The value written in this register controls the signal offset. The equation for this is:

$$D_{out} = D_{in} + [N_{off} / 2^{11}]$$

where: D_{out} is the signal output.
D_{in} is the signal input, and
N_{off} is the register value.

The value of this register is in 2's complement format. Inappropriate values may cause arithmetic overflow.

5.12.29 $2C-$2D TxRampUpInc Transmit Ramp Up Increment Register

For write access, the least significant bit of the address is used as bit 8 of the data word.

Bit	8	7	6	5	4	3	2	1	0
	Transmit ramp up increment [8:0]								

The value of this register sets the scale of the transmit amplitude gain increments which occur over each sample period, thus determining the amplitude ramp up time. The value is always positive. The ramp up time, in number of symbols is:

$N_{sym} = 64 / N_{inc}$ where: N_{sym} is the ramp time in number of symbols, and N_{inc} is the register value.

For read access, two read commands must be issued.

$2C

Bit	7	6	5	4	3	2	1	0
	Transmit ramp up increment [7:0]							

$2D

Bit	7	6	5	4	3	2	1	0
	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Transmit ramp up increment [8]

5.12.30 $2E-$2F TxRampDnDec Transmit Ramp Down Decrement Register

The least significant bit of the address is used as bit 8 of the data word.

Bit	8	7	6	5	4	3	2	1	0
	Transmit ramp down decrement [8:0]								

The value of this register sets the scale of the transmit amplitude gain decrements which occur over each sample period, thus determining the amplitude ramp down time. The value is always positive. The ramp down time, in number of symbols is:

$N_{sym} = 64 / N_{inc}$ where: N_{sym} is the ramp time in number of symbols, and N_{inc} is the register value.

For read access, two read commands must be issued.

$2E

Bit	7	6	5	4	3	2	1	0
	Transmit ramp down decrement [7:0]							

$2F

Bit	7	6	5	4	3	2	1	0
	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Not Used. Undefined on read.	Transmit ramp down decrement [8]

5.12.31 $30-$31 RxIGain Receive I Channel Gain Register

$30

Bit	7	6	5	4	3	2	1	0
	Receive I channel gain [7:0]							

$31

Bit	7	6	5	4	3	2	1	0
	Receive I channel gain [15:8]							

The value written in this register is used to control the gain of the transmitted data. The equation for this is:

$$D_{out} = D_{in} * [G_{val} / 2^{15}]$$

where: D_{out} is the signal output,
D_{in} is the signal input, and
G_{val} is the register value.

The value of this register is in 2's complement format, allowing phase inversion.

5.12.32 $32-$33 RxIOffset Receive I Channel Offset Register

$32

Bit	7	6	5	4	3	2	1	0
	Receive I channel offset [7:0]							

$33

Bit	7	6	5	4	3	2	1	0
	Receive I channel offset [15:8]							

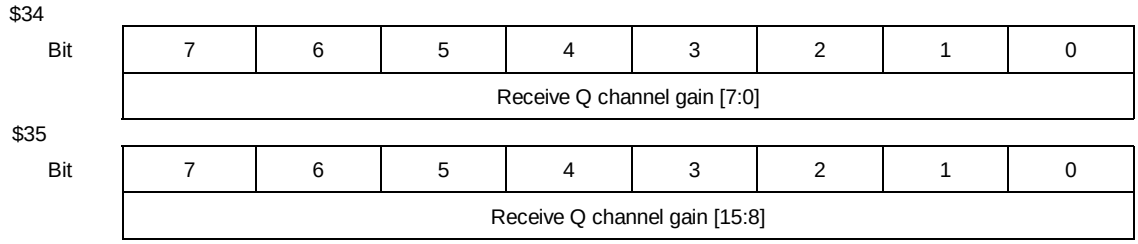
The value written in this register controls the signal offset. The equation for this is:

$$D_{out} = D_{in} + [N_{off} / 2^{15}]$$

where: D_{out} is the signal output.
D_{in} is the signal input, and
N_{off} is the register value.

The value of this register is in 2's complement format. Inappropriate values may cause arithmetic overflow.

5.12.33 $34-$35 RxQGain Receive Q Channel Gain Register



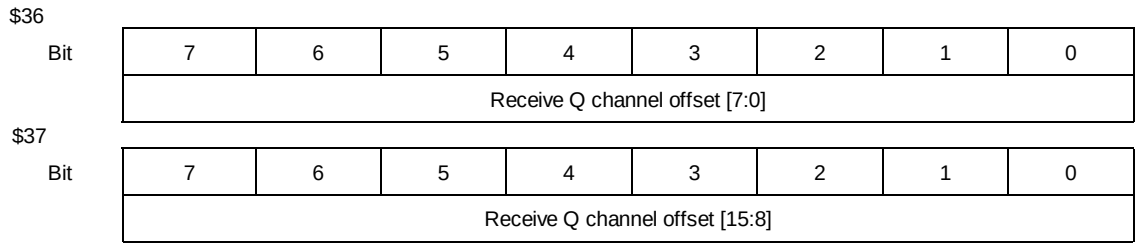
The value written in this register is used to control the gain of the transmitted data. The equation for this is:

$$D_{out} = D_{in} * [G_{val} / 2^{15}]$$

where: D_{out} is the signal output,
D_{in} is the signal input, and
G_{val} is the register value.

The value of this register is in 2's complement format, allowing phase inversion.

5.12.34 $36-$37 RxQOffset Receive Q Channel Offset Register



The value written in this register controls the signal offset. The equation for this is:

$$D_{out} = D_{in} + [N_{off} / 2^{15}]$$

where: D_{out} is the signal output.
D_{in} is the signal input, and
N_{off} is the register value.

The value of this register is in 2's complement format. Inappropriate values may cause arithmetic overflow.

5.12.35 $38-$3B RxDPData Receive Data Access Points

$38-$39	RxDPIData	Receive I Channel Data Access Point
$3A-$3B	RxDPQData	Receive Q Channel Data Access Point

$38, $3A

Bit	7	6	5	4	3	2	1	0
	Receive channel data [7:0]							

$39, $3B

Bit	7	6	5	4	3	2	1	0
	Receive channel data [15:8]							

These registers allow direct access to the receive data path values just after the gain and offset adjustment. Both read and write operations are permitted. A read operation reads the signal values on the I and Q channels. A write operation will write data to the data path operator output. To prevent normal data overwriting these values, bit 2 in the **LoopBackCtrl** register should be set. The MSB read data is buffered to enable access of a discrete sample value (if the register was not buffered, data from different sample periods could be in the MSB and LSB registers). Therefore, the LSB register must be read first for correct operation.

5.12.36 $3C-$3F TxDPData Transmit Data Access Points

$3C-$3D	TxDPIData	Transmit I Channel Data Access Point
$3E-$3F	TxDPQData	Transmit Q Channel Data Access Point

$3C, $3E

Bit	7	6	5	4	3	2	1	0
	Transmit channel data [7:0]							

$3D, $3F

Bit	7	6	5	4	3	2	1	0
	Not Used. Set this bit low.	Not Used. Set this bit low.	Transmit channel data [13:8]					

These registers allow direct access to the transmit data path values just after the gain, phase and offset adjustment. Both read and write operations are permitted. A read operation reads the signal values on the I and Q channels. A write operation will write data directly to the sigma-delta DAC input. To prevent normal data overwriting these values, bit 1 in the **LoopBackCtrl** register should be set. The MSB read data is buffered to enable access to a discrete sample value (if the register was not buffered, data from different sample periods could be in the MSB and LSB registers). Therefore the LSB register must be read first for correct operation.

5.12.37 $40-$4B AuxAdcData Auxiliary ADC Data Registers (Read only)

$40-$41	AuxAdcData1	Auxiliary ADC 1 Data Register
$42-$43	AuxAdcData2	Auxiliary ADC 2 Data Register
$44-$45	AuxAdcData3	Auxiliary ADC 3 Data Register
$46-$47	AuxAdcData4	Auxiliary ADC 4 Data Register
$48-$49	AuxAdcData5	Auxiliary ADC 5 Data Register
$4A-$4B	AuxAdcData6	Auxiliary ADC 6 Data Register

$40, $42, $44, $46, $48, $4A

Bit	7	6	5	4	3	2	1	0
	Not used. Bit value undefined	Not used. Bit value undefined	Not used. Bit value undefined	Not used. Bit value undefined	Not used. Bit value undefined	Not used. Bit value undefined	ADC Data [1:0]	

$41, $43, $45, $47, $49, $4B

Bit	7	6	5	4	3	2	1	0
	ADC Data [9:2]							

These registers enable the user to inspect the conversion value for each of the six auxiliary ADCs. There are two read registers per ADC, one to obtain the two least significant bits of the data, the other for the eight most significant bits. Reading these registers does not affect the ADC conversion cycle. Reading the MSB register directly reads the ADC output and simultaneously causes the two bits in the LSB register to be written to a holding register. This holding register is read when the LSB register is read. This mechanism is necessary to allow the user to read MSB and LSB data from the same ADC conversion cycle. If only the MSB register is read, the converter can be considered as an 8-bit ADC. If a 10-bit conversion is required, the MSB register must be read first.

5.12.38 $4C-$4F AuxRamData Auxiliary DAC Memory I/O Access Addresses

$4C

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	RAM data [1:0]	

$4D

Bit	7	6	5	4	3	2	1	0
	RAM data [9:2]							

$4E

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	RAM data [1:0]	

$4F

Bit	7	6	5	4	3	2	1	0
	RAM data [9:2]							

These four address locations allow access to the 64 x 10-bit RAM. The contents of this RAM can be pre-loaded with a table of values that can be automatically sent to the auxiliary DAC1 in either a single cycle or continuous mode. Therefore the RAM can be used in conjunction with DAC1 to enable user defined profile power ramping of an external RF power transmitter stage.

The RAM contents are addressed incrementally by first setting bit 2 of **ConfigCtrl2** register. While this bit is low, the RAM address pointer is held reset. The first two data words are written by writing to addresses $4C to $4F in order. Accessing location $4F post-increments the address pointer. Bit 3 of the **ConfigCtrl2** register determines whether a read or write operation will increment the RAM address pointer. Further write operations to addresses $4C to $4F, will load the next two locations.

All locations are accessed incrementally; further accesses to this port while bit 3 of **ConfigCtrl2** is active are not valid and may cause data loss.

5.12.39 $50-$57 AuxDacData Auxiliary DAC Data Registers (Write only)

$50-$51	AuxDacData1	Auxiliary DAC 1 Data Register
$52-$53	AuxDacData2	Auxiliary DAC 2 Data Register
$54-$55	AuxDacData3	Auxiliary DAC 3 Data Register
$56-$57	AuxDacData4	Auxiliary DAC 4 Data Register

$50, $52, $54, $56

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	DAC Data [1:0]	

$51, $53, $55, $57

Bit	7	6	5	4	3	2	1	0
	DAC Data [9:2]							

There are two input registers for each of the four auxiliary DACs. Writing to the LSB register ($50, $52, $54 and $56) writes the two least significant bits of DAC data. Writing to the MSB register ($51, $53, $55 and $57) writes the eight most significant bits of DAC data and then passes all ten bits to the appropriate DAC input. If the MSB register is written while the LSB register is left constant, the converter may be treated as an 8-bit DAC.

5.12.40 $58 CodecSetup1 Voice Codec Set-up Register 1

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Select output amplifier		Disable output 6dB gain	Disable input 20dB gain	Mute input signal	Select mic input

Bits 5 and 4 selects which output amplifier is enabled. It is not possible to enable both amplifiers simultaneously. The amplifiers automatically power down when disabled.

Bit 5	Bit 4	Amplifier
0	0	None
0	1	Earpiece
1	0	Speaker
1	1	Reserved

Bits 3 selects between 6 dB gain (when set low) and 0 dB gain (when set high) on the analogue output stage.

Bit 2 selects between 20 dB gain (when set low) and 0 dB gain (when set high) on the analogue input stage.

Setting bit 1 high will mute the analogue input.

Bit 0 is used to select which microphone input is fed into the voice codec, low meaning Mic1, high meaning Mic2.

5.12.41 $59 CodecSetup2 Voice Codec Set-up Register 2

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low.	Not used. Set this bit low.	Not used. Set this bit low.	Disable high pass filtering	Enable voice codec	Enable sidetone	Enable ring tone	Enable transmit signal

Setting bit 4 high will disable high pass filtering.

Setting bit 3 high enables the voice codec data path. The voice codec automatically powers down when this bit is set low.

Bit 2 enables the sidetone circuit.

Bit 1 enables the ring tone generator.

Bit 0 enables the voice signal on the digital to analogue path.

5.12.42 $5A CodecGain1 Voice Codec Gain Register 1

Bit	7	6	5	4	3	2	1	0
	Input gain				Output gain			

The values in this register control the gain of the input and output amplifiers for the voice codec.

Bit 7	Bit 6	Bit 5	Bit 4	Input Gain (dB)
0	0	0	0	0
0	0	0	1	1.5
0	0	1	0	3.0
0	0	1	1	4.5
0	1	0	0	6.0
0	1	0	1	7.5
0	1	1	0	9.0
0	1	1	1	10.5
1	0	0	0	12.0
1	0	0	1	13.5
1	0	1	0	15.0
1	0	1	1	16.5
1	1	0	0	18.0
1	1	0	1	19.5
1	1	1	0	21.0
1	1	1	1	22.5

Bit 3	Bit 2	Bit 1	Bit 0	Output Gain (dB)
0	0	0	0	0
0	0	0	1	-2
0	0	1	0	-4
0	0	1	1	-6
0	1	0	0	-8
0	1	0	1	-10
0	1	1	0	-12
0	1	1	1	-14
1	0	0	0	-16
1	0	0	1	-18
1	0	1	0	-20
1	0	1	1	-22
1	1	0	0	-24
1	1	0	1	-26
1	1	1	0	-28
1	1	1	1	-30

5.12.43 $5B CodecGain2 Voice Codec Gain Register 2

Bit	7	6	5	4	3	2	1	0
	Tone gain				Sidetone gain			

The values in this register control the amplitude of the ring tone generator and the sidetone path.

Bit 7	Bit 6	Bit 5	Bit 4	Tone Gain (dB)
0	0	0	0	0
0	0	0	1	-2
0	0	1	0	-4
0	0	1	1	-6
0	1	0	0	-8
0	1	0	1	-10
0	1	1	0	-12
0	1	1	1	-14
1	0	0	0	-16
1	0	0	1	-18
1	0	1	0	-20
1	0	1	1	-22
1	1	0	0	-24
1	1	0	1	-26
1	1	1	0	-28
1	1	1	1	-30

Bit 3	Bit 2	Bit 1	Bit 0	Sidetone Gain (dB)
0	0	0	0	-12.5
0	0	0	1	-13.5
0	0	1	0	-14.5
0	0	1	1	-15.5
0	1	0	0	-16.5
0	1	0	1	-17.5
0	1	1	0	-18.5
0	1	1	1	-19.5
1	0	0	0	-20.5
1	0	0	1	-21.5
1	0	1	0	-22.5
1	0	1	1	-23.5
1	1	0	0	-24.5
1	1	0	1	-25.5
1	1	1	0	-26.5
1	1	1	1	-27.5

5.12.44 $5C-$5D CodecToneFreq Voice Codec Tone Frequency Register

$5C

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low	Not used. Set this bit low	Not used. Set this bit low	Tone Frequency [12:8]				

$5D

Bit	7	6	5	4	3	2	1	0
	Tone Frequency [7:0]							

The value in this register controls the frequency of the ring tone generator, given by the equation:

$F = N_{val} / 2.048$ Hz where: F is the frequency of the generated tone, and N_{val} is the register value.

5.12.45 $5E-$5F CodecData Voice Codec Transmit/Receive Data Register

$5E

Bit	7	6	5	4	3	2	1	0
	Codec Data [7:0]							

$5F

Bit	7	6	5	4	3	2	1	0
	Not used. Set this bit low	Not used. Set this bit low	Codec Data [13:8]					

Writing to this register passes data to the voice codec decode path. Reading from this register returns the latest sample from the voice codec encode path.

5.12.46 $60 ClkDiv1 Clock Division Control Register 1

Bit	7	6	5	4	3	2	1	0
	Transmit Clock Divide Ratio				Receive Clock Divide Ratio			

This register is only accessible when bit 5 of the **TxSetup** register is set low. The values in this register control the frequencies of the transmit and receive path sample clocks..

Bit 7	Bit 6	Bit 5	Bit 4	Transmit Clock Divide Ratio	Transmit Sample Clock Rate	Transmit Symbol Clock Rate
Bit 3	Bit 2	Bit1	Bit 0	Receive Clock Divide Ratio	Receive Sample Clock Rate	
0	0	0	0	4	MCLK/64	MCLK/512
0	0	0	1	5	MCLK/80	MCLK/640
0	0	1	0	6	MCLK/96	MCLK/768
0	0	1	1	7	MCLK/112	MCLK/896
0	1	0	0	8	MCLK/128	MCLK/1024
0	1	0	1	9	MCLK/144	MCLK/1152
0	1	1	0	10	MCLK/160	MCLK/1280
0	1	1	1	11	MCLK/176	MCLK/1408
1	0	0	0	12	MCLK/192	MCLK/1536
1	0	0	1	13	MCLK/208	MCLK/1664
1	0	1	0	14	MCLK/224	MCLK/1792
1	0	1	1	15	MCLK/240	MCLK/1920
1	1	0	0	16	MCLK/256	MCLK/2048
1	1	0	1	Reserved	Reserved	Reserved
1	1	1	0	Reserved	Reserved	Reserved
1	1	1	1	Reserved	Reserved	Reserved

5.12.47 $61 ClkDiv2 Clock Division Control Register 2

Bit	7	6	5	4	3	2	1	0
	Not Used Set this bit low.	Not Used Set this bit low.	Not Used Set this bit low.	Not Used Set this bit low.	CODEC Clock Divide Ratio			

This register is only accessible when bit 5 of the **TxSetup** register is set low. This register resets to $07 (divide by 9), giving an 8kHz codec sample clock rate with a 9.216MHz Xtal. The value in this register controls the sample frequency of the voice codec.

Bit 3	Bit 2	Bit 1	Bit 0	Codec Clock Divide Ratio	Codec Sample Clock Rate
0	0	0	0	16	MCLK/2048
0	0	0	1	15	MCLK/1920
0	0	1	0	14	MCLK/1792
0	0	1	1	13	MCLK/1664
0	1	0	0	12	MCLK/1536
0	1	0	1	11	MCLK/1408
0	1	1	0	10	MCLK/1280
0	1	1	1	9	MCLK/1152
1	x	x	x	8	MCLK/1024

5.12.48 $60-$7F DirectWrite79tap Transmit Path Direct Write Data Register (Write only)

$60-$6F	DirectWrite79tapI	Transmit Path Direct Write Data Register (I)
$70-$7F	DirectWrite79tapQ	Transmit Path Direct Write Data Register (Q)

The four least significant bits of the address are used as bits 11 to 8 of the data word.

Bit	11	10	9	8	7	6	5	4	3	2	1	0
	Direct Write Data [11:0]											

These registers are only accessible when bit 5 in the **TxSetup** register is set high. These registers are the direct access points to the 79-tap filter inputs.

6. Application Notes

6.1 Interrupt Handling

Interrupt handling requires an extra read to clear the source of the interrupt. Handling interrupts is sometimes a source of confusion. The notes below are intended to clarify the operation of interrupts:

Tx FIFO Status Interrupts

These interrupts can only be cleared by first carrying out the appropriate action to stop the source of the Tx FIFO interrupt (this would usually require writing some data to the Tx FIFO) and then carrying out a further read on the **Status1** register to reset the N_IRQ1 (or N_IRQ2) pin.

Tx/Rx FIR filter overflow, and gain, phase and offset overflow interrupts

A typical interrupt handling procedure for Tx (the same can be applied to Rx) would be:

- Read the **Status2** register and confirm that a Tx FIR filter error has occurred.
- This will reset the N_IRQ1 (or N_IRQ2) pin.

Rx ADC I and Q channel overflow - due to excessive input amplitude interrupts

These interrupts will remain set until the source of the excessive amplitude has been reduced to below the acceptable level. Once this has been achieved, the **Status3** register can be read in order to reset the interrupt pin.

6.2 Developing and Optimising FIR Filter Coefficients

If it is required to re-optimise FIR filter coefficients for a different application, or to compensate for the behaviour of components external to the CMX981, the default coefficients can be overwritten. There are many ways to develop FIR filter coefficients for a non-TETRA application.

The basic algorithm is to take the required frequency domain response, apply an inverse Fourier transform and use a windowing function to reduce the impulse response to the desired length. The impulse response is then identical to the required FIR coefficients. In the case of the CMX981, both transmit and receive filters are configured as two cascaded filters. When developing customised coefficients, the user has a choice of whether to design the two filters separately or to develop a single filter and then factorise the resultant polynomial in z (representing the impulse response of the overall FIR filter) into two shorter polynomials of appropriate length. Various commercial and public domain software is available which may help with this process.

In order to develop optimal FIR filter coefficients for the CMX981, knowledge of the non-programmable filters in the design is required, together with a more detailed understanding of the function of certain external components. Please refer to the block diagram in figure 1 and the external components diagrams in figures 2a and 2b.

The combined effect of all of the filters in the Tx or Rx, when using default FIR coefficients, is to give a linear phase root raised cosine filter shape, with a symbol rate of MCLK/512 and $\alpha = 0.35$. This tracks fairly well with MCLK frequency, provided that the dominant external RC poles (R3/C3 for Tx, R2/C2 for Rx, as shown in figure 2a and 2b) are also scaled with MCLK. For the case of MCLK = 8.192MHz, this means increasing the RC products by approximately 10%.

There is a small attenuation caused by two pole on-chip continuous time filters in both the Tx and Rx, which do not scale with MCLK. This will cause attenuation at 10kHz of between 0.05dB and 0.15dB in the Rx, and between 0.03dB and 0.08dB in the Tx. This effect can be ignored in many applications, but is described here for completeness. The Rx filter can be bypassed by setting bit 7 in the **LoopBackCtrl** register.

6.3 Tx Path Details

Data can be input via the DQPSK modulator or via the direct write port.

I and Q data is passed through the following elements:

1. A pair of programmable FIR filters (79-tap and 63-tap).
2. A gain/phase/offset adjustment block.
3. A matched pair of sigma delta DACs
4. A switched capacitor data reconstruction filter (which requires one external RC pole).
5. A two pole continuous time active filter which suppresses clock noise. This has a fixed pole frequency of 140kHz (subject to ±40% tolerance for process variations). It has no significant effect on the passband for all allowable MCLK frequencies, but the level of clock noise suppression supplied by this filter (48dB for MCLK = 9.216MHz) is reduced at lower MCLK frequencies.

The reconstruction filter has significant attenuation in the passband, with the following characteristic (including the external RC):

MCLK/Freq	0	4608	2304	1536	1152	1024	922
Attenuation (dB)	0	0.1	0.4	0.9	1.6	2.1	2.6

This attenuation is compensated in the default filter coefficients by convolving the required FIR response with a 15-tap pre-emphasis FIR filter. The reconstruction filter and the FIR filters will track with the MCLK frequency, provided that the external RC is scaled in proportion. The FIR filter approximately cancels the reconstruction filter attenuation up to a frequency of MCLK/900.

Coefficients for the pre-emphasis FIR filter used in the default filter coefficients are shown below.

-0.00737876
-0.00987614
-0.0150585
-0.0206503
-0.0260154
-0.0304823
-0.0334478
1.22444
-0.0334478
-0.0304823
-0.0260154
-0.0206503
-0.0150585
-0.00987614
-0.00737876

If there is no source of attenuation or phase distortion external to the IC for which the user wishes to compensate, this filter can be combined with the main shaping filter as described in section 6.2. If there are additional sources of attenuation or phase distortion, these can be catered for either by designing a new pre-emphasis filter that incorporates gain to compensate for the attenuation in the above table, or by designing another compensating filter and cascading with the filter described here. Both approaches are essentially equivalent.

6.4 Rx Path Details

The I and Q Rx data paths are nominally identical and consist of the following elements:

1. A continuous time anti-alias filter, which can be bypassed (two poles at 100kHz, Q = 0.5 on-chip and one pole at 34kHz off-chip), with the following characteristics:

MCLK/Freq	0	4608	2304	1536	1152	920
Attenuation (dB)	0	0.03	0.13	0.29	0.52	0.77

   Note: the 34kHz pole is responsible for around 60% of the passband attenuation. The two on-chip poles attenuate by approximately 0.1dB at 10kHz (equivalent to MCLK/922 for MCLK = 9.216MHz), while the decimation filter supplies 0.2dB at this frequency. Only the decimation filter attenuation will track with MCLK, while the other poles will remain fixed (subject to component tolerances). There is an 800ns variation in nominal group delay of this decimation filter up to 10kHz. This could be compensated in the FIR coefficients if considered significant.
2. A sigma delta ADC and decimation filter.
3. A gain/offset adjustment block.
4. A pair of programmable FIR filters (both 63-tap).

The passband attenuation caused by the Rx AAF and decimation filters is compensated in the default filter coefficients by convolving the required FIR response with a 15-tap pre-emphasis FIR filter. It approximately cancels the filter attenuation up to a frequency of 10kHz. This pre-emphasis FIR filter will track with the MCLK frequency, unlike the Rx AAF, but performance should be adequate for MCLK frequencies between 7MHz and 12MHz. The user is free to alter the external RX filter and/or to bypass the two on-chip poles of the AAF. In either case, the compensation FIR filter may require adjustment. In the event of a user designing their own Rx AAF, it is suggested that close attention is paid to the effect of component tolerances.

Two example sets of coefficients for this filter, for MCLK frequencies of 9.216MHz and 8.192MHz, are given below. These assume that external components R2 and C2 are NOT changed from the default values.

MCLK = 9.216MHz	MCLK = 8.912MHz
-0.00113692	0
-0.00227383	-0.00112409
-0.00568459	-0.00449636
-0.00909534	-0.00899271
-0.0147799	-0.0134891
-0.0193276	-0.0191095
-0.0227383	-0.0224818
1.16307	1.14994
-0.0227383	-0.0224818
-0.0193276	-0.0191095
-0.0147799	-0.0134891
-0.00909534	-0.00899271
-0.00568459	-0.00449636
-0.00227383	-0.00112409
-0.000113692	0

6.5 Procedure For Reconfiguring FIR Filters

1. Obtain or design the required filter characteristic(s), either in s- or z-transform format. Note that all programmable FIR filters are sampled at a frequency of MCLK/64 by default. This is equivalent to 144kHz for MCLK = 9.216MHz and 128kHz for MCLK = 8.192MHz.

The task may be made slightly easier if the desired filter specification can be split into two filters of roughly similar complexity, but if this is not possible, or if it is preferable to treat the desired filter as a single entity, then a single impulse response can be considered as a polynomial in Z and factorised into two polynomials of appropriate length.

The Tx 79-tap filter MUST have symmetrical (hence linear phase) coefficients, but all of the 63-tap filters allow asymmetrical coefficients. Hence any prototype filter function aimed at the Tx 79-tap filter must be linear phase.

2. Obtain the impulse response of the desired filter shape, either by simulation of the filter response to an impulse, or by using an inverse Fourier transform. Convolve the impulse response with the impulse response of the appropriate compensation filter described above. This may be accomplished either by concatenating the filters and simulating the impulse response of the combined system, or by multiplying the Z transfer function polynomials together.

3. Use a standard windowing function (e.g. Blackman, Hamming) to limit the impulse response to 141 samples for the Tx, 125 samples for the Rx, or 79 and 63 samples (Tx), 63 and 63 samples (Rx), if designing the filters separately. Alternatively, it may be possible to approximate small outer coefficients to zero.

4. Scale the FIR coefficients to appropriate values. To maximise the use of dynamic range, scale the dc gain to give values similar to those given by the default coefficients (approximately 4.5x for Tx and 1.6x for Rx). Note that 16-bit coefficients are used in Rx filters, but only 12-bit for Tx filters, while the use of appropriate dc gains within the system may result in one or two of the most significant bits being redundant.

5. Load in your new coefficients, run the chip with maximum sized signals and check for internal overflows (see **Status2** and **Status3** registers). Optimise individual filter gains to a level at least 5% below those which cause overflows.

6.6 Guidelines for use of Powersave Modes

The CMX981 contains a number of powersave modes. In order to maximise flexibility for architectures and modes of operation, several register bits are available which control different parts of the device. Operation of the various control bits is described in the appropriate sections. These guidelines provide an overview of the powersaving features.

6.6.1 Auxiliary Section

When one or more Auxiliary DACs are not required, they can be individually powered down using bits 3 to 0 of the **PowerDownCtrl** register.

When the auxiliary ADC channels are not required, the ADC will automatically power down if no ADC channel is selected. If ADC conversions are only required occasionally, these can be performed in single shot mode - the ADC will automatically power down between conversions.

When neither auxiliary channels nor the RAM DAC are required, the auxiliary section digital logic can be powered down using bit 2 of the **ClkStopCtrl** register.

Note that the auxiliary ADC will power up within 2 conversion periods, while the DAC circuits will power up in less than 5μs.

6.6.2 Tx Section

The Tx section can be powered down by setting bits 5 and 4 in the **ClkStopCtrl** register, and disabling the transmit path (bit 3 of **TxSetup**). Note that the transmit path should not be disabled until the transmit path active status bit in the **Status1** register has been cleared.

The power up time for the Tx section is limited by the filter response time. Thus the analogue circuitry will be correctly biased to receive data by the time the data emerges from the digital filters.

6.6.3 Rx Section

The Rx section can be powered down by setting bits 3 and 0 in the **ClkStopCtrl** register, and disabling the receive path (bit 3 of **RxSetup1**).

All of the analogue circuitry within the Rx will power up within 10μs. Thus, the time from power up to valid data appearing at the RxDat pin will be dominated by the digital filter group delay (nominally 8 symbol periods).

6.6.4 Voice Codec

The voice codec section powers down automatically when disabled (bit 3 of the **CodecSetup2** register set low). The output amplifiers are powered down by setting bits 5 and 4 of the **CodecSetup1** register low.

The voice codec section takes 1 sample (288/MCLK) to power up.

6.6.5 Bias Section

When the Voice codec, Tx, Rx and Aux ADC are powered down, a small amount of current can be saved by clearing bit 5 of the **PowerDownCtrl** register. This bit powers down the analogue bias chain. However, this causes the voltage on the BIAS1 pin, which is used as the internal "analogue ground", to move towards VDD with a 250μs time constant. Up to 2ms should be allowed for this node to recover before enabling the Aux ADC or Tx, Rx, codec sections.

6.6.6 Serial Interface

A small power saving can be made if it is possible to run with a serial interface clock rate of MCLK/4. Note that this reduces the Rx output rate to four samples per symbol, although symbol timing can still be adjusted using bit 6 of the **RxSetup1** register and the vernier control in the **RxSetup2** register.

When running with a low serial interface clock rate, it is possible to invoke the serial interface clock stop mode by setting bit 1 of the **ClkStopCtrl** register. When this mode is active, all FSB serial interface activity will stop if there is no activity on any frame sync pin for more than 7 symbol clock periods.

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply			
V_{DDIO} - V_{SSD}	-0.3	4.5	V
V_{DDTX} - V_{SSTX}	-0.3	3.5	V
V_{DDRX} - V_{SSRX}	-0.3	3.5	V
V_{DDAUX} - V_{SSAUX}	-0.3	3.5	V
V_{DDVC} - V_{SSVC}	-0.3	3.5	V
V_{DDPA} - V_{SSPA}	-0.3	3.5	V
V_{DDD} - V_{SSD}	-0.3	3.5	V
Voltage on any pin to any V_{SS}	-0.3	V_{DDIO} + 0.3	V
Current into or out of any V_{DD} and V_{SS} pin	-30	30	mA
Current into or out of any other pin	-20	20	mA
Voltage differential between power supplies:			
V_{DDTX}, V_{DDRX}, V_{DDAUX}, V_{DDVC}, V_{DDPA} and V_{DDD}	0	0.3	V
V_{SSTX}, V_{SSRX}, V_{SSAUX}, V_{SSVC}, V_{SSPA} and V_{SSD}	0	50	mV

64-pin VQFN Package (Q1)	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		1275	mW
... Derating		15	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

Supply Limits

	Notes	Min.	Max.	Units
Supply				
V_{DDIO} - V_{SSD}		2.25	3.6	V
V_{DDTX} - V_{SSTX}		2.25	2.75	V
V_{DDRX} - V_{SSRX}		2.25	2.75	V
V_{DDAUX} - V_{SSAUX}		2.25	2.75	V
V_{DDVC} - V_{SSVC}		2.25	2.75	V
V_{DDPA} - V_{SSPA}		2.25	2.75	V
V_{DDD} - V_{SSD}		2.25	2.75	V
Operating Temperature		-40	+85	°C
MCLK Frequency - (nominally 9.216MHz)		0.5	12.5	MHz

Input/Output Levels

	Notes	Min.	Max.	Units
Inputs: (VDDIO = 2.25V - 3.6V)				
Cmos Inputs				
Logic 1 (VIH)		70%	-	Vdd
Logic 0 (VIL)		-	30%	Vdd
Outputs (VDDIO = 2.7V - 3.6V)				
Logic 1 (VOH)	I_{OH} = 2mA	80%	-	Vdd
Logic 0 (VOL)	I_{OL} = -3mA	-	0.4	V
Outputs (VDDIO = 2.25V - 2.7V)				
Logic 1 (VOH)	I_{OH} = 1.7mA	80%	-	Vdd
Logic 0 (VOL)	I_{OL} = -2.5mA	-	0.4	V

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 9.216MHz, Tx Sample Rate = Rx Sample Rate = 144kHz,
Voice Codec Sample Rate = 8kHz, Codec speaker and earpiece drivers disabled.
V_{DDIO} - V_{SSD} = V_{DDD} - V_{SSD} = V_{DDTX} - V_{SSTX} = V_{DDRX} - V_{SSRX} = V_{DDAUX} - V_{SSAUX} = V_{DDVC} - V_{SSVC} = V_{DDPA} - V_{SSPA} = 2.25V to 2.75V.
Tamb = - 40°C to +85°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters (MCLK not toggled)					
I_{DD} (Tx powersaved)	1		7.0	11.0	mA
I_{DD} (Rx powersaved)	1		6.5	10.0	mA
I_{DD} (Aux powersaved)	1		10.0	15.0	mA
I_{DD} (Codec powersaved)	1		8.0	12.0	mA
I_{DD} (All powersaved)	1		-	50.0	µA
I_{DD} (Not powersaved)	1		10.5	16.0	mA
AC Parameters (MCLK at 9.216MHz)					
I_{DD} (Tx powersaved)	1		17.0	22.0	mA
I_{DD} (Rx powersaved)	1		12.0	16.0	mA
I_{DD} (Aux powersaved)	1		22.0	28.0	mA
I_{DD} (Codec powersaved)	1		20.0	26.0	mA
I_{DD} (All powersaved except serial clock)	1		1.3	2.0	mA
I_{DD} (All powersaved)	1		1.0	1.5	mA
I_{DD} (Not powersaved)	1		23.0	30.0	mA
MCLK Input					
'High' pulse width	2	30.0			ns
'Low' pulse width	2	35.0			ns
Input impedance (at 100Hz)		10.0			MΩ

Notes:
1. Not including any current drawn from the device pins by external circuitry.
2. Timing for an external input to the MCLK pin.

General Points:

3. The current quoted when MCLK is not toggled is essentially analogue current (digital current is negligible in this case), while the current quoted when MCLK is toggled is a combination of analogue and digital current.
4. The bias chain must be powered up in order to power up the Aux ADC, Tx, Rx and Codec sections, but NOT the auxiliary DACs. It is recommended that the bias chain is powered up at least 1ms before powering up the Aux ADC, Tx, Rx or Codec. Powering down the bias chain reduces current by 10-15µA
5. Currents in other modes can be calculated from the above figures. For example, operation with Tx and auxiliary sections powersaved:
   From the table, auxiliary current is approximately 1.0mA (23.0 - 22.0mA).
   Subtracting this from Tx powersaved current (17.0mA) gives a predicted current of 16.0mA.
6. Supply currents for other MCLK frequencies can be calculated by assuming the analogue current is constant and the digital current is proportional to MCLK frequency.

Transmit Parameters

Parameter	Notes	Min.	Typ.	Max.	Units
External capacitive load				100	pF
External resistive load		30			kΩ
Input bit rate (2 bits per symbol)			MCLK/256		bps
Number of channels			2		
Modulation type			π/4 DQPSK		
FIR filter sampling rate			MCLK/64		Hz
DAC output update rate			MCLK/4		Hz
DAC resolution			14		Bits
Integral accuracy				±2	LSB
Differential accuracy				±1	LSB
Signal to noise plus distortion	1	65.0	70.0		dB
Offset (without adjustment)			±10.0	±20.0	mV
Gain matching, I to Q (without adjustment)				±0.25	dB
Phase matching, I to Q				±0.5	Degrees
Storage time	2			20.0	Symbols
I, Q output level	3	2.1	2.2	2.3	V
Adjacent channel power	4				
at MCLK/384 frequency offset			-70.0	-68.0	dBc
at MCLK/192 frequency offset			-78.0	-76.0	dBc
at MCLK/128 frequency offset			-80.0	-78.0	dBc
at MCLK/96 frequency offset			-88.0	-86.0	dBc
at MCLK/48 frequency offset			-90.0	-88.0	dBc
at MCLK/20 frequency offset			-92.0	-90.0	dBc
TETRA Specific Parameters					
Gain matching, (I or Q) to ideal Tx (normalised, 0 – 9kHz)				±0.3	dB
RRC Roll-off coefficient (α)			0.35		
|H(f)| 0 - 5.85kHz		-0.1	0.0	+0.1	dB
|H(f)| at 9kHz		-2.9	-3.0	-3.1	dB
|H(f)| at 10.05kHz		-6.6	-6.8	-7.0	dB
|H(f)| at 12.15kHz		-30.0			dB
Adjacent Channel Power	5				
at 25kHz frequency offset			-72.0	-70.0	dBc
at 50kHz frequency offset			-80.0	-78.0	dBc
at 75kHz frequency offset			-82.0	-80.0	dBc
at 100kHz frequency offset			-90.0	-88.0	dBc
at 200kHz frequency offset			-93.0	-91.0	dBc
at 500kHz frequency offset			-95.0	-93.0	dBc
at 5MHz frequency offset			-104	-102	dBc

Parameter	Notes	Min.	Typ.	Max.	Units
TETRA Specific Parameters (continued)					
Adjacent Channel Power during ramping over 5 symbols at 25kHz frequency offset					
Linear Ramping			-55.0	-53.0	dBc
Sigmoidal Ramping			-60.0	-57.0	dBc
Vector Error (peak)	6		0.045	0.070	

Tx Notes:

1. Measured with an MCLK/4096 test signal in MCLK/1024 bandwidth.
2. Storage time defines the maximum number of symbols that can be stored during a transmit sequence and thus indicates the minimum rate at which the TX fifo requires servicing. The maximum storage condition occurs when a byte is internally transferred to the transmit register and the resulting fifo location immediately filled. There are thus 4 bytes in the fifo and 1 in the transmit register, with each byte representing 4 symbols.
3. Peak to peak, differential at maximum gain.
4. Power measured through an MCLK/460 filter centred at the stated frequency offset, relative to power measured through an MCLK/460 filter centred on the main channel, with Tx gain set to $5A7 (-3dB below maximum).
5. Power measured through an ideal RRC filter (α = 0.35) centred at the stated frequency offset, relative to power measured through an ideal RRC filter (α = 0.35) centred on the main channel, with Tx gain set to $5A7 (-3dB below maximum).
6. Vector errors are measured with ideal IF and RF sections, after gain and offset adjustment, and specified as a fraction of the nominal vector value.

General Points:

7. All parameters refer to the entire Tx baseband I and Q channels, with recommended external components and default filter coefficients, unless otherwise indicated.
8. A gain multiplier function allows independent proportional control of each channel. The multiplier is a 12-bit word for each channel, input via the serial interface, representing a value from 0 to 1. This multiplication is applied to the signals from the FIR filters.
9. Offset adjustment for each channel is available by loading a 12-bit word into the transmit offset register via the serial interface.

Receive Parameters

Parameter	Notes	Min.	Typ.	Max.	Units
Input Impedance					
(Capacitive load to V_{SSRX})				10	pF
(Source impedance should be < 1kΩ)		100			kΩ
Differential input voltage	1		2.4	2.7	V pk-pk
Signal to noise	2	88.0	92.0		dB
Signal to noise plus distortion	2	85.0	88.0		dB
3rd order intercept	3		200		V pk-pk
ADC sampling rate			MCLK/4		Hz
ADC resolution			16		Bits
Integral accuracy				±1	LSB
Differential accuracy				±1	LSB
FIR filter sampling rate (Decimation section)			MCLK/4		Hz
(RRC section)			MCLK/64		Hz
Output rate (16 bit words per channel) - selectable					
SCLK >= MCLK/2			MCLK/64		Hz
SCLK = MCLK/4			MCLK/128		Hz
Offset (without adjustment)			±10.0	±20.0	mV
Gain matching, I to Q (without adjustment, 0 - 10kHz)				±0.1	dB
Phase matching, I to Q (0 - 10kHz)				±0.5	Degrees
With internal anti-alias filter disabled:					
External anti-alias requirements	4				
at MCLK/70	5			-15.0	dB
at MCLK/4	5			-110	dB
With internal anti-alias filter enabled:					
External anti-alias requirements	6, 7				
at MCLK/70	5			-13	dB
at MCLK/4	5			-30	dB
TETRA Specific Parameters					
RRC roll-off coefficient (α)	8		0.35		
|H(f)| 0 - 5.85kHz		-0.2	0	+0.2	dB
|H(f)| at 9kHz		-2.9	-3.0	-3.1	dB
|H(f)| at 10.05kHz		-6.5	-6.9	-7.3	dB
|H(f)| at 12.15kHz		-30.0			dB
|H(f)| at 16kHz		-70.0			dB
|H(f)| >25kHz		-85.0			dB

Rx Notes:

1. Note this means ±0.6V on each input of the differential pair.

The input voltages specified are at a suppy voltage of 2.5V. The typical and maximum input voltage range is directly proportional to VDDRX and should be scaled accordingly.

2. Measured with MCLK/4096 test signal, in MCLK/1024 bandwidth using the typical input voltage at a supply of 2.5V VDDRX.
3. Extrapolated from third harmonic distortion at maximum signal.
4. These anti-alias filter requirements can be supplied by IF channel filtering, baseband filtering or a combination of both. It is recommended that in order to maximise the performance obtained from the CMX981 for TETRA applications, at least 10dB and 25dB attenuation be provided at MCLK/70 and MCLK/4 respectively, prior to an external AGC function. Other applications may require less stringent external filtering.
5. With respect to typical input level.
6. This should be supplied by a network equivalent to Figure 2a.
7. These figures assume that 10-15dB attenuation at MCLK/4 is provided by IF channel filtering or by additional filtering at baseband. Note that the recommended configuration shown in Figure 2a includes an AGC after the 34kHz pole.
8. With default coefficients and internal anti-alias filter selected.

General Points:

9. Offset adjustment for each channel is available by loading a 16-bit word into the receive offset register via the serial interface.
10. Optimally, as much anti-alias filtering as possible should be carried out prior to any AGC function before the receive inputs. This allows the AGC to act on a reduced bandwidth signal and thereby improve the relative magnitude of the wanted part. The device has been designed to reduce the complexity of any external anti-alias filter as much as possible and a 4-pole Butterworth or 3-pole Chebyshev with a -3dB point at about MCLK/150 should be adequate. The internal anti-alias filter, if used, cannot provide the required 110dB attenuation at MCLK/4 and must be supplemented by external filtering. An example of a suitable external filter structure is shown in Figure 2a.
11. Anti-alias filter requirements quoted are for mobile station applications. For base station applications, all attenuation figures should be increased by 3dB.

Auxiliary Circuit Parameters

Parameter	Notes	Min.	Typ.	Max.	Units
DACs					
Resolution			10		Bits
Settling time to 0.5 LSB	1			10.0	μs
Output resistance				250	Ω
Integral non-linearity				±4	Bits
Differential non-linearity	2			±1	Bits
Zero error (offset)				±10.0	mV
Power (all DACs operating)				4.0	mW
Resistive load		5.0			kΩ
Output noise voltage in 30kHz bandwidth			5.0		μV rms
ADC and Multiplexed Inputs					
Resolution			10		Bits
Sample rate				MCLK/91	Hz
Conversion time	3	88/MCLK		176/MCLK	s
Integral non-linearity	4			±2	Bits
Differential non-linearity	4,5			±1	Bits
Zero error (offset)				±10	mV
A-D clock frequency		MCLK/16		MCLK/8	Hz
Input capacitance				5.0	pF
Power				1.0	mW

Auxiliary Circuit Notes:

1. Worst case large signal transition.
2. Guaranteed monotonic.
3. Conversion time = $\frac{11}{\textit{A-D clock frequency}}$, where *A-D clock frequency* is programmable to either MCLK/8 or MCLK/16, as shown in the table below:

	Minimum	Maximum
A-D Clock Frequency:	MCLK/16	MCLK/8
Conversion time:	88/MCLK	176/MCLK

   Due to latency in the control logic, the maximum sample rate is lower than this. Refer to the output rate details in the Receive Parameters section.
4. Non-linearity specified between 0.5% and 99.5% of output range.
5. No missing codes.

Voice Codec Parameters

Parameter	Notes	Min.	Typ.	Max.	Units
Digital Input					
Input sample rate			MCLK/1152		Hz
Input resolution			14		Bits
Tone Generator					
Frequency range		0		3999.5	Hz
Frequency resolution			0.488		Hz
Gain range		-30.0		0	dB
Gain resolution			2.0		dB
Harmonic distortion	1		-38.0	-35.0	dB
Analogue Output					
Gain range		-30.0		0	dB
Gain resolution			2.0		dB
Gain tolerance				0.1	dB
Speaker output impedance			95	120	mΩ
Speaker offset error				±10.0	mV
Speaker signal range		20		80	$\%V_{DD}$
Earpiece output impedance			95	120	mΩ
Earpiece offset error				±10.0	mV
Earpiece signal range		20		80	$\%V_{DD}$
Analogue Input					
Load resistance		100		550	kΩ
Signal range		20		80	$\%V_{DD}$
Offset error			±2.0	±10.0	mV
Gain range		0		22.5	dB
Gain resolution			1.5		dB
Gain tolerance				0.1	dB
Filter Characteristics					
Passband		300		3400	Hz
Passband gain	2		0.1		dB
Passband ripple (300Hz – 3000Hz)	3	-0.25		+0.25	dB
Stopband attenuation	3	40.0			dB
Crosstalk					
Codec Tx to Codec Rx / Codec Rx to Codec Tx				-80.0	dB
Codec to Rx				-80.0	dB
Codec to Tx				-80.0	dB

Voice Codec Notes:

1. For tones between 50Hz and 4kHz.
2. At 1.02kHz.
3. Relative to gain at 1.02kHz.

7.1.3 Operating Characteristics (continued)

The following timings are provisional:

Timing Parameters - Serial Ports	Marker	Min.	Typ.	Max.	Units
MCLK to SClk out - low to high	t_{cslh}	15		50	ns
MCLK to SClk out - high to low	t_{cshl}	10		35	ns
CmdDat/TxDat setup to falling edge of SClk	t_{sis}	35			ns
CmdFS/TxFS setup to falling edge of SClk	t_{sis}	35			ns
CmdDat/TxDat hold from fall edge of SClk	t_{sih}			0	ns
CmdFS/TxFS hold from fall edge of SClk	t_{sih}			0	ns
CmdRdDat/RxDat propagation from rising edge of SClk	t_{sop}			5	ns
CmdRdFS/RxFS propagation from rising edge of SClk	t_{sop}			5	ns
CmdRdDat/RxDat hold from rising edge of SClk	t_{soh}	-5			ns
CmdRdFS/RxFS hold from rising edge of SClk	t_{soh}	-5			ns
** Cmd1 port in bi-directional mode **					
CmdDat1 propagation from rising edge of SClk	t_{sop}			7	ns
CmdDat1 hold from rising edge of SClk	t_{soh}	-7			ns
** TxFS in bi-directional mode **					
TxFS propagation from rising edge of SClk	t_{sop}			7	ns
TxFS hold from rising edge of SClk	t_{soh}	-7			ns

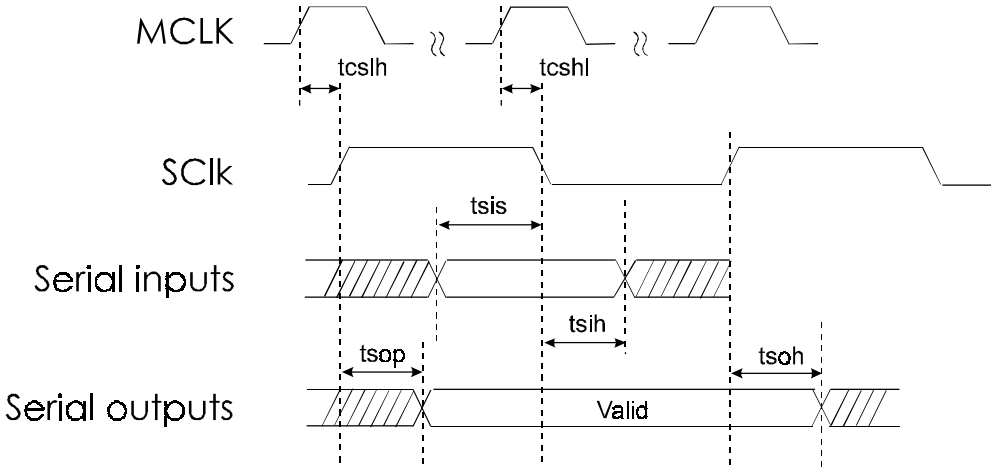


Figure 7 Serial Port Interfaces - Timing Parameters

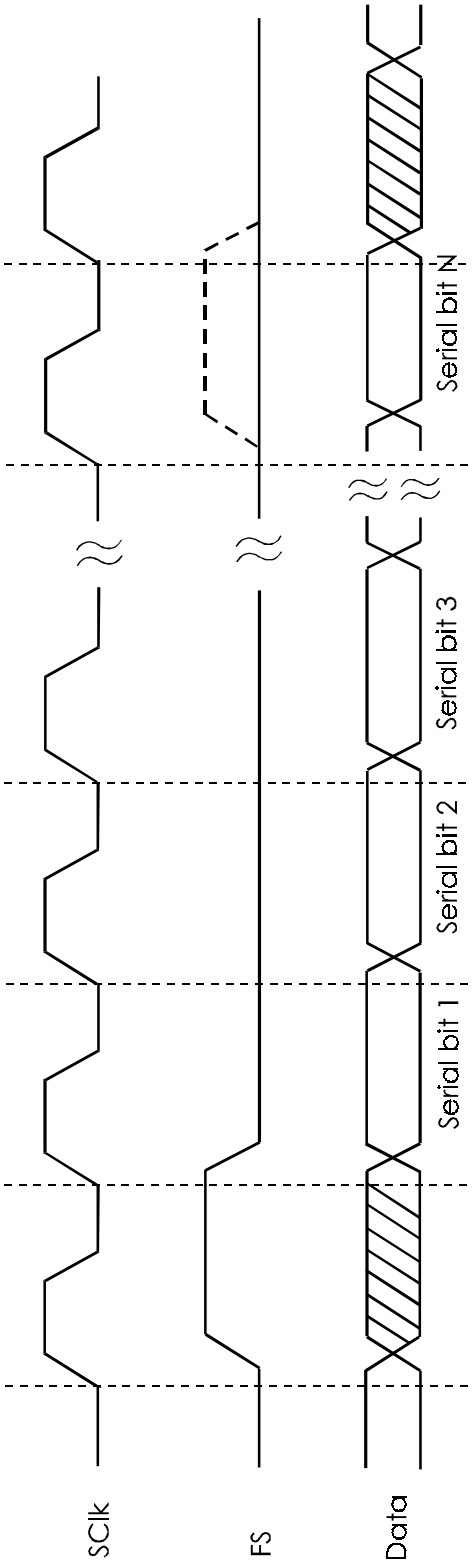


Figure 7a Basic Serial Port Signals

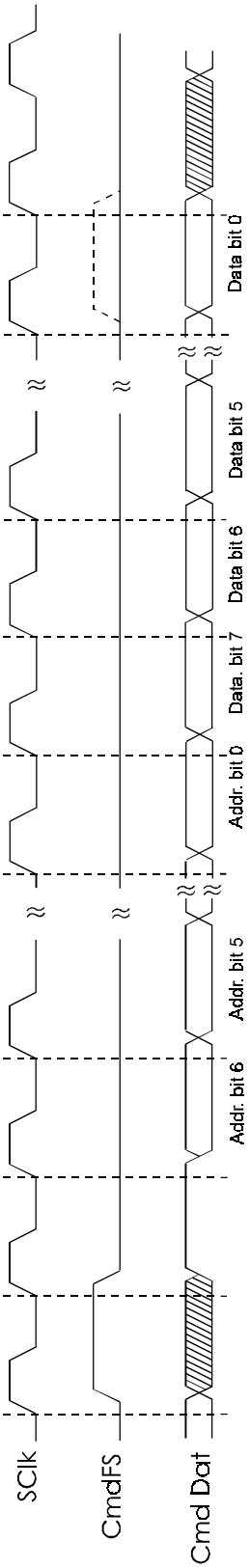


Figure 7b Command Write operation

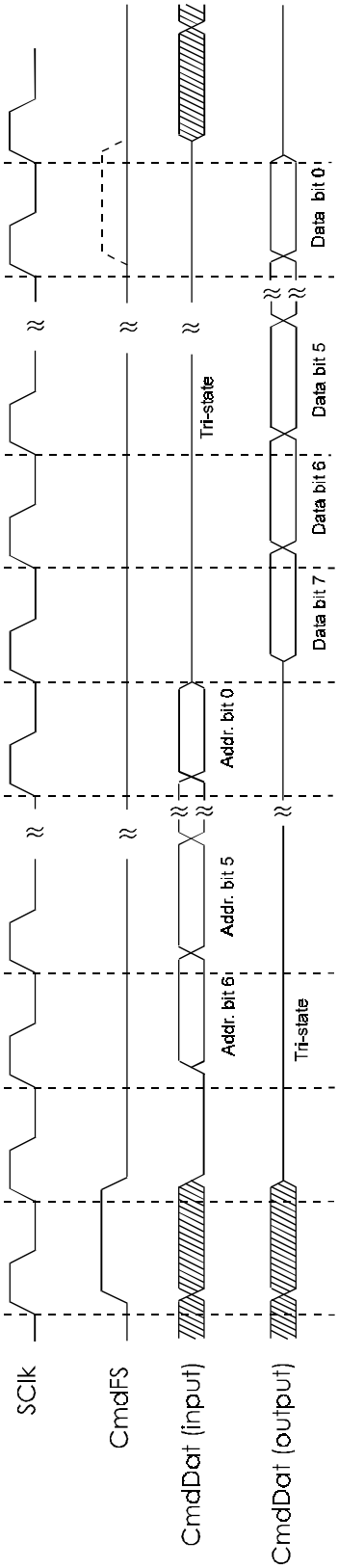


Figure 7c Bi-dir Command Read Operation

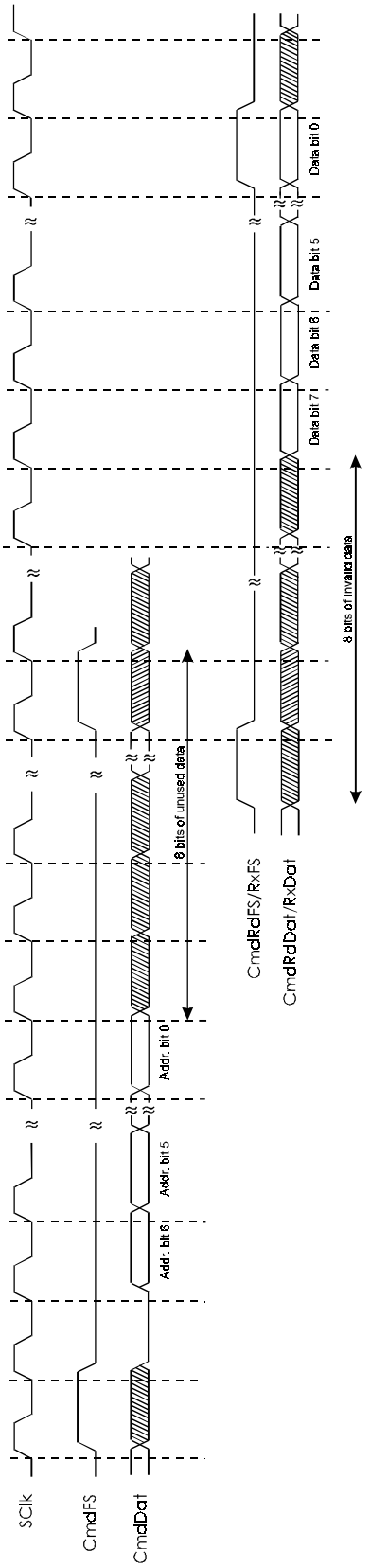


Figure 7d Non bi-dir Command Read Operation

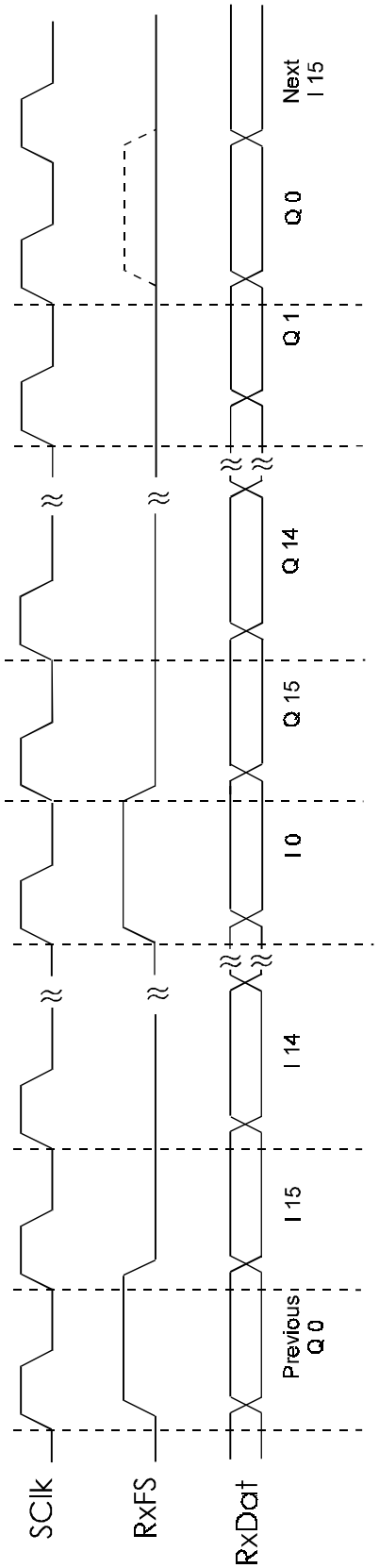


Figure 7e Rx Data Serial Port Read Operation

Timing Parameters - C-BUS	Marker	Min.	Typ.	Max.	Units
CSN low to CCLK high time	t_{CSE}	1/MCLK			s
Last CCLK high to CSN high time	t_{CSH}	1/MCLK			s
CCLK low to RDATA output enable time	t_{LOZ}	0.0			ns
CSN high to RDATA high impedance	t_{HIZ}			10/MCLK	s
CSN high time between transactions	t_{CSOFF}	10/MCLK			s
Inter-byte time	t_{NXT}	2/MCLK			s
CCLK cycle time	t_{CK}	3/MCLK			s
CCLK high time	t_{CH}	1/MCLK			s
CCLK low time	t_{CL}	1/MCLK			s
CDATA setup time	t_{CDS}	75			ns
CDATA hold time	t_{CDH}	25			ns
RDATA setup time	t_{RDS}	50			ns
RDATA hold time	t_{RDH}	0			ns

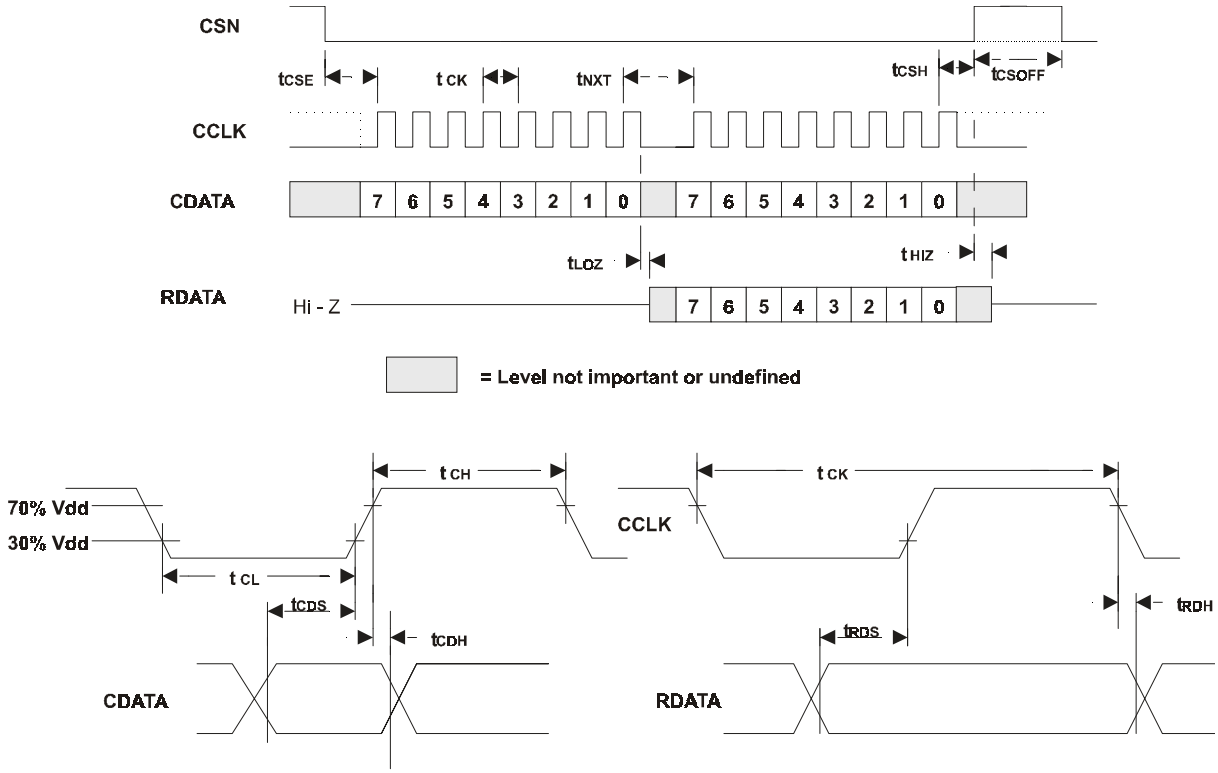


Figure 7f C-BUS Interface - Timing Parameters

7.2 Packaging

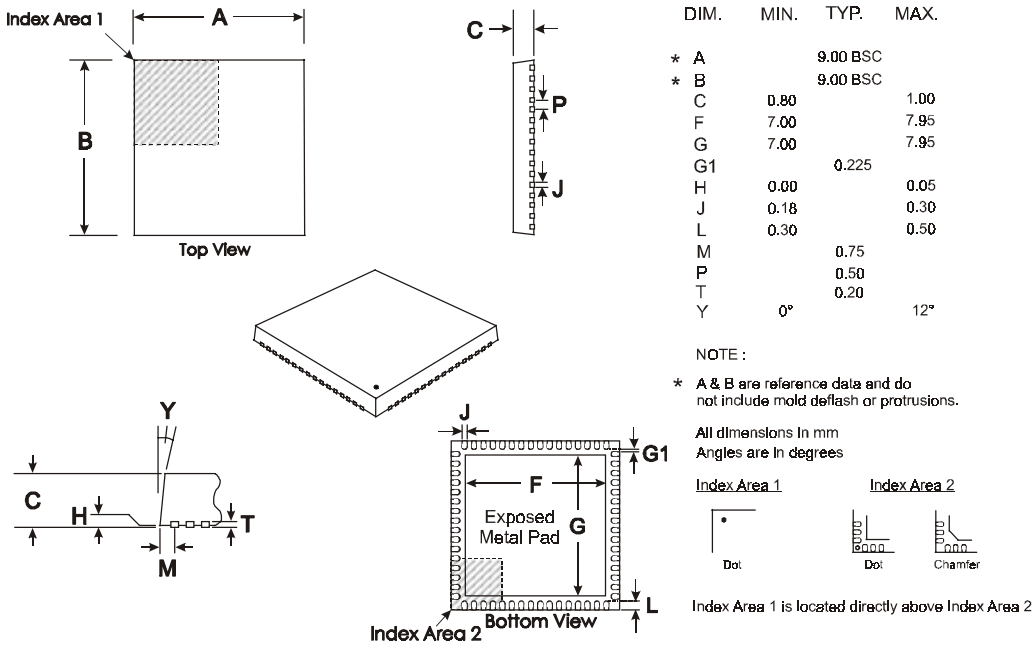


Figure 8 Q1 Mechanical Outline: *Order as part no. CMX981Q1*

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