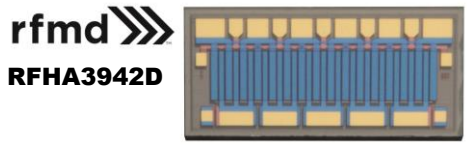
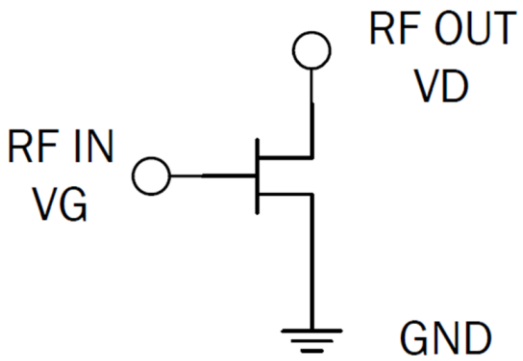
# RFHA3942D

## 35W Linear GaN on SiC Power Amplifier Die




The RFHA3942D is a 48V, 35W, GaN on SiC high power discrete amplifier die designed for military communications, electronic warfare, general purpose broadband, commercial wireless infrastructure, and industrial/scientific/medical applications. Using a second generation advanced high power density gallium nitride (GaN) semiconductor process with improved linearity, the RFHA3942D is able to achieve high efficiency, excellent linearity, and flat gain over a broad frequency range in a single amplifier design with proper packaging and assembly. The RFHA3942D is an unmatched 0.5µm gate, GaN transistor die suitable for many applications with > 45.5dBm saturated power, > 56% saturated drain efficiency, and > 16.5dB small signal gain at 2GHz.




Functional Block Diagram

Package: Die

## Features

- Broadband Operation DC to 4GHz
- Advanced GaN HEMT Technology
- Packaged Small Signal Gain = 16.3dB at 2GHz
- 48V Typical Modulated Packaged Performance
  - $P_{OUT}$ 39.5dBm
  - Gain 16.3dB
  - Drain Efficiency 32.6%
  - ACP-40dBc
- 48V Typical CW Package Performance
  - $P_{OUT}$ 45.2dBm
  - Gain 15.3dB
  - Drain Efficiency 58%
- Large Signal Models Available
- Chip Dimensions: 0.96mm x 1.92mm x 0.10mm
- Active Area Periphery: 11.1mm

## Applications

- Military Communications
- General Purpose Broadband Amplifiers
- Electronic Warfare
- Public Mobile Radios
- Commercial Wireless Infrastructure
- Cellular and WiMAX Infrastructure
- Industrial, Scientific, and Medical

## Ordering Information

| | |
|---|---|
| RFHA3942D | 35W Linear GaN on SiC Power Amplifier Die |

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
DS131024
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

## Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Drain Voltage ($V_D$) | 150 | V |
| Gate Voltage ($V_G$) | -8 to +2 | V |
| Gate Current ($I_G$) | 15 | mA |
| Ruggedness (VSWR) | 10:1 | |
| Storage Temperature Range | -55 to +125 | °C |
| Operating Junction Temperature ($T_J$) | 250 | °C |
| Human Body Model | Class 1A | |
| MTTF ($T_J$ < 200°C, 95% Confidence Limits)* | 3.2E + 06 | Hours |
| MTTF ($T_J$ < 250°C, 95% Confidence Limits)* | 5.3E + 04 | Hours |
| Thermal Resistance, Rth (junction to case) measured at $T_C$ = 85°C, DC bias only | 3.0 | °C/W |

**Caution!** ESD sensitive device.

RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, <1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

* MTTF – median time to failure for wear-out failure mode (30% $I_{DSS}$ degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT (random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

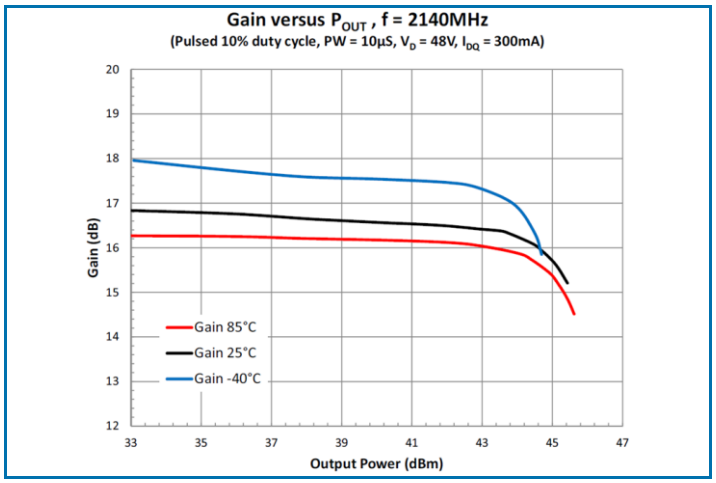
**Thermal resistance assumes AuSn die attach on 1.5mm thick CPC carrier similar to Kyocera A1933. User will need to define this specification in the final application and ensure bias conditions satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$ to maintain maximum operating junction temperature at MTTF.

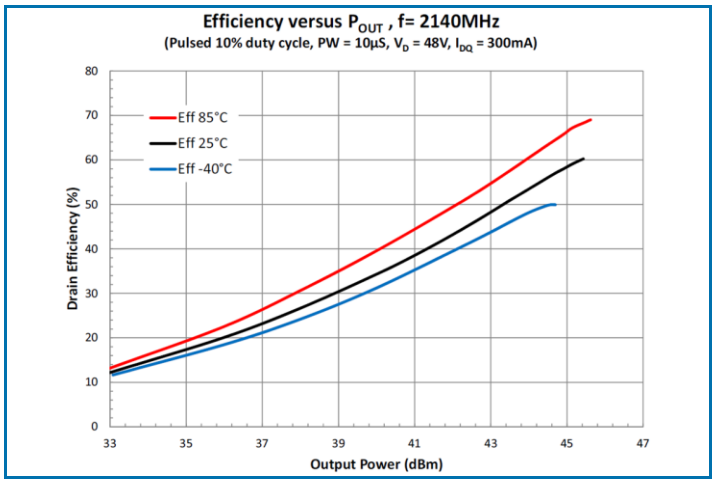
## Nominal Operating Parameters

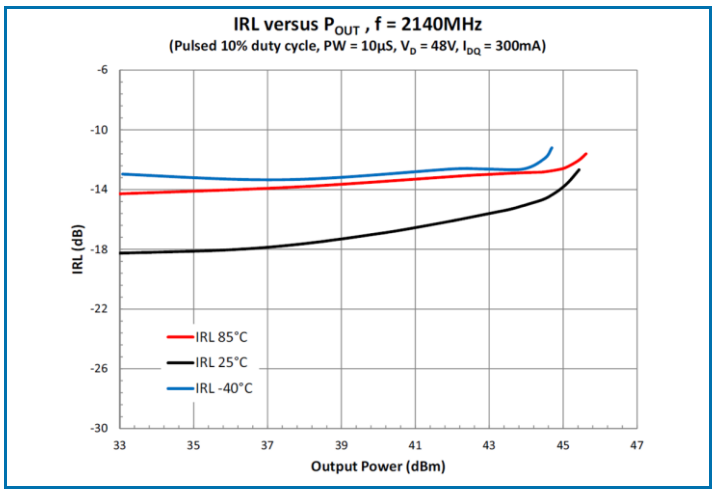
| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **Recommended Operating Conditions** | | | | | |
| Drain Voltage ($V_{DSQ}$) | 28 | | 48 | V | |
| Gate Voltage ($V_{GSQ}$) | -1.2 | -0.9 | -0.6 | V | |
| Drain Bias Current ($I_{DSQ}$) | | 300 | | mA | |
| Frequency of Operation | DC | | 4000 | MHz | |
| **Die Capacitance from Packaged Device Measurements (Package Capacitance Removed During Calibration)** | | | | | |
| $C_{RSS}$ | | 1.4 | | pF | $V_G$ = -8V, $V_D$ = 0V |
| $C_{ISS}$ | | 15 | | pF | |
| $C_{OSS}$ | | 11 | | pF | |
| **DC Functional Test** | | | | | |
| $I_{G(ON)}$ – Forward Bias Diode Gate Current | | | 50 | mA | $V_G$ = 1.1V, $V_D$ = 0V |
| $I_{G(OFF)}$ – Gate Leakage | | | 2 | mA | $V_G$ = -8V, $V_D$ = 0V |
| $I_{D(OFF)}$ – Drain Leakage | | | 0.2 | mA | |
| $I_{D(OFF)}$ – 48V Drain Leakage | | | 2.5 | mA | $V_G$ = -8V, $I_D$ = 48A |

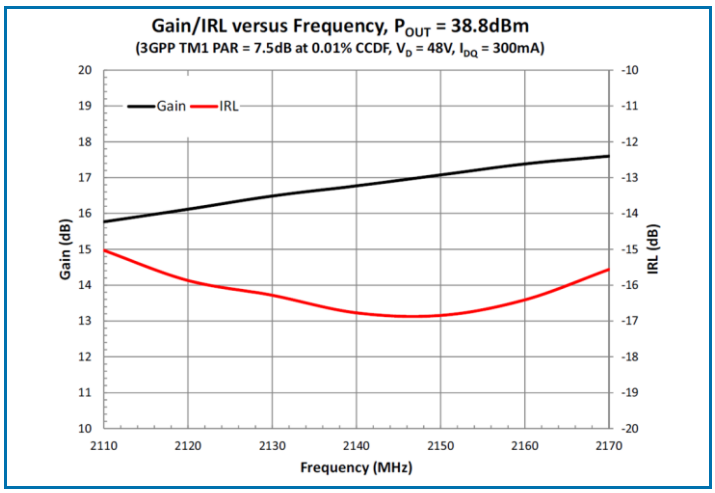
| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **DC Functional Test (cont'd)** | | | | | |
| $I_{D(OFF)}$ – 150V Drain Leakage | | | 5.0 | mA | $V_G$ = -8V, $V_D$ = 150V |
| $V_{GS(TH)}$ – Threshold Voltage | | -1.5 | | V | $V_D$ = 48V, $I_D$ = 11mA |
| $V_{DS(ON)}$ – Drain Voltage at High Current | | 1.5 | | V | $V_G$ = 0V, $I_D$ = 1.5A |
| **RF Typical Performance** | | | | | **Test Conditions: $V_{DSQ}$ = 48V, $I_{DSQ}$ = 300mA, T = 25°C, IS95 (9 Channel Model)** |
| $V_{GS(Q)}$ | -1.5 | -0.9 | -0.3 | V | $V_D$ = 48V, $I_{DQ}$ = 300mA |
| Gain | | 16.3 | | dB | IS95 (9.8dB PAR at 0.01% CCDF), $P_{OUT}$ = 39.5dBm, f = 2140MHz |
| Drain Efficiency | | 32.6 | | % | |
| Output PAR (CCDF at 0.01%) | | 6.1 | | dB | |
| Gain | | 15.3 | | dB | CW, f = 2140MHz |
| Output Power | | 45.2 | | dBm | |
| Drain Efficiency | | 58 | | % | |

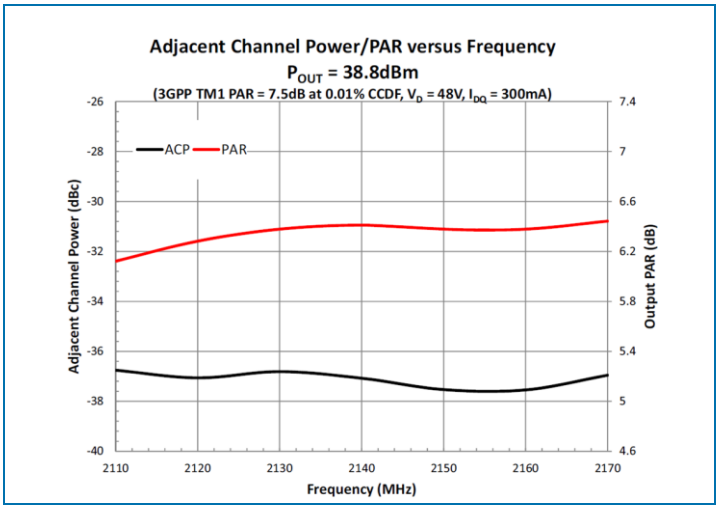
## Typical Performance of Non-Internally Matched Packaged Die in Linearity Optimized Circuit (T = 25°C unless noted)



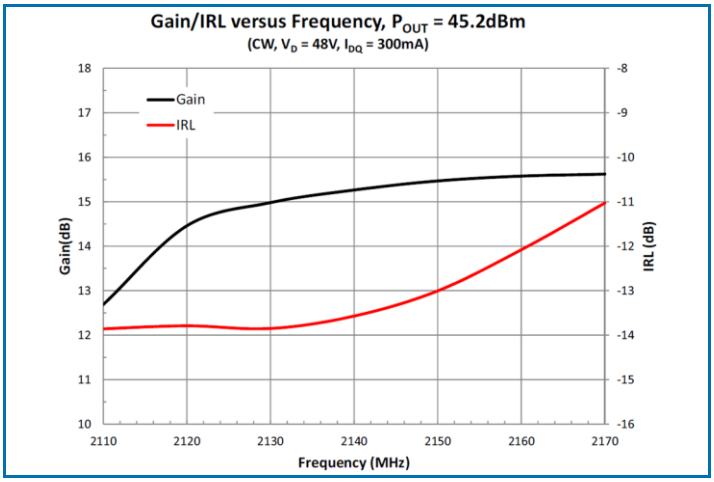



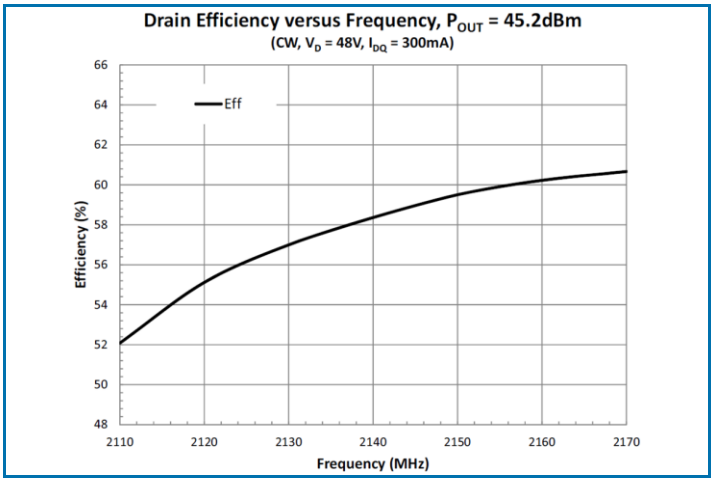



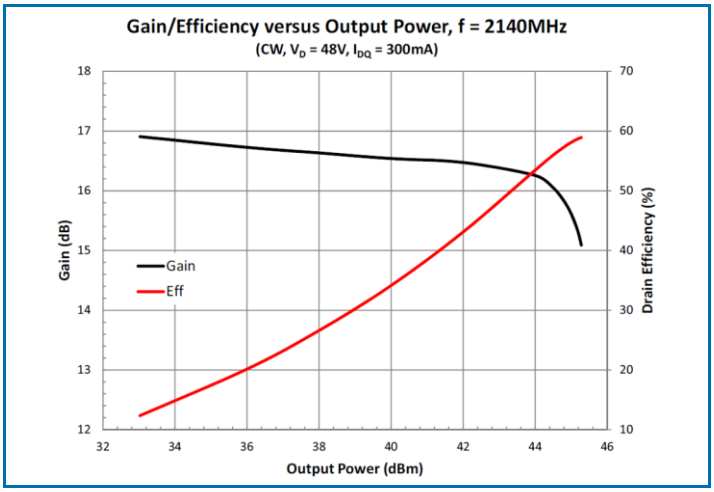



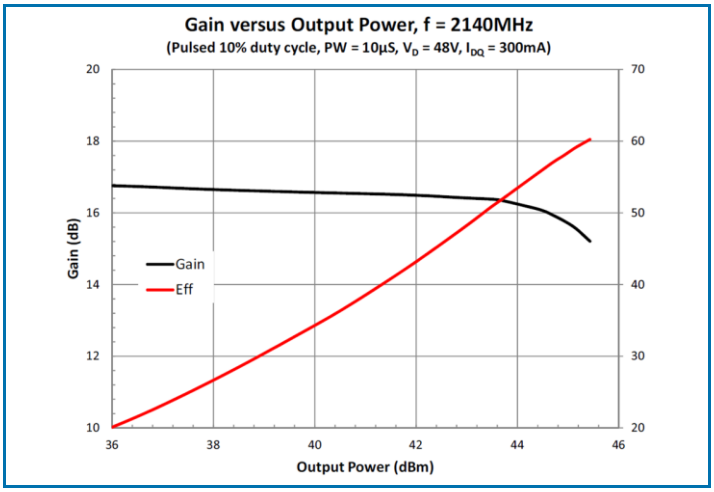



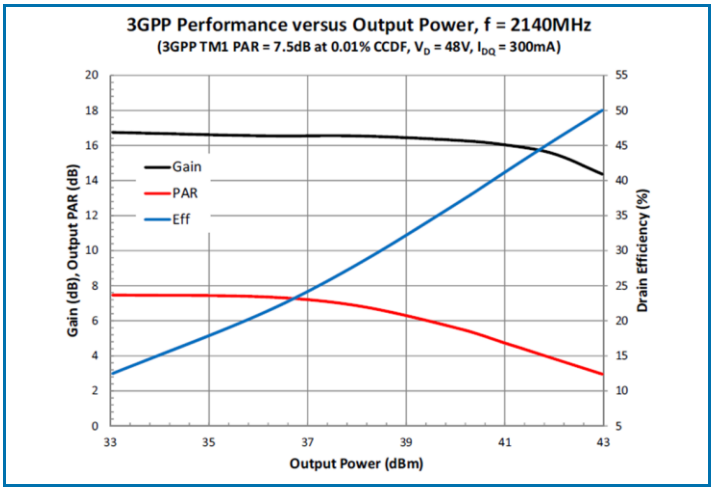
## Typical Performance of Non-Internally Matched Packaged Die in Linearity Optimized Circuit (T = 25°C unless noted) (continued)

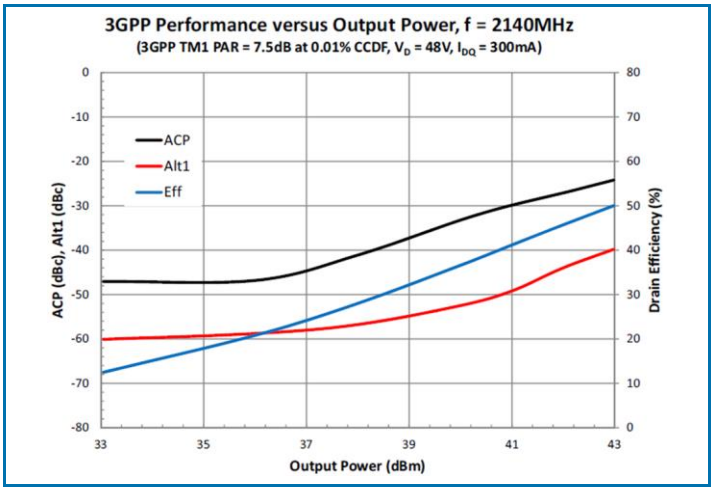


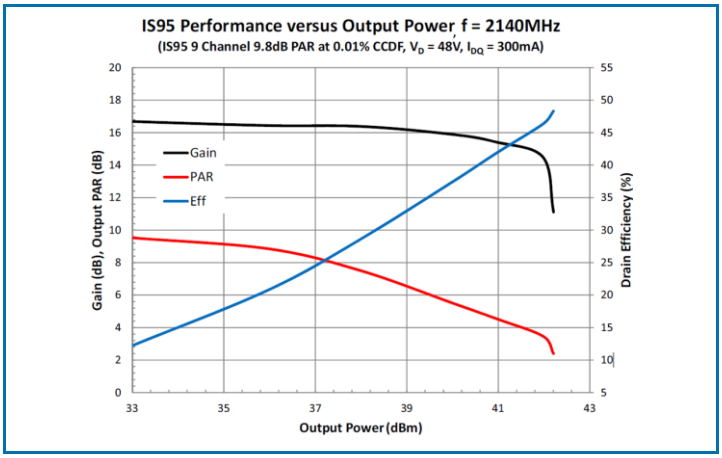



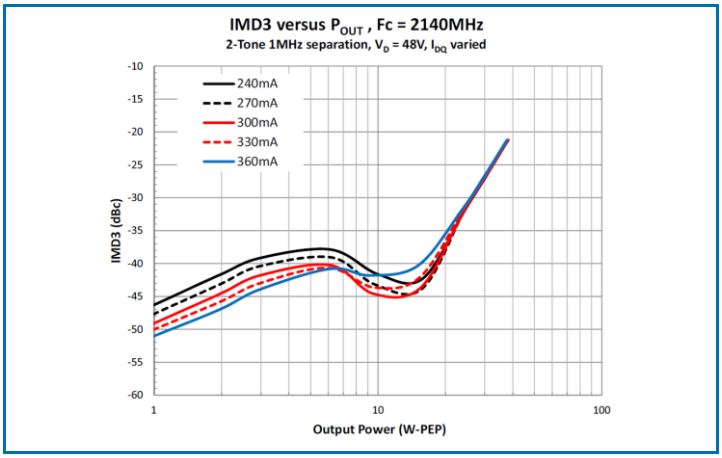



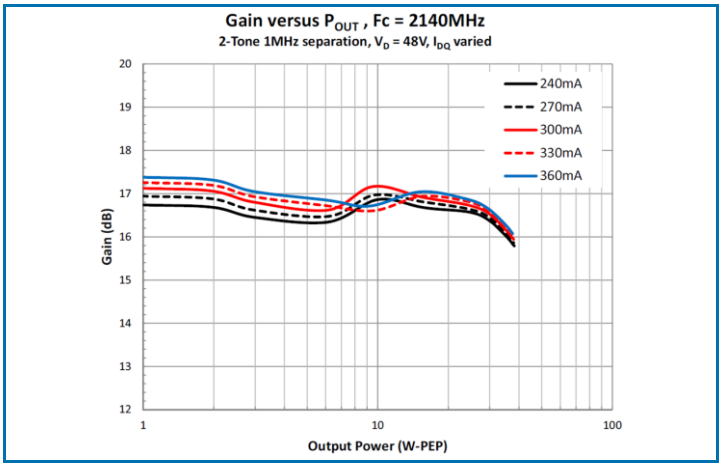



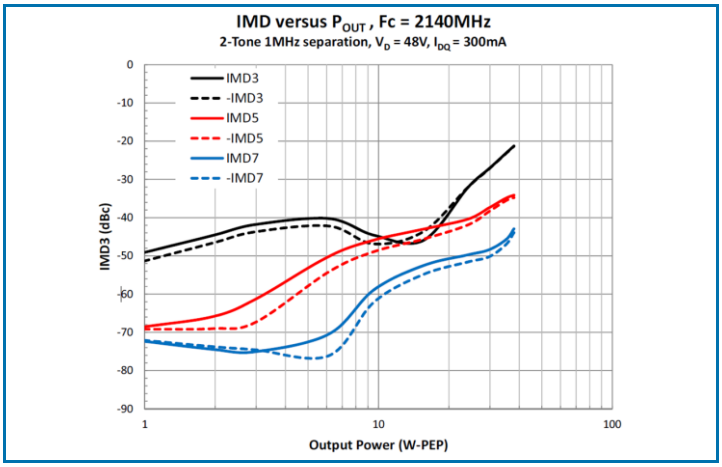



## Typical Performance of Non-Internally Matched Packaged Die in Linearity Optimized Circuit (T = 25°C unless noted) (continued)

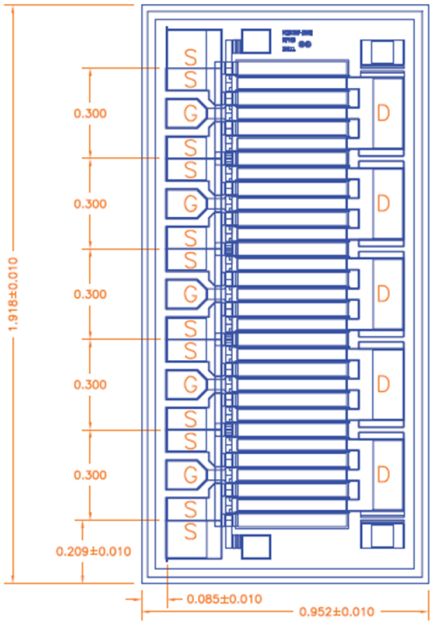


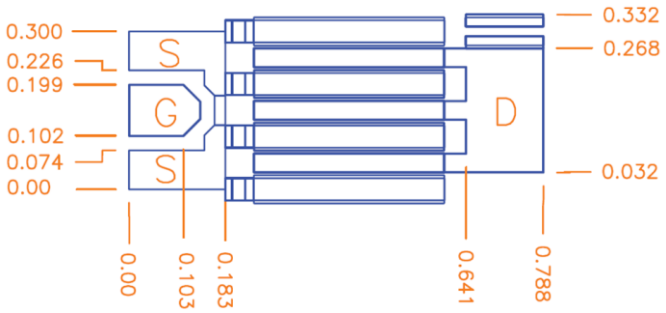



## Die Drawing (Dimensions in millimeters)




External dim. tolerance due to dicing process development

Bond Pad Key
G = Gate
S = Source
D = Drain
Die thickness = 0.101mm
Die backside metal = Au




Detail of Unit Cell

## Bias Instruction for RFHA3942D Die

ESD Sensitive Material. Please use proper ESD precautions when handling devices die.
Die must be mounted with minimal die attach voids for proper thermal dissipation. This device is a depletion mode HEMT and must have gate voltage applied for pinched off prior to applying drain voltage.

1. Mount device on carrier or package with minimal die attach voiding and applying proper heat removal techniques.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -8V to VG.
4. Apply 48V to VD.
5. Increase $V_G$ until drain current reaches desired bias point.
6. Turn on the RF input.

# Assembly Notes

## Die Storage

- Individual bare die should be held in appropriately sized ESD waffle trays or ESD GEL packs.
- Die should be stored in CDA/N2 cabinets and in a controlled temperature and humidity environment.

## Die Handling

- Die should only be picked using an auto or semi-automated pick system and an appropriate pick tool.
- Pick parameters will need to be carefully defined so not to cause damage to either the top or bottom die surface.
- GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.
- RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

Caution: The use of inappropriate or worn-out ejector needle and improper ejection parameter settings can cause die backside tool marks or micro-cracks that can eventually lead to die cracking.

## Die Attach

There are two commonly applied die attach processes: adhesive die attach and eutectic die attach. Both processes use special equipment and tooling to mount the die.

### EUTECTIC ATTACH

- 80/20 AuSn preform, 0.5mil to 1mil thickness, made from virgin melt gold.
- Pulsed heat or die scrub attach process using auto or semi-automatic equipment.
- Attach process carried out in an inert atmosphere.
- Custom die pick collets are required that match the outline of the die and the specific process employed using either pulsed, fixed heat, or scrub.
- Maximum temperature during die attach should be no greater than 320°C and for less than 30 seconds.
- Key parameters that need to be considered include: die placement force, die scrub profile and heat profile.
- Minimal amount of voiding is desired to ensure maximum heat transfer to the carrier and no voids should be present under the active area of the die.
- Voiding can be measured using X-ray or acoustic microscopy.
- The acceptable level of voiding should be determined using thermal modeling analysis.

### ADHESIVE ATTACH

- High thermal silver filled epoxy is dispensed in a controlled manner and die is placed using an appropriate collet. Assembled parts are cured at temperatures between 150°C and 180°C.
- Always refer to epoxy manufacturer's data sheet.
- Industry recognized standards for epoxy die attach are clearly defined within MIL-883.

## Early Life Screen Conditions

RFMD recommends an Early Life Screen test that subjects this die to $T_J$ = 250°C (junction temperature) for at least 1 hour prior to field deployment.

## Mounting and Thermal Considerations

The thermal resistance provided as $R_{TH}$ (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

## DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts $V_{GS}$ the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying $V_{GS}$ = -5V before applying any $V_{DS}$.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current ($I_{DQ}$) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance trade-offs.

## GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the $C_{DS}$ (drain to source), $C_{GS}$ (gate to source) and $C_{GD}$ (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off ($V_{GS}$ = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input ($C_{ISS}$), output ($C_{OSS}$), and reverse ($C_{RSS}$) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$