

LD3003

128 Segment LCD Controller and Driver

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OVERVIEW

LD3003, LCD Display Driver IC with microcontroller displays 1/4-duty LCD with up to 128 segments.

LD3003 uses a serial interface data input protocol. This device is compatible with MC14LC5003 of MOTOROLA.

FEATURES

- Supports 1/4 duty LCD drive under serial data control.
- Drives up to 128 segments.
- Supports serial interface data input protocol with the system controller.
- Operating Voltage Range : 2.7V ~ 5.5V
- Quiescent Supply Current : 30uA @ 2.7V V_{DD}
- Operating Temperature Range : -40 to 85°C
- Package : 52MQFP, 44MQFP
- Major Applications : Segmented Alphanumeric, Bar Graph, Dot matrix, Custom

ORDERING INFORMATION

PART NUMBER	PACKAGE	Ta
LD3003-52QFP	52 QFP	-40°C to 85 °C

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, VSS = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	VDD max	VDD	-0.5 to +6.5	V
	VLCD max	VLCD	-0.5 to +6.5	V
Input Voltage	VIN 1	DIN, DCLK, ENB	-0.5 to +6.5	V
	VIN 2	OSC1	-0.5 to VDD + 0.5	V
Output Voltage	VOUT 1	OSC2	-0.5 to VDD + 0.5	V
	VOUT 2	SEG1 to SEG32, COM1 to COM4	-0.5 to VLCD + 0.5	V
Output Current	IOUT 1	SEG1 to SEG32	300	μA
	IOUT 2	COM1 to COM4	1	mA
Allowable Power Dissipation	Pd max	Ta = 85°C	150	mW
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, VSS = 0 V)

Parameter	Symbol	VDD	VLCD	Min	Typical	Max	Unit
Input High-level Voltage	VIH	2.8	5	2			V
		5.5	5	3.85			
Input Low-level Voltage	VIL	2.8	5			0.85	V
		5.5	5			1.65	

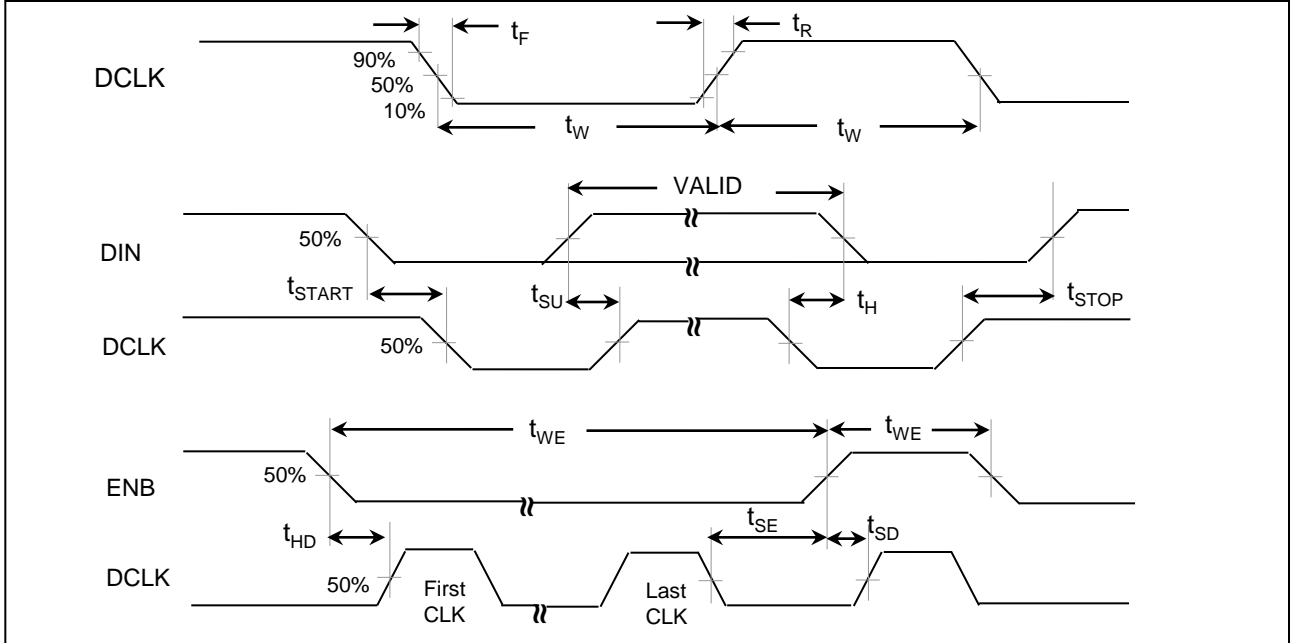
ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Symbol	VDD	VLCD	Min	Typical	Max	Unit
Frequencies OSC2 Frequent @ R1; R1 =200 kΩ OSC2 Frequent @ R2; R2 =996 kΩ)	FOSC2	5	5	100	-	150	KHz
	FOSC2	5	5	23	-	33	
Supply Standby Current (No Clock)	IDDS	2.7	-	-	15	30	μA
		5.5	-	-	18	50	
	ILCDS	-	2.7	-	20	800	
		-	5.5	-	150	1500	
Supply Current No Loading Loading = 270pF	IDDQ	2.7	-		30		μA
		2.7	-			70	
No Loading Loading = 270pF		5.5	-		170		
		5.5	-			400	
No Loading No Loading	ILCDQ	-	2.7			40	
		-	5.5			70	
Input Leakage	I _{IH}	-	-	-0.1		0.1	μA
	I _{IL}	-	-	-0.1		0.1	μA
Output high-level Voltage Seg to Seg32, IO=-20uA Com1 to Com4, IO=-100uA	VOH1	2.7	2.7	VLCD-0.15	VLCD-0.1	VLCD	V
	VOH2	2.7	2.7	VLCD-0.15	VLCD-0.1	VLCD	
Output low-level Voltage Seg to Seg32, IO=20uA Com1 to Com4, IO=100uA	VOL1	2.7	2.7	-	0.1	0.15	V
	VOL2	2.7	2.7	-	0.1	0.15	

ELECTRICAL CHARACTERISTICS (Continued)

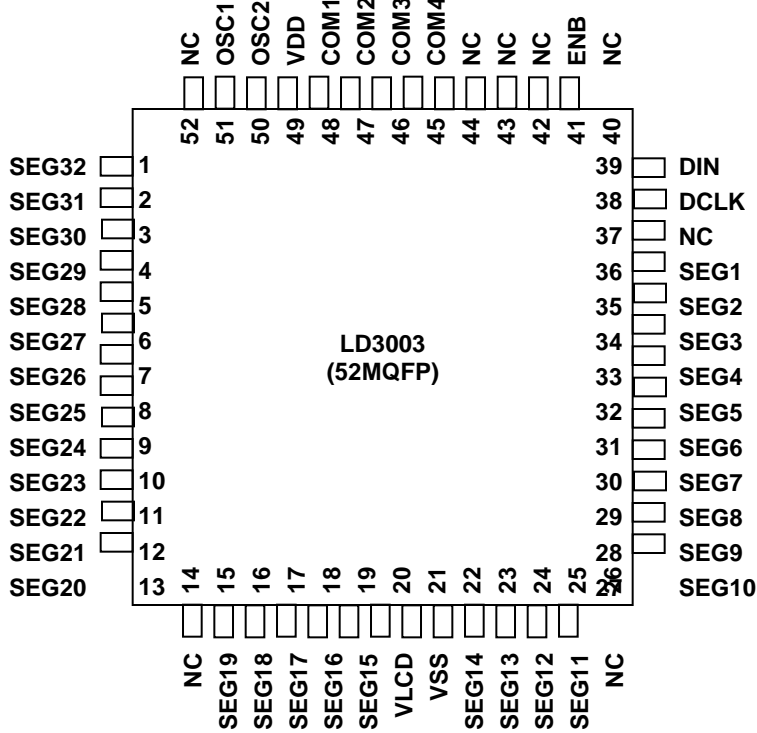
Parameter	Symbol	VDD	VLCD	Min	Typical	Max	Unit
Pulse Width, DCLK	t_w	5	-	100		-	ns
		3	-	100		-	
DCLK Rise/Fall time	t_R, t_F	5	-	-		120	μ s
		3	-	-		120	
Setup time, DIN to DCLK	t_{SU}	5	-	20		-	ns
		3	-	20		-	
Hold time, DIN to DCLK	t_H	5	-	40		-	ns
		3	-	60		-	
Hold time for Start Condition	t_{START}	5	-	100		-	ns
		3	-	100		-	
Hold time for Stop Condition	t_{STOP}	5	-	100		-	ns
		3	-	100		-	
DCLK Low to ENB High	t_{SE}	5	-	20		-	ns
		3	-	20		-	
ENB High to DCLK High	t_{SD}	5	-	20		-	ns
		3	-	20		-	
ENB High Pulse Width	t_{WE}	5	-	100		-	ns
		3	-	100		-	
ENB Low to DCLK High	t_{HD}	5	-	20		-	ns
		3	-	20		-	

SWITCHING WAVEFORMS

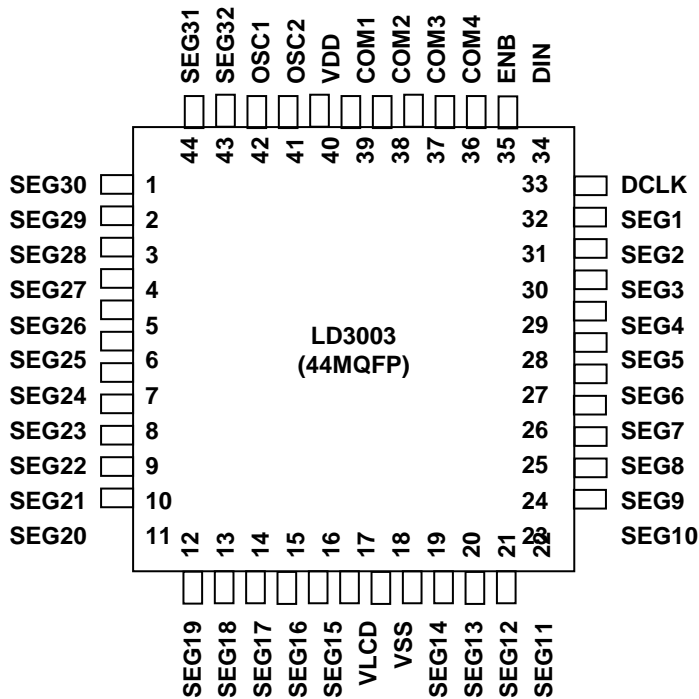


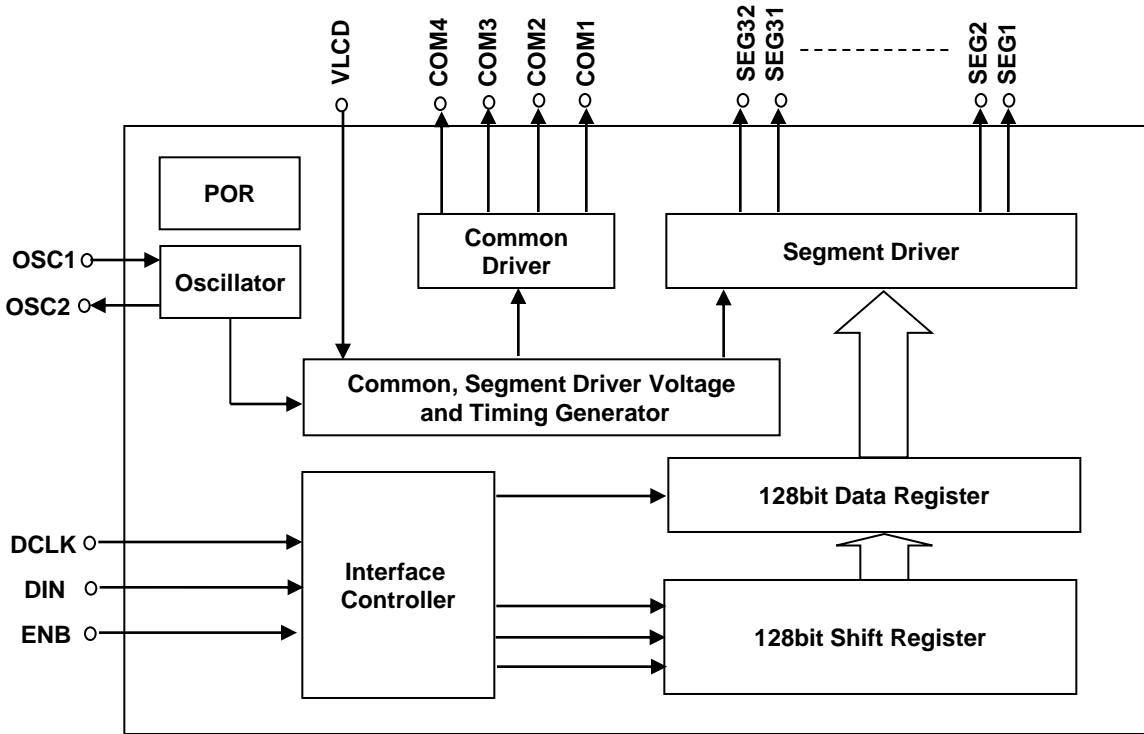
PIN ASSIGNMENT

52 MQFP



44 MQFP



BLOCK DIAGRAM


PIN DISCREPTION

Pin Name	Pin NO (52MQFP)	Functions	I/O	Handling when unused
SEG32 to SEG1	1 to 13 15 to 19 22 to 25 27 to 36	Segment outputs for displaying the display data transferred by serial data input.	O	Open
COM4 to COM1	45 to 48	Common driver outputs. The frame frequency f_O is given by: $f_O = 100 \text{ Hz}$ at $f_{osc}=100\text{KHz}$.	O	Open
OSC1	51	Oscillator input pin. Connected resistor with OSC2 pin.	I	GND
OSC2	50	Oscillator output pin. Connected resistor with OSC1 pin.	O	Open
DCLK	38	Synchronization clock input pin.	I	GND
DIN	39	Transfer data input pin.		
ENB	41	Enable input pin. These pins are connected to the microcontroller.		
VLCD	20	Used to apply the LCD drive voltage externally.	I	Open
VDD	49	Logic block power supply. Provide a voltage in the range 2.7 to 5.5 V.	-	-
NC	14 26 37 40 42 43 44 52	No connection pins	-	Open
VSS	21	Ground pin. Connect to ground.	-	-

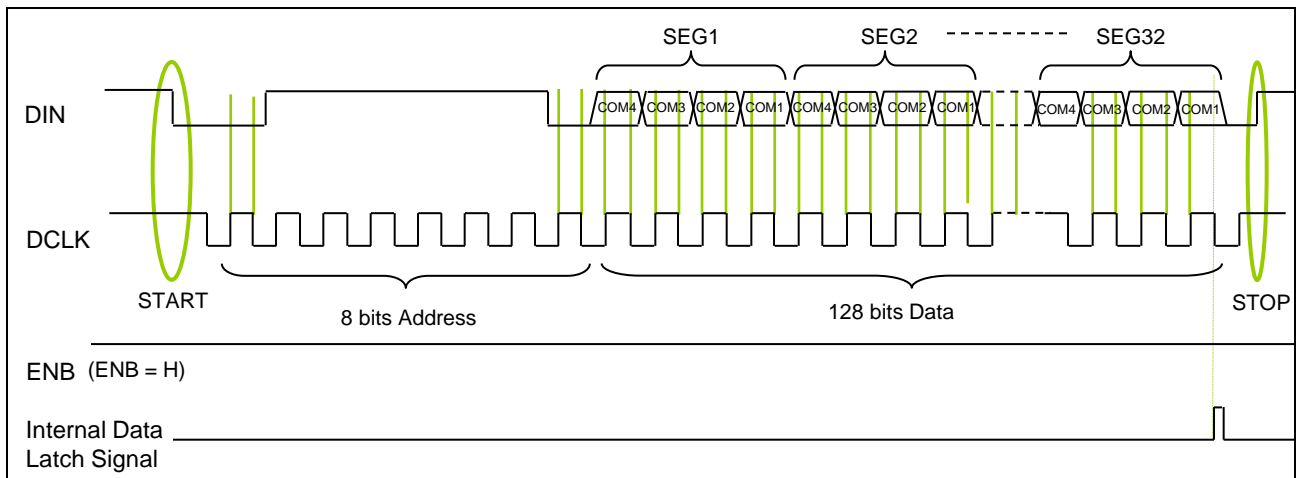
SERIAL DATA TRANSFER FORMAT

Before communication with LD3003 can begin, a start condition must be set up on the bus by the transmitter. To establish a start condition, the transmitter must pull the data line(DIN) low for at least one clock-pulse time while the clock line(DCLK) is high. The "idle" state for the clock line and data line is the high state. After the start condition has been established, an 8 bits address (01111110) should be sent by the transmitter. If the address sent corresponds to the address of LD3003 then on each successive clock pulse, the addressed device will accept a data bit.

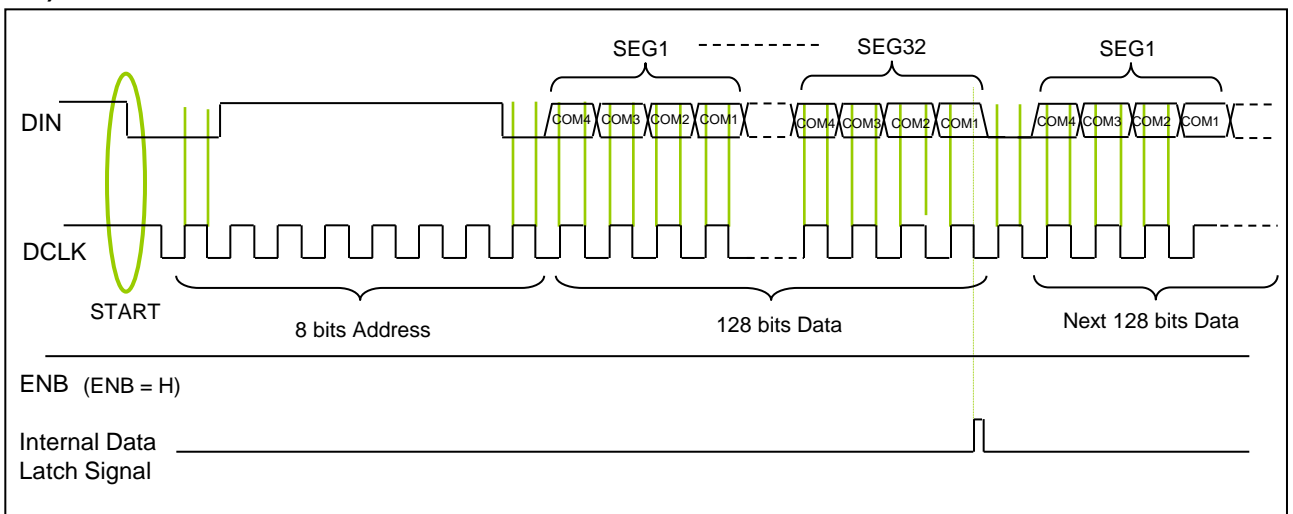
If the ENB pin is permanently high, then the addressed LD3003's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise, the control of this latch function may be overridden by holding the ENB line low until the new data is required to be displayed, then a high pulse should be sent on the ENB line. The high pulse must be sent during DCLK high(clock idle). To end communication with LD3003, a stop condition should be setup on the bus(or another start condition maybe set up if another communication is desired.). To establish a stop condition, the transmitter must pull the data line high for at least one clock-pulse time while the clock line is high.

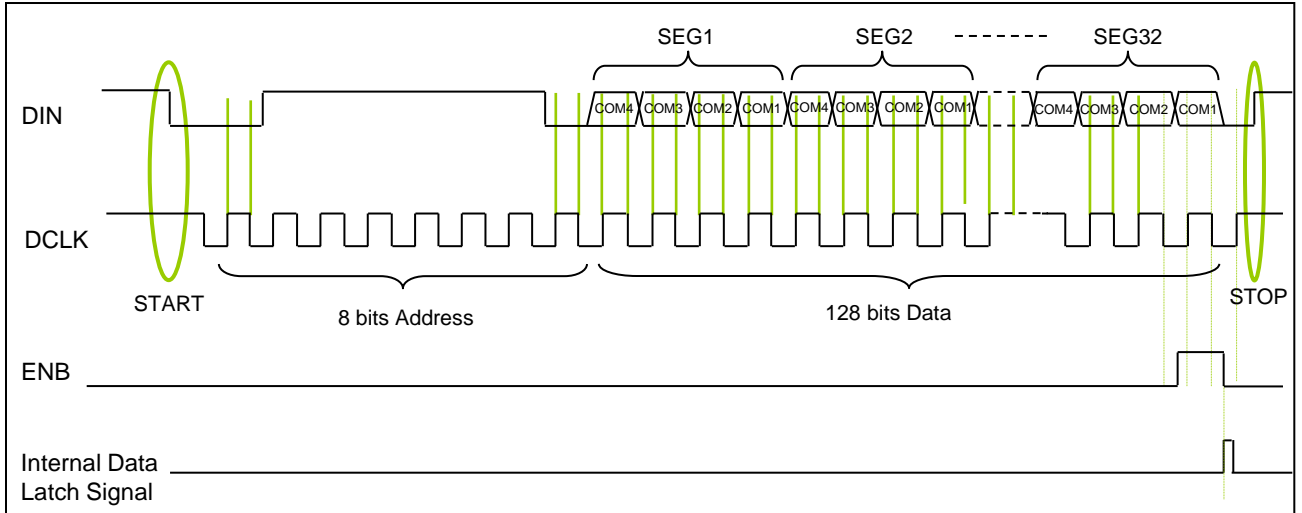
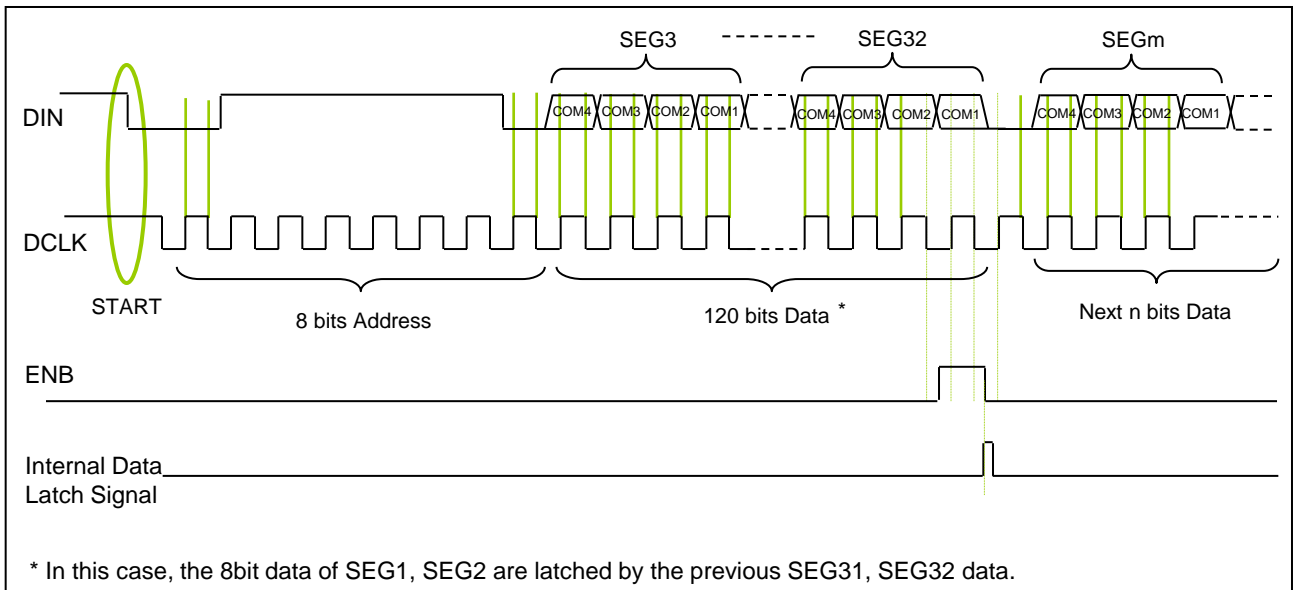
WHEN ENB PIN IS FIXED TO VDD

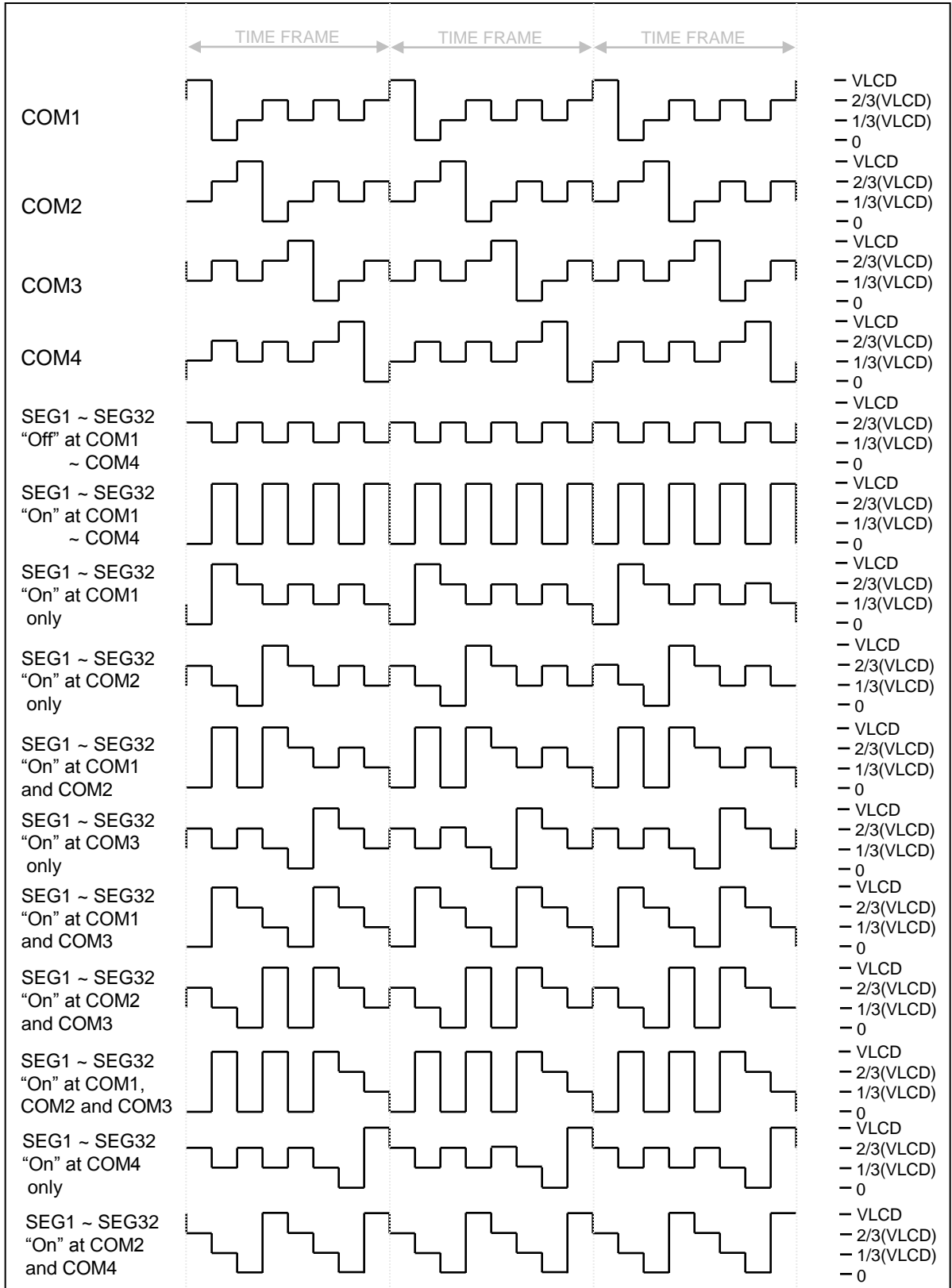
a) 128 bit Data Only Transfer Case



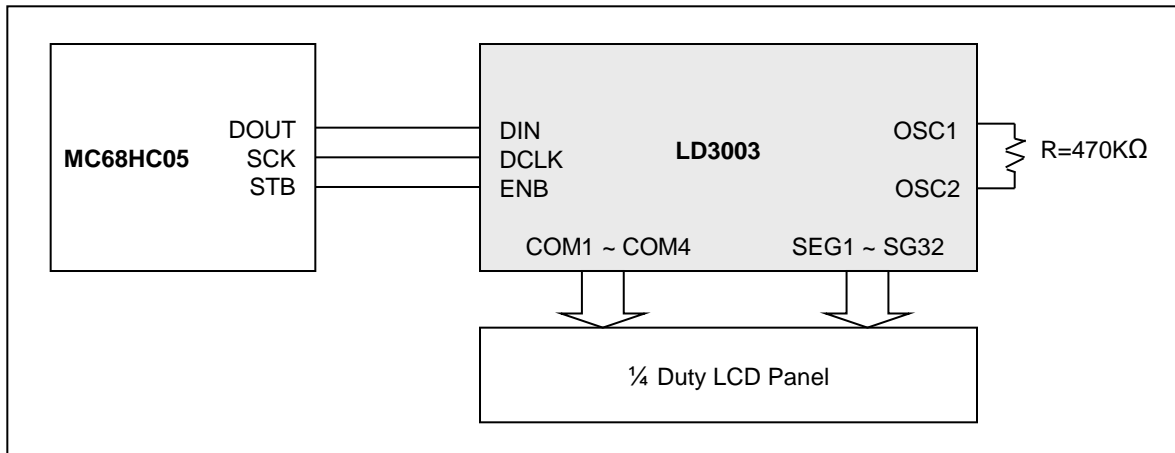
b) Continuous Transfer Case



WHEN ENB PIN IS USED
a) 128 bit Data Only Transfer Case

b) Under 128bit Data Transfer Case


LCD DRIVING WAVEFORM


APPLICATION INFORMATION



Serial Interface Example between LD3003 and MC68HC05

SERIAL DATA INTERFACE METHOD

PORTC	EQU	\$02	PORTC
DDRC	EQU	\$06	PORTDC
SEN	EQU	\$07	ENABLE PIN, PC7
SCL	EQU	\$06	CLOCK PIN, PC6
SDA	EQU	\$05	DATA PIN, PC5
DOUT	EQU	\$FF	OUTPUT DATA
	ORG	\$0050	
W1	RMB	1	
COUNT	RMB	1	
	ORG	\$1FFE	ADDRESS OF RESET VECTOR OF MC68HC05C4
	FCB	#\$01	RESET VECTOR
	FCB	#\$00	
***** Main Program start at 0100 *****			
START	ORG	\$0100	
	LDA	#DOUT	SET DATA LINE OUTPUT
	STA	DDRC	
AGAIN			
	LDX	#\$00	
	BSET	SDA, PORTC	IDLE STATE
	BSET	SCL, PORTC	CLOCK AND DATA ARE HIGH
READY			
	BSET	SEN, PORTC	EN=1
	LDA	#\$11	SET ADDRESS AND 8 CHARACTERS
	STA	W1	
	BCLR	SDA, PORTC	START CONDITION, DATA LOW WHILE CLOCK HIGH
LBYTE			
	CLC		
	LDA	#\$08	
	STA	COUNT	8 BITS TO SHIFT
	LDA	SEND, X	GET A BYTE
	INCX		

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LBIT          BCLR          SCL, PORTC      CLOCK LOW
              ROLA
              BCC          DZERO          DATA BIT=0?
              BSET          SDA, PORTC     NO, BIT=1 AND DATA HIGH
              JUMP         CLKHI

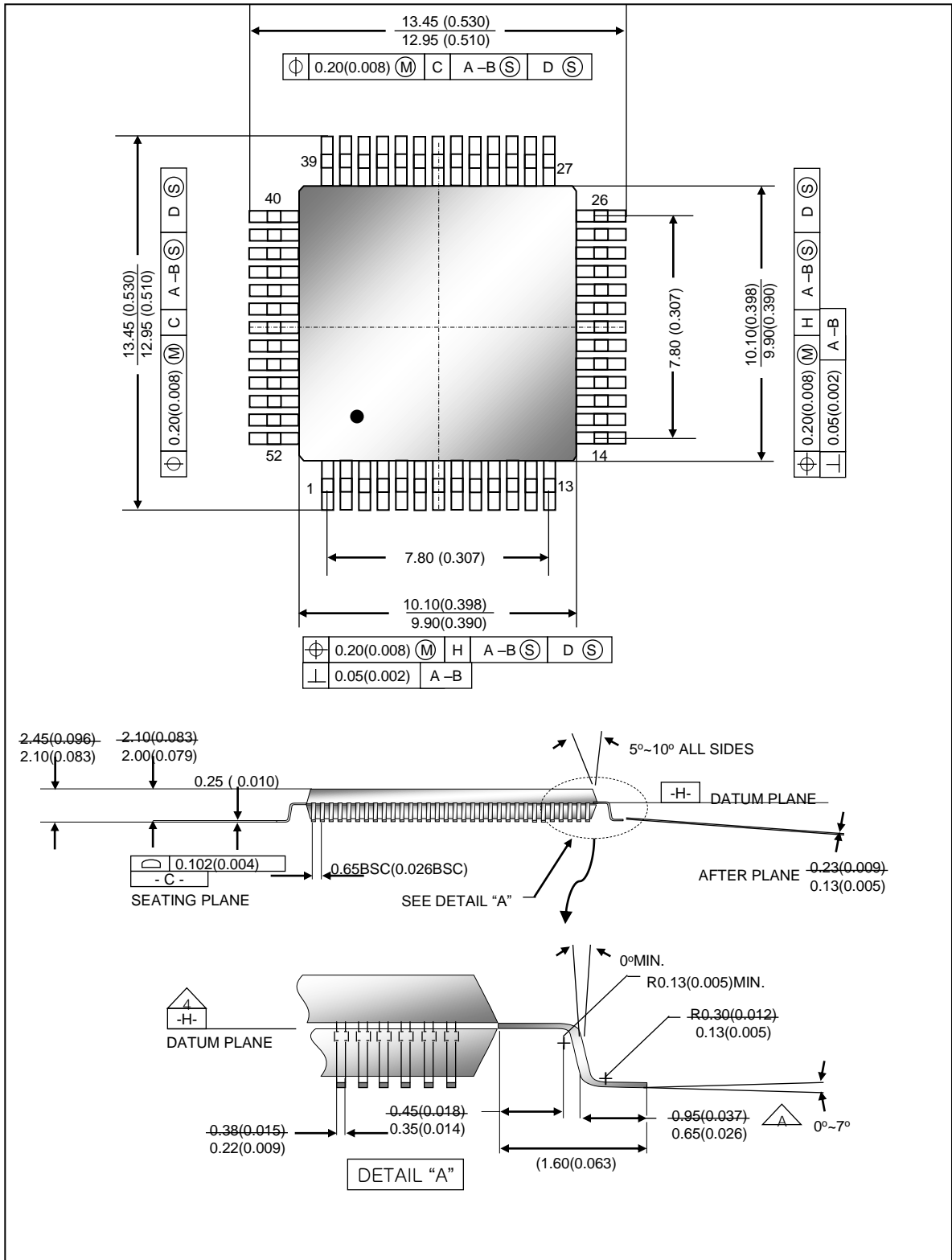
DZERO        BCLR          SDA, PORTC     DATA LOW
CLKHI        BSET          SCL, PORTC     CLOCK HIGH
              DEC          COUNT
              BNE          LBIT
              DEC          W1
              BNE          LBYTE          LAST BYTE?

STOP         BCLR          SCL, PORTC
              BCLR          SDA, PORTC     STOP CONDITION
              BSET          SCL, PORTC     DATA GOES HIGH WHILE CLOCK HIGH
              BSET          SDA, PORTC
              BCLR          SEN, PORTC     EN=0
              RTS

***** End of Program *****

***** LCD Address and Data *****

SEND        FCB          $7E          LCD DRIVER ADDRESS
              FCB          $FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF     DATA TO SENT
              FCB          $FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF
              RTS
    
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PACKAGE INFORMATION
52 PIN MQFP (10 x 10 Body)


The products listed herein are designed for ordinary electronic applications, such as electrical applications, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instrument, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

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