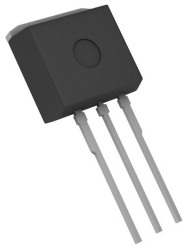
KERSEMI ELECTRONIC CO.,LTD.

# IRF9530NL

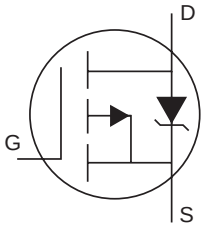
- Advanced Process Technology
- Surface Mount (IRF9530NS)
- Low-profile through-hole (IRF9530NL)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated

TO-262



## Description

The $D^2Pak$ is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The $D^2Pak$ is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.
The through-hole version (IRF9530NL) is available for low-profile applications.




$V_{DSS}$ = -100V

$R_{DS(on)}$ = 0.20Ω

$I_D$ = -14A

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ -10V⑤ | -14 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ -10V⑤ | -10 | |
| $I_{DM}$ | Pulsed Drain Current ①⑤ | -56 | |
| $P_D$ @$T_A$ = 25°C | Power Dissipation | 3.8 | W |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 79 | W |
| | Linear Derating Factor | 0.53 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy②⑤ | 250 | mJ |
| $I_{AR}$ | Avalanche Current① | -8.4 | A |
| $E_{AR}$ | Repetitive Avalanche Energy① | 7.9 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③⑤ | -5.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | ℃ |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |

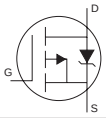
## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | 1.9 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ( PCB Mounted,steady-state)** | —— | 40 | |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | -100 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = -250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | -0.11 | —— | V/°C | Reference to 25°C, $I_D$ = -1mA⑤ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | —— | 0.20 | Ω | $V_{GS}$ = -10V, $I_D$ = -8.4A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | -2.0 | —— | -4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = -250μA |
| $g_{fs}$ | Forward Transconductance | 3.2 | —— | —— | S | $V_{DS}$ = -50V, $I_D$ = -8.4A⑤ |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | -25 | μA | $V_{DS}$ = -100V, $V_{GS}$ = 0V |
| | | —— | —— | -250 | | $V_{DS}$ = -80V, $V_{GS}$ = 0V, $T_J$ = 150°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -20V |
| $Q_g$ | Total Gate Charge | —— | —— | 58 | nC | $I_D$ = -8.4A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | —— | 8.3 | | $V_{DS}$ = -80V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | —— | 32 | | $V_{GS}$ = -10V, See Fig. 6 and 13 ④⑤ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 15 | —— | ns | $V_{DD}$ = -50V |
| $t_r$ | Rise Time | —— | 58 | —— | | $I_D$ = -8.4A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 45 | —— | | $R_G$ = 9.1Ω |
| $t_f$ | Fall Time | —— | 46 | —— | | $R_D$ = 6.2Ω, See Fig. 10 ④ |
| $L_S$ | Internal Source Inductance | —— | 7.5 | —— | nH | Between lead, and center of die contact |
| $C_{iss}$ | Input Capacitance | —— | 760 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 260 | —— | | $V_{DS}$ = -25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 170 | —— | | $f$ = 1.0MHz, See Fig. 5⑤ |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | -14 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ①⑤ | —— | —— | -56 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | -1.6 | V | $T_J$ = 25°C, $I_S$ = -8.4A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 130 | 190 | ns | $T_J$ = 25°C, $I_F$ = -8.4A |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 650 | 970 | nC | di/dt = -100A/μs ④⑤ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② Starting $T_J$ = 25°C, L =7.0mH $R_G$ = 25Ω, $I_{AS}$ = -8.4A. (See Figure 12)

③ $I_{SD}$ ≤ -8.4A, di/dt ≤ -490A/μs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRF9530N data and test conditions

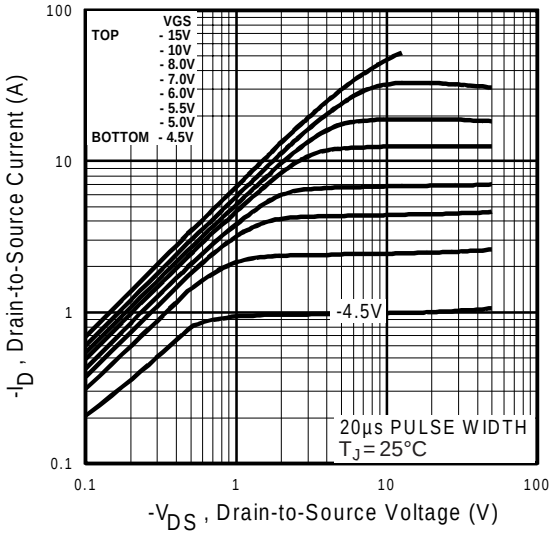



**Fig 1.** Typical Output Characteristics

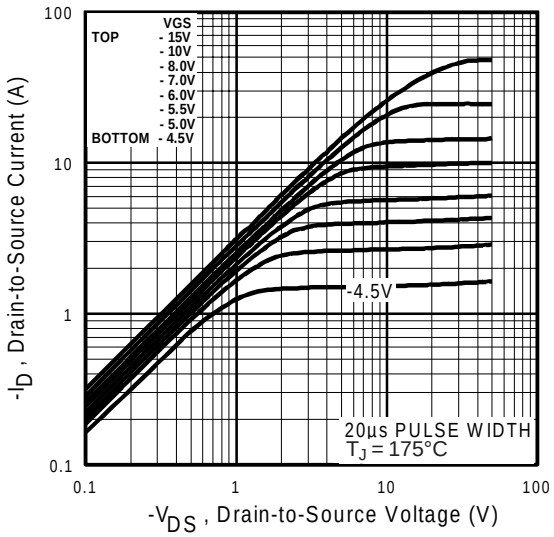



**Fig 2.** Typical Output Characteristics

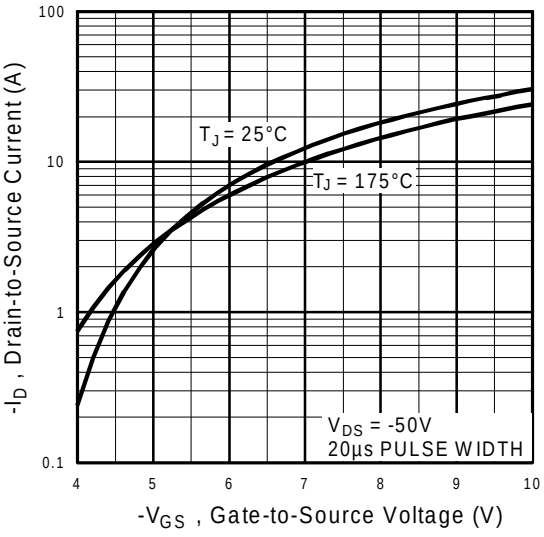



**Fig 3.** Typical Transfer Characteristics

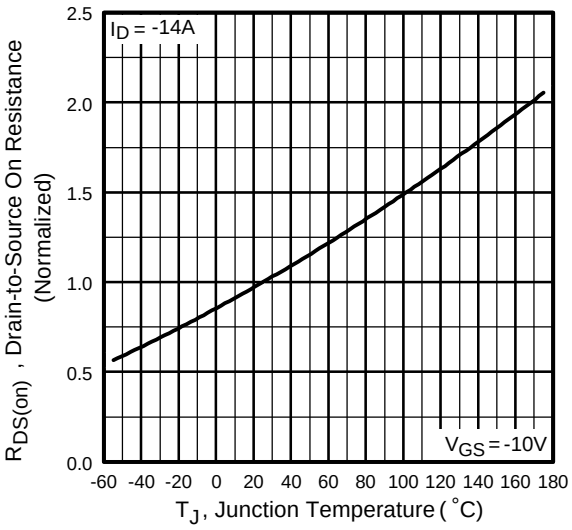



**Fig 4.** Normalized On-Resistance Vs. Temperature

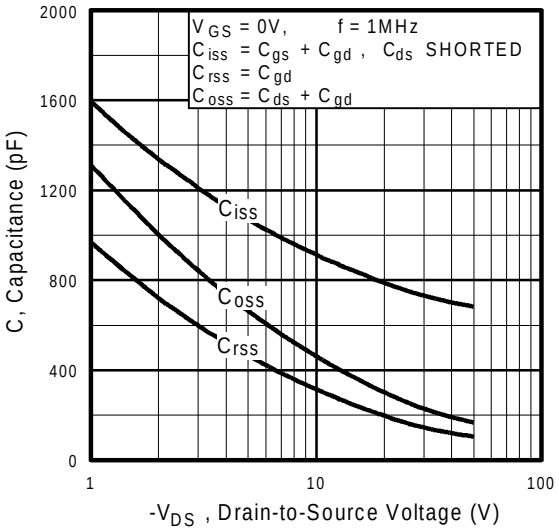



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

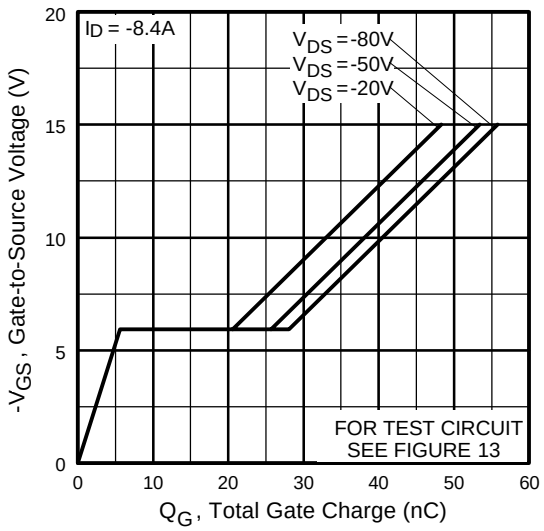



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

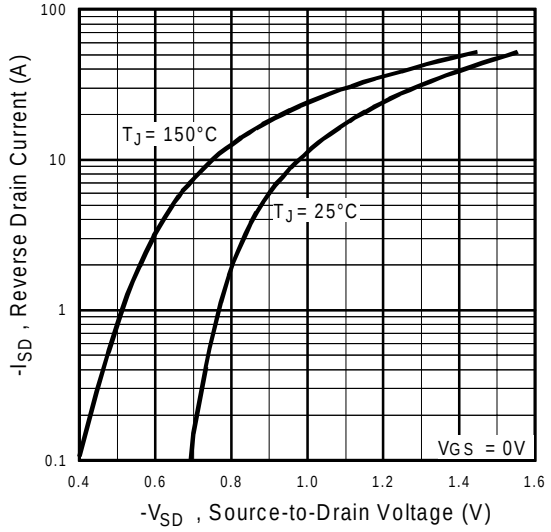



**Fig 7.** Typical Source-Drain Diode Forward Voltage

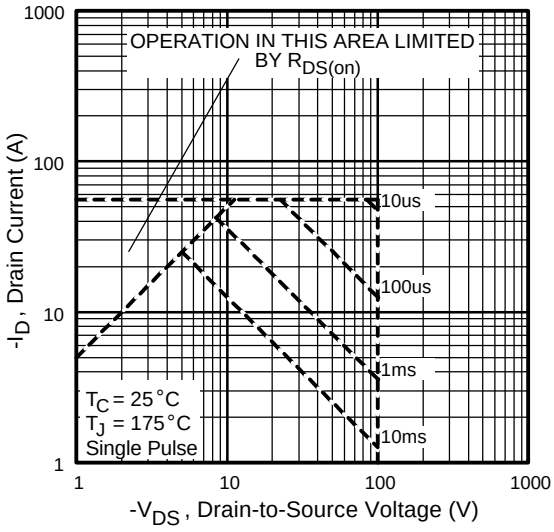



**Fig 8.** Maximum Safe Operating Area

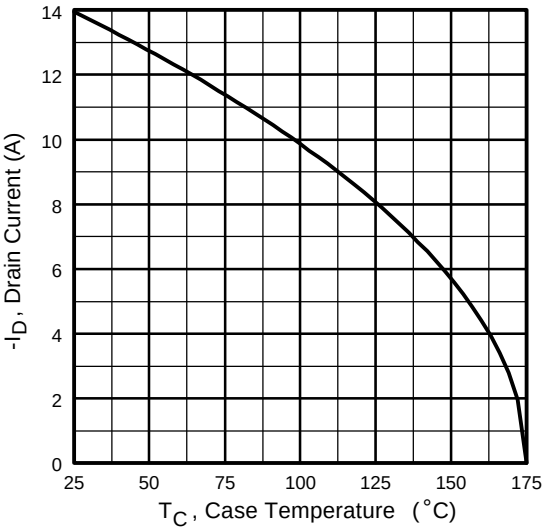



**Fig 9.** Maximum Drain Current Vs. Case Temperature

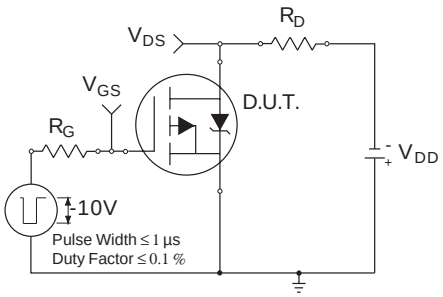



**Fig 10a.** Switching Time Test Circuit

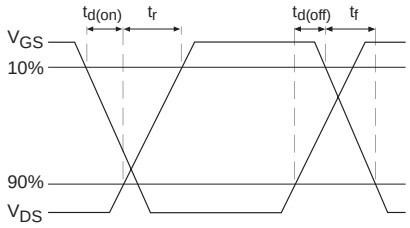



**Fig 10b.** Switching Time Waveforms

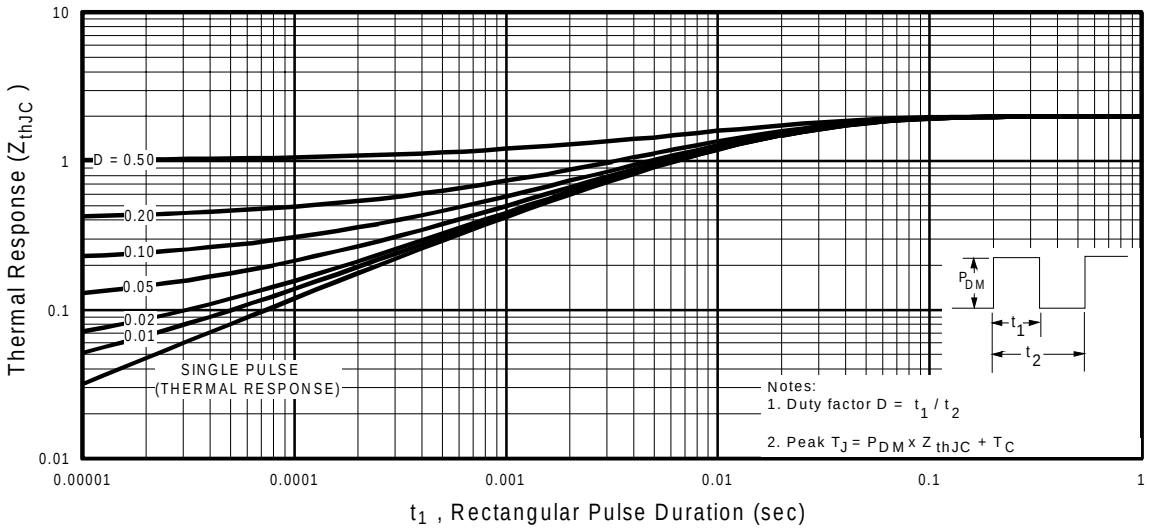



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

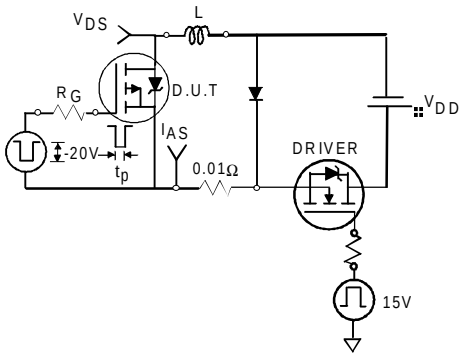



**Fig 12a.** Unclamped Inductive Test Circuit

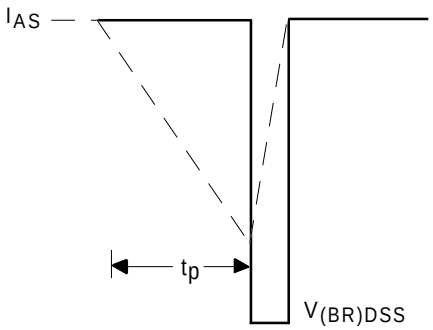



**Fig 12b.** Unclamped Inductive Waveforms

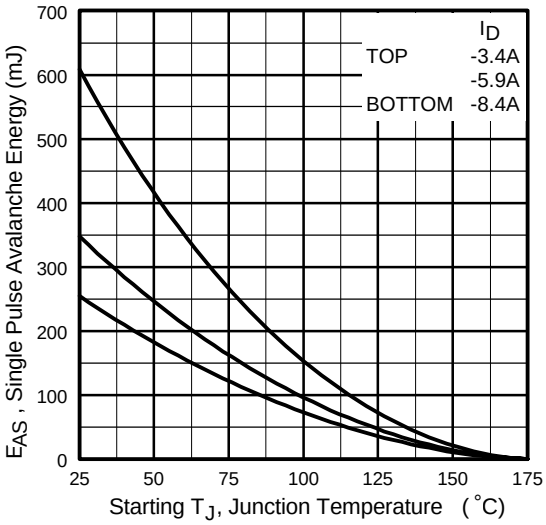



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

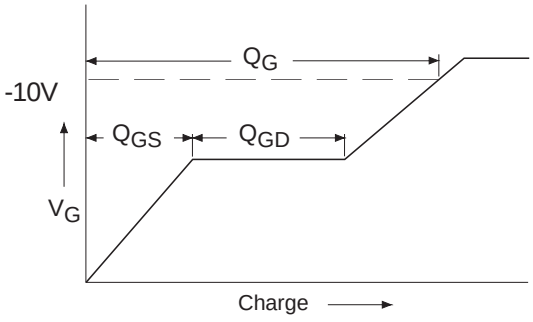



**Fig 13a.** Basic Gate Charge Waveform

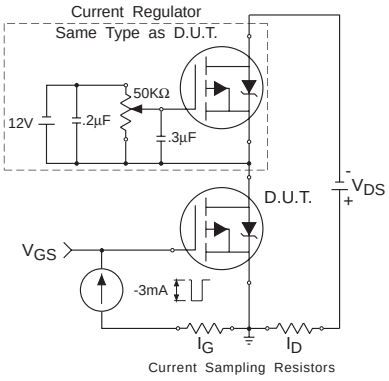
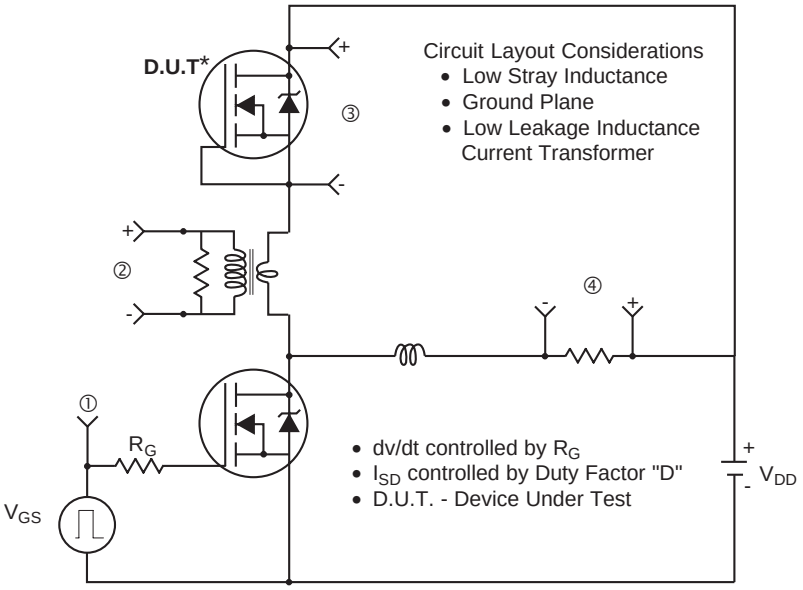
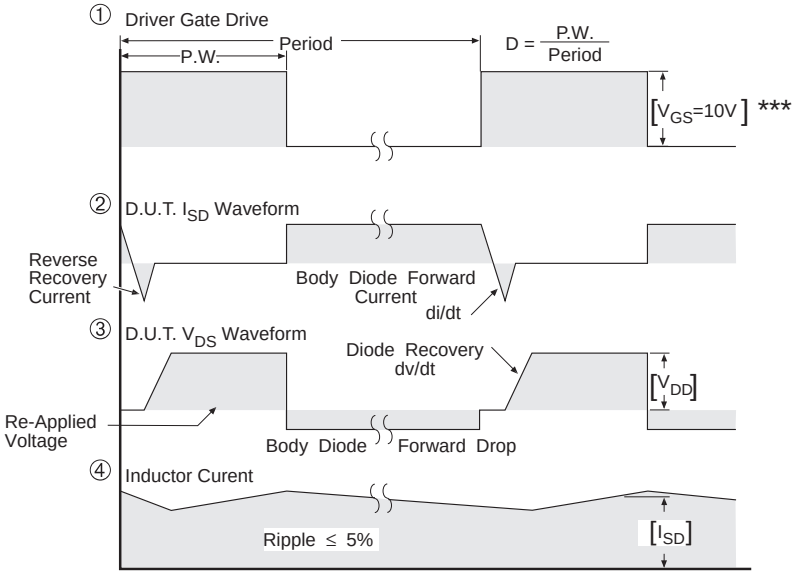



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit

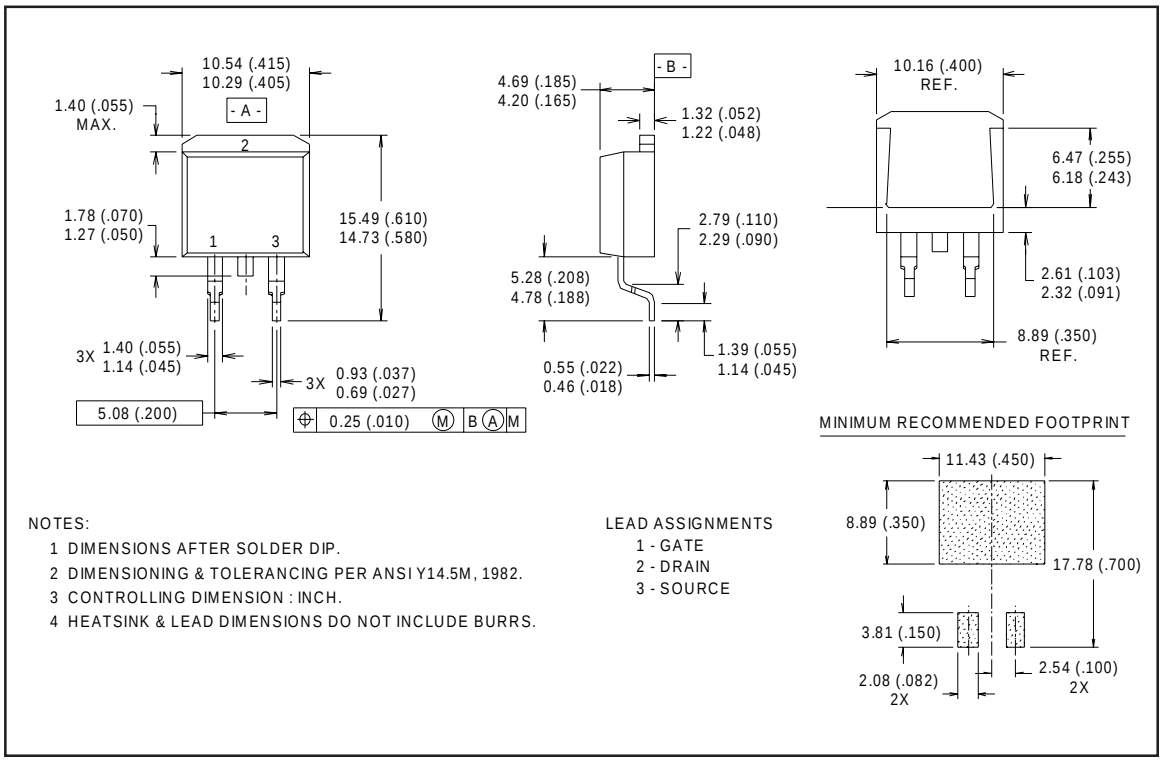



* Reverse Polarity of D.U.T for P-Channel



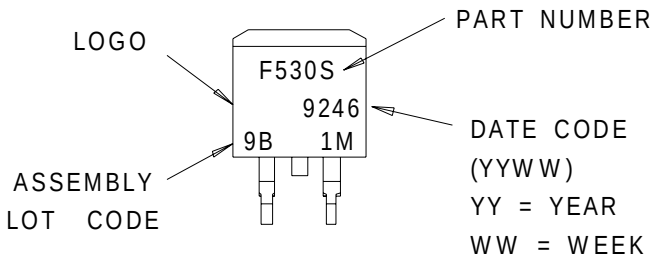

*** $V_{GS}$ = 5.0V for Logic Level and 3V Drive Devices

## D²Pak Package Outline



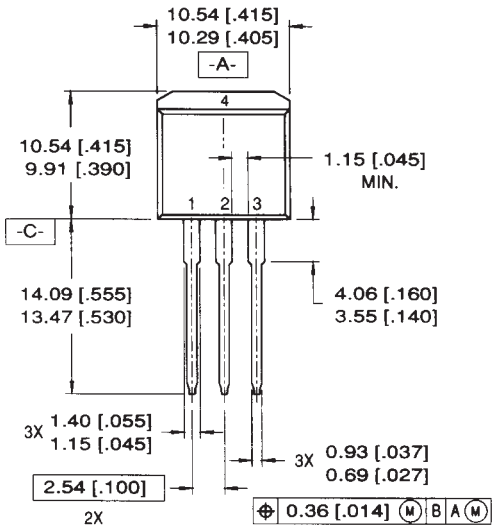

## Part Marking Information

**D²Pak**



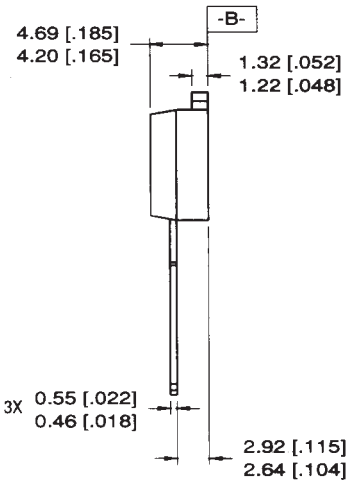
## Package Outline

**TO-262 Outline**




LEAD ASSIGNMENTS

1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN



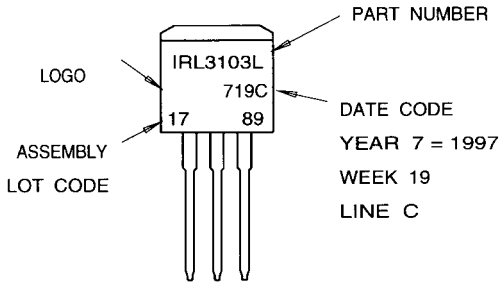

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## Part Marking Information

**TO-262**

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



## Tape & Reel Information

**D²Pak**