TOSHIBA CMOS Integrated Circuit Silicon Monolithic

TC62D776CFG

16-Channel Constant-Current LED Driver of the 3.3-V and 5-V Power Supply

The TC62D776CFG is a constant-current driver for LED and LED display lighting applications.

The output current from each of the 16 outputs is programmable via a single external resistor.

The TC62D776CFG contains a 16-channel shift register, a 16-channel latch, a 16-channel AND gate and a 16-channel constant-current output.

Fabricated with a CMOS process, the TC62D776CFG allows high-speed data transfer.

It operates with a 3.3- or 5-V power supply.

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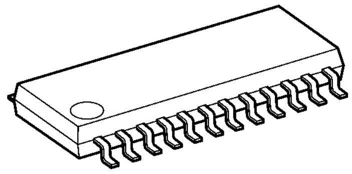


SSOP24-P-300-1.00B

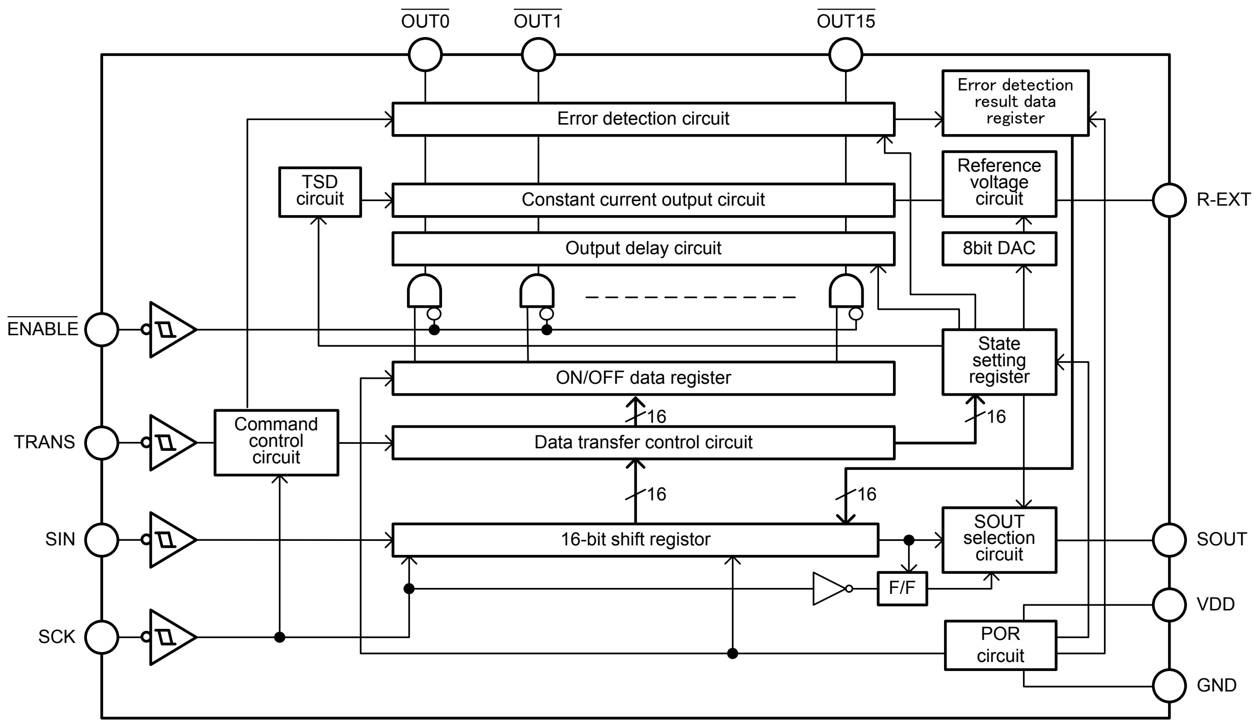
Weight : 0.32g Typ.

Features

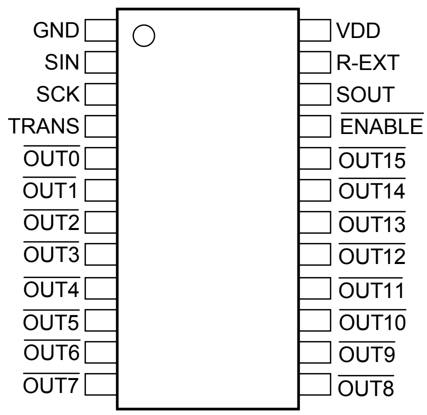
● Supply voltage : V_{DD} = 3.0 to 5.5 V
● 16-output built-in
● Output current setup range : I_{OUT} = 1.5 to 90 mA
● Constant current output accuracy (@ R_{EXT} = 1.2 kΩ, V_{OUT} = 1.0 V, V_{DD} = 3.3 V, 5.0 V)
: S rank; between outputs ± 1.5 % (max)
: S rank; between devices ± 1.5 % (max)
: N rank; between outputs ± 2.5 % (max)
: N rank; between devices ± 2.5 % (max)
●Output voltage : V_{OUT} = 17 V (max)
● I/O interface : CMOS interfaces (Schmitt trigger input)
● Data transfer frequency : f_{SCK} = 25 MHz (max)
● Operation temperature range : T_{opr} = –40 to 85 °C
● 8-bit (256 steps) current correction function built-in.
1 bit (HC) by the MSB side: Selects the output current range.
7 bit by the LSB side: Output current is adjusted at 128 steps in the range of 11% to 45%. (In the case of HC=1)
Output current is adjusted at 128 steps in the range of 50% to 200%. (In the case of HC=0)
● Thermal shutdown function (TSD) built-in.
● Output error detection function built-in.
Auto-output error detection and manual-output error detection using commands
Output open detection function (OOD) and output short detection function (OSD) built-in.
● Power-on-reset function built-in. (When the power supply is turned on, internal data is reset)
● Stand-by function built-in. (I_{DD} = 1μA at standby mode)
● Output delay function built-in. (Output switching noise is reduced)
● Package : SSOP24-P-300-1.00B

For detailed part naming conventions, contact your local Toshiba sales representative or distributor.

Block Diagram



Pin Assignment (top view)

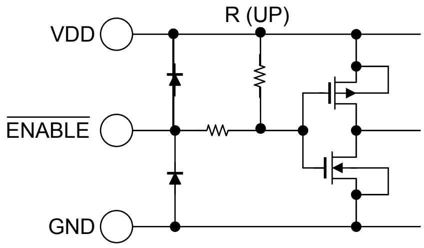


Terminal Description

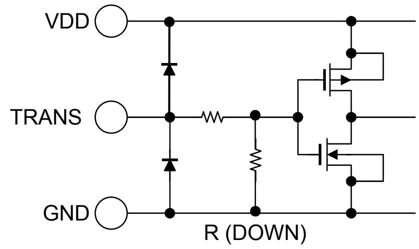
Pin No.	Pin Name	Function
1	GND	GND terminal
2	SIN	Serial data input terminal
3	SCK	Serial data transfer clock input terminal
4	TRANS	Data transfer command input terminal
5	$\overline{\text{OUT0}}$	Constant-current output terminal
6	$\overline{\text{OUT1}}$	Constant-current output terminal
7	$\overline{\text{OUT2}}$	Constant-current output terminal
8	$\overline{\text{OUT3}}$	Constant-current output terminal
9	$\overline{\text{OUT4}}$	Constant-current output terminal
10	$\overline{\text{OUT5}}$	Constant-current output terminal
11	$\overline{\text{OUT6}}$	Constant-current output terminal
12	$\overline{\text{OUT7}}$	Constant-current output terminal
13	$\overline{\text{OUT8}}$	Constant-current output terminal
14	$\overline{\text{OUT9}}$	Constant-current output terminal
15	$\overline{\text{OUT10}}$	Constant-current output terminal
16	$\overline{\text{OUT11}}$	Constant-current output terminal
17	$\overline{\text{OUT12}}$	Constant-current output terminal
18	$\overline{\text{OUT13}}$	Constant-current output terminal
19	$\overline{\text{OUT14}}$	Constant-current output terminal
20	$\overline{\text{OUT15}}$	Constant-current output terminal
21	$\overline{\text{ENABLE}}$	An output current enable signal input terminal In "H" level input, outputs are turned off compulsorily. In "L" level input, outputs are ON/OFF controlled according to serial data.
22	SOUT	Serial data output terminal.
23	R-EXT	An external resistance for an output current setup is connected between this terminal and ground.
24	VDD	Power supply terminal

Equivalent Circuits for Inputs and Outputs

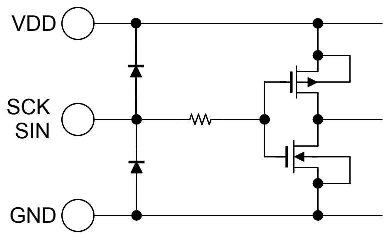
$\overline{\text{ENABLE}}$ Terminal



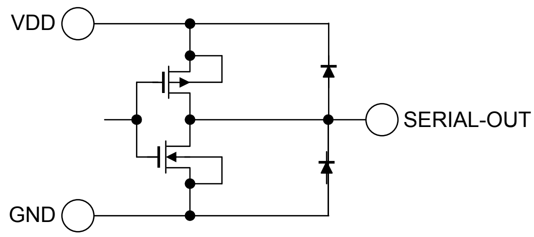
TRANS Terminal



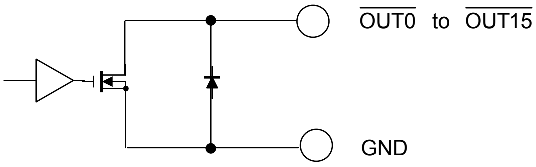
SCK and SIN Terminals



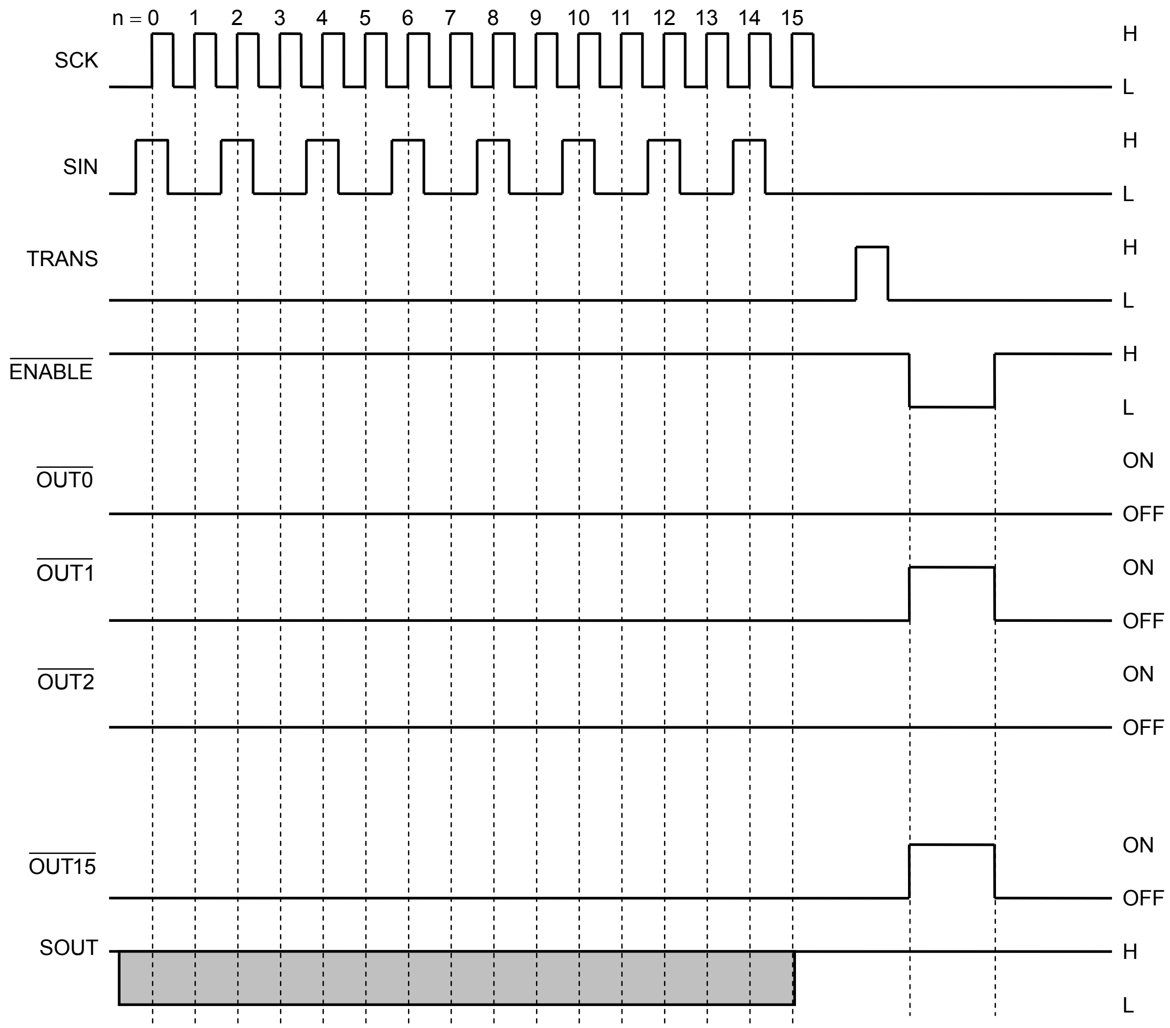
SOUT Terminal



$\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ Terminals



Timing Diagram



The TC62D776CFG can operate with a 3.3- or 5.0-V power supply. The same voltage must be supplied to the power and signal (SCK/SIN/TRANS/$\overline{\text{ENABLE}}$) domains.

The explanation of the function (Basic data input pattern)

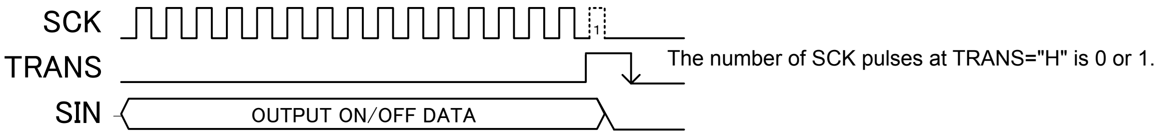
Data is serially loaded into the TC62D776CFG using the SIN and SCK inputs. Command selection is done via the SCK and TRANS inputs.

About the operation of each command

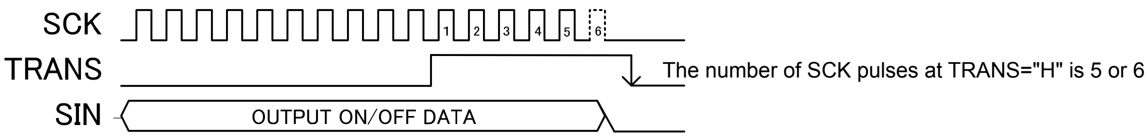
Symbol	Num of SCK at TRANS="H" (Note2)	Operation
S0	0,1	Input of output ON/OFF data.
S1	5,6	Executes output open/short detection manually. (Note1) Transfers the result of open/short detection to the 16-bit Shift Register. (Note1)
S2	7,8	Input of state setting data (1).
S3	9,10	Input of state setting data (2).

Note 1: When output open/short detection is enabled.
Note 2: SCK pulse trains other than those shown above are not recognized as commands.

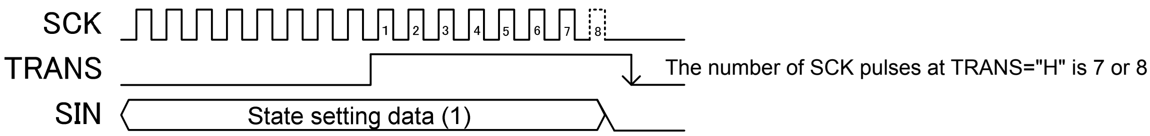
•S0 command (Input of output ON/OFF data.)



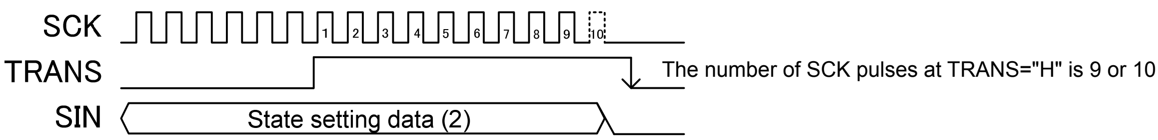
•S1 command (Output open/short detection function manual operation is executed.)



•S2 command (Input of state setting data (1).)



•S3 command (Input of state setting data (2).)



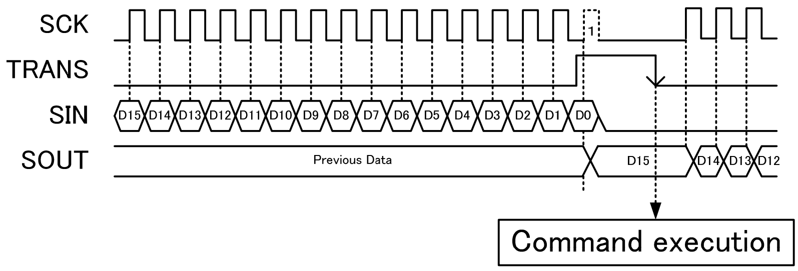
About the operation of each command

S0 command (Input of output ON/OFF data.)

Description

If SCK pulses High zero or one time while TRANS is High, it is interpreted as the S0 command, which acts as follows.

Basic input pattern of S0 command



Input form of output ON/OFF data

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{OUT15}}$	$\overline{\text{OUT14}}$	$\overline{\text{OUT13}}$	$\overline{\text{OUT12}}$	$\overline{\text{OUT11}}$	$\overline{\text{OUT10}}$	$\overline{\text{OUT9}}$	$\overline{\text{OUT8}}$	$\overline{\text{OUT7}}$	$\overline{\text{OUT6}}$	$\overline{\text{OUT5}}$	$\overline{\text{OUT4}}$	$\overline{\text{OUT3}}$	$\overline{\text{OUT2}}$	$\overline{\text{OUT1}}$	$\overline{\text{OUT0}}$

Input in MSB first.

Output ON/OFF data setting

Input Data	Setting
1	Output turn on
0	Output turn off

Default after power-on

Data	Setting
0	Output turn off

Automatic Error Detection Mode

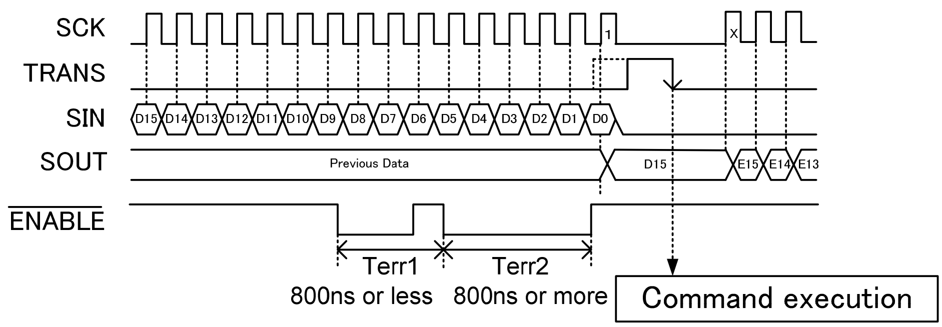
If output open/short detection is enabled, its result is automatically transferred from the Error Detection Result register to the 16-bit Shift Register, which can be shifted out from the SOUT pin.

Output open/short detection can be enabled with the S3 command.

Open/short errors can be detected only for output channels that are enabled for at least 800 ns (Note 1) and are configured to be turned on. For the disabled output channels, the detection result will be 1 (normal). If the output channels stay on for no longer than 800 ns, the automatic error detection result will be invalid; in this case, the detection results of all channels will be 1 (normal).

Note 1: Automatic error detection is triggered by the falling edge of the $\overline{\text{ENABLE}}$ signal. Thus, this feature can not be used when $\overline{\text{ENABLE}}$ is tied Low.

In the figure shown below, the outputs are enabled for over 800 ns during the Terr2 period, but the automatic error detection result is invalid; thus, it should be kept in mind that the detection results will be 1 (normal) for all channels.



Output form of output opening/short detection result data

The result of output open/short detection is transferred to the 16-bit Shift Register in the format shown below.

MSB LSB

E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0
$\overline{OUT15}$	$\overline{OUT14}$	$\overline{OUT13}$	$\overline{OUT12}$	$\overline{OUT11}$	$\overline{OUT10}$	$\overline{OUT9}$	$\overline{OUT8}$	$\overline{OUT7}$	$\overline{OUT6}$	$\overline{OUT5}$	$\overline{OUT4}$	$\overline{OUT3}$	$\overline{OUT2}$	$\overline{OUT1}$	$\overline{OUT0}$

Error code (when output open detection function is effective)

Judging in error detection	Error code	Condition of output terminal
$V_{OOD} \geq V_{OUT}$	0	Open
$V_{OOD} < V_{OUT}$	1	Normal

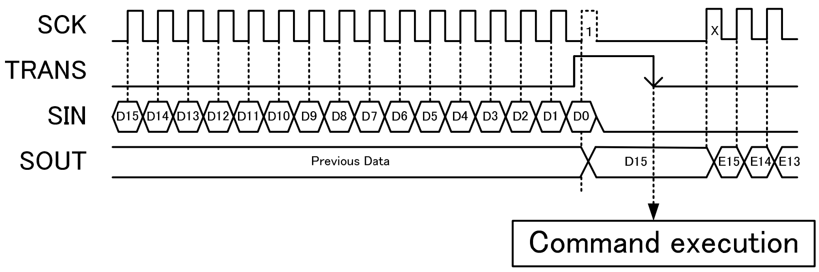
Error code (when output short detection function is effective)

Judging in error detection	Error code	Condition of output terminal
$V_{OSD} \leq V_{OUT}$	0	short-circuit
$V_{OSD} > V_{OUT}$	1	Normal

Error code (when output open/short detection function is effective)

Judging in error detection	Error code	Condition of output terminal
$V_{OOD} \geq V_{OUT}$ or $V_{OSD} \leq V_{OUT}$	0	Open or short-circuit
$V_{OOD} < V_{OUT}$ or $V_{OSD} > V_{OUT}$	1	Normal
*When both output error detection function is effective, Open and short-circuit are undistinguishable.		

Basic input pattern of S0 command （When output opening/short detection is effective.）



After the S0 command is loaded, the first SCK pulse (marked X above) is used to transfer an error detection result to the 16-bit Shift Register. At this time, the TC62D776CFG ignores the SIN input.

S1 command (Output open/short detection function manual operation is executed.)

Description

If SCK pulses High five or six times while TRANS is High, it is interpreted as the S1 command, which acts as follows.

If output open/short detection is enabled, a current of approximately 60 μA is forced to flow to all the outputs during the $t_{ON(S1)}$ period in order to perform open/short detection. $t_{ON(S1)}$ is approximately 800 ns long.

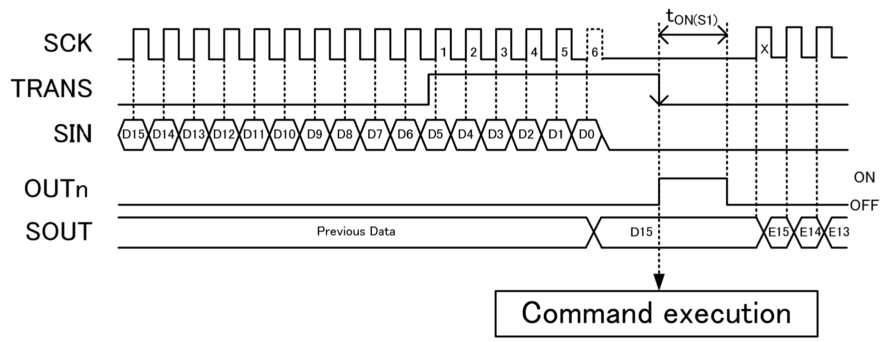
Its result is immediately transferred to the 16-bit Shift Register, which can be shifted out from the SOUT pin.

The format used to transfer the detection result is the same as for the S0 command.

Output open/short detection can be enabled with the S3 command.

Note: The S1 command should be loaded when the outputs are off. The S1 command is not executed if it is loaded when $\overline{\text{ENABLE}}$ = Low.The S1 command is not also executed when output open/short detection is disabled.
SCK should not be applied during the $t_{ON(S1)}$ period.

Basic input pattern of S1 command



After the S1 command is loaded, the first SCK pulse (marked X above) is used to transfer an error detection result to the 16-bit Shift Register. At this time, the TC62D776CFG ignores the SIN input.

S2 command (Input of state setting data (1).)

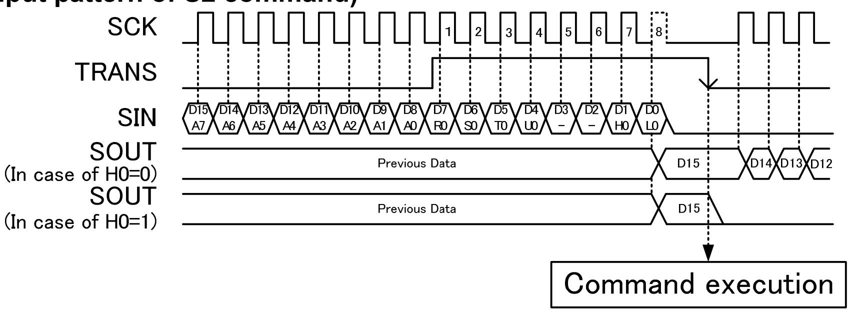
Description

If SCK pulses High seven or eight times while TRANS is High, it is interpreted as the S0 command, which acts as follows.

The TC62D776CFG transfers the state control data (1) from the 16-bit Shift Register to the State Control register.

The states that can be programmed with the S2 command are shown below.

Basic input pattern of S2 command)



Input form of state setting data (1)

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	A2	A1	A0	R0	S0	T0	U0	-	-	H0	L0

*Input in MSB first.

*Please input "L" data to D7 to D2.

State setting data (1) setting

Setting bit	Outline of command	Input data		Default after power-on
		0	1	
A7	Setting of current correction range	High set mode 50% to 200%	Low set mode 11% to 45%	High set mode 50% to 200%
A6 to A0	Setting of current correction data	Refer to attached table.		100%
R0 to U0	TEST Mode setting. Please input "L" data.			"L"
H0	Data Initialization	Normal	Initialization	Normal
L0	Setting of standby mode (1)	Normal	Active	Normal

Details of each setting

A setting (setting of current correction data)

1. In the case of a high setting mode (50% to 200%)

A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Current gain(%)
1	1	1	1	1	1	1	200.00
1	1	1	1	1	1	0	198.82
1	1	1	1	1	0	1	197.64
1	1	1	1	1	0	0	196.46
1	1	1	1	0	1	1	195.28
1	1	1	1	0	1	0	194.09
1	1	1	1	0	0	1	192.91
1	1	1	1	0	0	0	191.73
1	1	1	0	1	1	1	190.55
1	1	1	0	1	1	0	189.37
1	1	1	0	1	0	1	188.19
1	1	1	0	1	0	0	187.01
1	1	1	0	0	1	1	185.83
1	1	1	0	0	1	0	184.65
1	1	1	0	0	0	1	183.46
1	1	1	0	0	0	0	182.28
1	1	0	1	1	1	1	181.10
1	1	0	1	1	1	0	179.92
1	1	0	1	1	0	1	178.74
1	1	0	1	1	0	0	177.56
1	1	0	1	0	1	1	176.38
1	1	0	1	0	1	0	175.20
1	1	0	1	0	0	1	174.02
1	1	0	1	0	0	0	172.83
1	1	0	0	1	1	1	171.65
1	1	0	0	1	1	0	170.47
1	1	0	0	1	0	1	169.29
1	1	0	0	1	0	0	168.11
1	1	0	0	0	1	1	166.93
1	1	0	0	0	1	0	165.75
1	1	0	0	0	0	1	164.57
1	1	0	0	0	0	0	163.39
1	0	1	1	1	1	1	162.20
1	0	1	1	1	1	0	161.02
1	0	1	1	1	0	1	159.84
1	0	1	1	1	0	0	158.66
1	0	1	1	0	1	1	157.48
1	0	1	1	0	1	0	156.30
1	0	1	1	0	0	1	155.12
1	0	1	1	0	0	0	153.94
1	0	1	0	1	1	1	152.76
1	0	1	0	1	1	0	151.57
1	0	1	0	1	0	1	150.39
1	0	1	0	1	0	0	149.21
1	0	1	0	0	1	1	148.03
1	0	1	0	0	1	0	146.85
1	0	1	0	0	0	1	145.67
1	0	1	0	0	0	0	144.49
1	0	0	1	1	1	1	143.31
1	0	0	1	1	1	0	142.13
1	0	0	1	1	0	1	140.94
1	0	0	1	1	0	0	139.76
1	0	0	1	0	1	1	138.58
1	0	0	1	0	1	0	137.40
1	0	0	1	0	0	1	136.22
1	0	0	1	0	0	0	135.04
1	0	0	0	1	1	1	133.86
1	0	0	0	1	1	0	132.68
1	0	0	0	1	0	1	131.50
1	0	0	0	1	0	0	130.31
1	0	0	0	0	1	1	129.13
1	0	0	0	0	1	0	127.95
1	0	0	0	0	0	1	126.77
1	0	0	0	0	0	0	125.59

A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Current gain(%)
0	1	1	1	1	1	1	124.41
0	1	1	1	1	1	0	123.23
0	1	1	1	1	0	1	122.05
0	1	1	1	1	0	0	120.87
0	1	1	1	0	1	1	119.69
0	1	1	1	0	1	0	118.50
0	1	1	1	0	0	1	117.32
0	1	1	1	0	0	0	116.14
0	1	1	0	1	1	1	114.96
0	1	1	0	1	1	0	113.78
0	1	1	0	1	0	1	112.60
0	1	1	0	1	0	0	111.42
0	1	1	0	0	1	1	110.24
0	1	1	0	0	1	0	109.06
0	1	1	0	0	0	1	107.87
0	1	1	0	0	0	0	106.69
0	1	0	1	1	1	1	105.51
0	1	0	1	1	1	0	104.33
0	1	0	1	1	0	1	103.15
0	1	0	1	1	0	0	101.97
0	**1**	**0**	**1**	**0**	**1**	**1**	**100.79 (Default)**
0	1	0	1	0	1	0	99.61
0	1	0	1	0	0	1	98.43
0	1	0	1	0	0	0	97.24
0	1	0	0	1	1	1	96.06
0	1	0	0	1	1	0	94.88
0	1	0	0	1	0	1	93.70
0	1	0	0	1	0	0	92.52
0	1	0	0	0	1	1	91.34
0	1	0	0	0	1	0	90.16
0	1	0	0	0	0	1	88.98
0	1	0	0	0	0	0	87.80
0	0	1	1	1	1	1	86.61
0	0	1	1	1	1	0	85.43
0	0	1	1	1	0	1	84.25
0	0	1	1	1	0	0	83.07
0	0	1	1	0	1	1	81.89
0	0	1	1	0	1	0	80.71
0	0	1	1	0	0	1	79.53
0	0	1	1	0	0	0	78.35
0	0	1	0	1	1	1	77.17
0	0	1	0	1	1	0	75.98
0	0	1	0	1	0	1	74.80
0	0	1	0	1	0	0	73.62
0	0	1	0	0	1	1	72.44
0	0	1	0	0	1	0	71.26
0	0	1	0	0	0	1	70.08
0	0	1	0	0	0	0	68.90
0	0	0	1	1	1	1	67.72
0	0	0	1	1	1	0	66.54
0	0	0	1	1	0	1	65.35
0	0	0	1	1	0	0	64.17
0	0	0	1	0	1	1	62.99
0	0	0	1	0	1	0	61.81
0	0	0	1	0	0	1	60.63
0	0	0	1	0	0	0	59.45
0	0	0	0	1	1	1	58.27
0	0	0	0	1	1	0	57.09
0	0	0	0	1	0	1	55.91
0	0	0	0	1	0	0	54.72
0	0	0	0	0	1	1	53.54
0	0	0	0	0	1	0	52.36
0	0	0	0	0	0	1	51.18
0	0	0	0	0	0	0	50.00

2. In the case of a low setting mode (11% to 45%)

A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Current gain(%)
1	1	1	1	1	1	1	45.00
1	1	1	1	1	1	0	44.73
1	1	1	1	1	0	1	44.46
1	1	1	1	1	0	0	44.20
1	1	1	1	0	1	1	43.93
1	1	1	1	0	1	0	43.66
1	1	1	1	0	0	1	43.39
1	1	1	1	0	0	0	43.13
1	1	1	0	1	1	1	42.86
1	1	1	0	1	1	0	42.59
1	1	1	0	1	0	1	42.32
1	1	1	0	1	0	0	42.06
1	1	1	0	0	1	1	41.79
1	1	1	0	0	1	0	41.52
1	1	1	0	0	0	1	41.25
1	1	1	0	0	0	0	40.98
1	1	0	1	1	1	1	40.72
1	1	0	1	1	1	0	40.45
1	1	0	1	1	0	1	40.18
1	1	0	1	1	0	0	39.91
1	1	0	1	0	1	1	39.65
1	1	0	1	0	1	0	39.38
1	1	0	1	0	0	1	39.11
1	1	0	1	0	0	0	38.84
1	1	0	0	1	1	1	38.57
1	1	0	0	1	1	0	38.31
1	1	0	0	1	0	1	38.04
1	1	0	0	1	0	0	37.77
1	1	0	0	0	1	1	37.50
1	1	0	0	0	1	0	37.24
1	1	0	0	0	0	1	36.97
1	1	0	0	0	0	0	36.70
1	0	1	1	1	1	1	36.43
1	0	1	1	1	1	0	36.17
1	0	1	1	1	0	1	35.90
1	0	1	1	1	0	0	35.63
1	0	1	1	0	1	1	35.36
1	0	1	1	0	1	0	35.09
1	0	1	1	0	0	1	34.83
1	0	1	1	0	0	0	34.56
1	0	1	0	1	1	1	34.29
1	0	1	0	1	1	0	34.02
1	0	1	0	1	0	1	33.76
1	0	1	0	1	0	0	33.49
1	0	1	0	0	1	1	33.22
1	0	1	0	0	1	0	32.95
1	0	1	0	0	0	1	32.69
1	0	1	0	0	0	0	32.42
1	0	0	1	1	1	1	32.15
1	0	0	1	1	1	0	31.88
1	0	0	1	1	0	1	31.61
1	0	0	1	1	0	0	31.35
1	0	0	1	0	1	1	31.08
1	0	0	1	0	1	0	30.81
1	0	0	1	0	0	1	30.54
1	0	0	1	0	0	0	30.28
1	0	0	0	1	1	1	30.01
1	0	0	0	1	1	0	29.74
1	0	0	0	1	0	1	29.47
1	0	0	0	1	0	0	29.20
1	0	0	0	0	1	1	28.94
1	0	0	0	0	1	0	28.67
1	0	0	0	0	0	1	28.40
1	0	0	0	0	0	0	28.13

A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Current gain(%)
0	1	1	1	1	1	1	27.87
0	1	1	1	1	1	0	27.60
0	1	1	1	1	0	1	27.33
0	1	1	1	1	0	0	27.06
0	1	1	1	0	1	1	26.80
0	1	1	1	0	1	0	26.53
0	1	1	1	0	0	1	26.26
0	1	1	1	0	0	0	25.99
0	1	1	0	1	1	1	25.72
0	1	1	0	1	1	0	25.46
0	1	1	0	1	0	1	25.19
0	1	1	0	1	0	0	24.92
0	1	1	0	0	1	1	24.65
0	1	1	0	0	1	0	24.39
0	1	1	0	0	0	1	24.12
0	1	1	0	0	0	0	23.85
0	1	0	1	1	1	1	23.58
0	1	0	1	1	1	0	23.31
0	1	0	1	1	0	1	23.05
0	1	0	1	1	0	0	22.78
0	1	0	1	0	1	1	22.51
0	1	0	1	0	1	0	22.24
0	1	0	1	0	0	1	21.98
0	1	0	1	0	0	0	21.71
0	1	0	0	1	1	1	21.44
0	1	0	0	1	1	0	21.17
0	1	0	0	1	0	1	20.91
0	1	0	0	1	0	0	20.64
0	1	0	0	0	1	1	20.37
0	1	0	0	0	1	0	20.10
0	1	0	0	0	0	1	19.83
0	1	0	0	0	0	0	19.57
0	0	1	1	1	1	1	19.30
0	0	1	1	1	1	0	19.03
0	0	1	1	1	0	1	18.76
0	0	1	1	1	0	0	18.50
0	0	1	1	0	1	1	18.23
0	0	1	1	0	1	0	17.96
0	0	1	1	0	0	1	17.69
0	0	1	1	0	0	0	17.43
0	0	1	0	1	1	1	17.16
0	0	1	0	1	1	0	16.89
0	0	1	0	1	0	1	16.62
0	0	1	0	1	0	0	16.35
0	0	1	0	0	1	1	16.09
0	0	1	0	0	1	0	15.82
0	0	1	0	0	0	1	15.55
0	0	1	0	0	0	0	15.28
0	0	0	1	1	1	1	15.02
0	0	0	1	1	1	0	14.75
0	0	0	1	1	0	1	14.48
0	0	0	1	1	0	0	14.21
0	0	0	1	0	1	1	13.94
0	0	0	1	0	1	0	13.68
0	0	0	1	0	0	1	13.41
0	0	0	1	0	0	0	13.14
0	0	0	0	1	1	1	12.87
0	0	0	0	1	1	0	12.61
0	0	0	0	1	0	1	12.34
0	0	0	0	1	0	0	12.07
0	0	0	0	0	1	1	11.80
0	0	0	0	0	1	0	11.54
0	0	0	0	0	0	1	11.27
0	0	0	0	0	0	0	11.00

R, S, T, U setting (Setting of Test Mode)

R, S, T, U[0]	Setting of Test Mode
0	**Normal operation mode. (Default after power-on)**
1	Test Mode.

H setting (Setting of Initialization)

H[0]	Setting of Initialization
0	**Normal operation mode (Default after power-on)**
1	Initializes all the internal data of the IC. After initialization, the TC62D776CFG returns to normal operation mode.

L setting (Setting of standby mode (1))

L[0]	**Setting of standby mode (1)**
0	**Normal operation mode (Default after power-on)**
1	Standby mode Disables all circuits except digital logic, reducing the supply current of the IC. (All data in the TC62D776CFG is retained, and data can be loaded into the TC62D776CFG.) Loading the S0 command in Standby mode causes the TC62D776CFG to return to normal operation mode.

S3 command (Input of state setting data (2).)

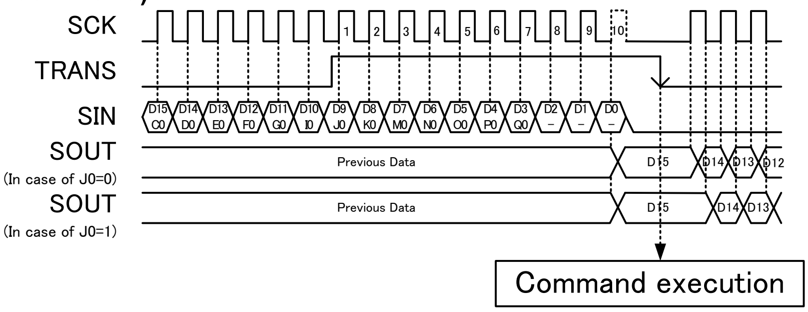
Description

If SCK pulses High nine or ten times while TRANS is High, it is interpreted as the S3 command, which acts as follows.

The TC62D776CFG transfers the state control data (2) from the 16-bit Shift Register to the State Control register.

The states that can be programmed with the S3 command are shown below.

Basic input pattern of S3 command)



Input form of state setting data (2)

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C0	D0	E0	F0	G0	I0	J0	K0	M0	N0	O0	P0	Q0	-	-	-

*Input in MSB first.
*Please input "L" data to D8 to D0.

State setting data (2) setting

Setting bit	Outline of command	Input data		Default after power-on
		0	1	
C0	Setting of thermal shutdown function (TSD)	Active	Not Active	Active
D0	Setting of output open detection function (OOD)	Not Active	Active	Not Active
E0	Setting of output short detection function (OSD)	Not Active	Active	Not Active
F0	Setting of standby mode (2)	Normal Operation	Active	Normal Operation
G0	Setting of output short detection voltage	V_{OSD1}	V_{OSD2}	V_{OSD1}
I0	Setting of output deLay function of output terminal	Active	Not Active	Active
J0	Setting of SCK trigger of SOUT	Up↑	Down↓	Up↑
K0 to Q0	TEST Mode setting. Please input "L" data.			"L"

Details of each setting

C setting (Setting of thermal shutdown function (TSD))

C[0]	Setting of thermal shutdown function
0	**Enables thermal shutdown. (Default after power-on)**
1	Disables thermal shutdown.

D setting (Setting of output open detection function (OOD))

D[0]	Setting of output open detection function
0	**Disables output error detection. (Default after power-on)**
1	Enables output error detection.

E setting (Setting of output short detection function (OSD))

E[0]	Setting of output short detection function
0	**Disables output error detection. (Default after power-on)**
1	Enables output error detection.

F setting (Setting of standby mode (2))

F[0]	Setting of standby mode (2)
0	**Normal operation mode. (Default after power-on)**
1	Pre standby mode. Condition 1: Enters Standby mode when the contents of the Latch become all-0s in normal operation mode. This disables all circuits except digital logic, reducing the supply current of the IC.(All data in the TC62D776CFG is retained, and data can be loaded into the TC62D776CFG.) Condition 2: Other than Condition 1 The TC62D776CFG operates the same way as normal operation mode.

G setting (Setting of output short detection voltage)

G[0]	Setting of output short detection voltage
0	**V_{OSD1} (Default after power-on)**
1	V_{OSD2}

I setting (Setting of output delay function of output terminal)

I[0]	Setting of output delay function of output terminal
0	**Disables output delay function. (Default after power-on)**
1	Enables output delay function.

J setting (Setting of SCK trigger of SOUT)

J[0]	Setting of SCK trigger of SOUT
0	**Data output trigger of SOUT is up edge of SCK (Default after power-on)**
1	Data output trigger of SOUT is down edge of SCK

K,M,N,O,P,Q setting (Setting of Test Mode)

K,M,N,O,P,Q[0]	Setting of Test Mode
0	**Normal operation mode. (Default after power-on)**
1	Test Mode.

Thermal shutdown function (TSD)

If the internal temperature of the IC exceeds 150°C, the thermal shutdown (TSD) circuitry trips, turning off all constant-current outputs. When the temperature drops below the TSD release threshold, the TC62D776CFG restarts constant-current output.

Since TSD is not intended to protect the IC against permanent damage. it should not be employed actively to monitor chip temperature.

Output delay function

In order to reduce di/dt caused by simultaneously switching outputs, the TC62D776CFG allows for delays ($t_{DLY\ (ON)}$, $t_{DLY\ (OFF)}$) between contiguous outputs.

Switching time difference between outputs are provided in order as follows;

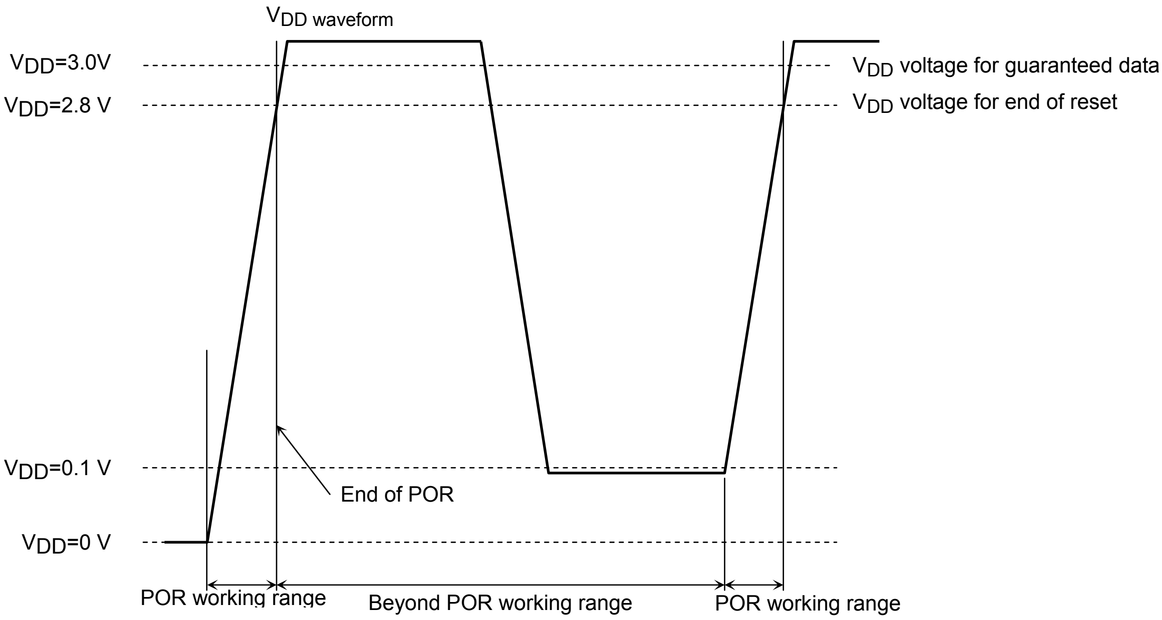
$\overline{\textbf{OUT0}} \rightarrow \overline{\textbf{OUT15}} \rightarrow \overline{\textbf{OUT7}} \rightarrow \overline{\textbf{OUT8}} \rightarrow \overline{\textbf{OUT1}} \rightarrow \overline{\textbf{OUT14}} \rightarrow \overline{\textbf{OUT6}} \rightarrow \overline{\textbf{OUT9}} \rightarrow \overline{\textbf{OUT2}} \rightarrow \overline{\textbf{OUT13}} \rightarrow$

$\overline{\textbf{OUT5}} \rightarrow \overline{\textbf{OUT10}} \rightarrow \overline{\textbf{OUT3}} \rightarrow \overline{\textbf{OUT12}} \rightarrow \overline{\textbf{OUT4}} \rightarrow \overline{\textbf{OUT11}}$

Power on reset function (POR)

The TC62D776CFG provides a power-on reset to reset all internal data in order to prevent malfunctions.

The POR circuitry works properly only when V_{DD} rises from 0 V. To re-activate the POR circuitry, V_{DD} must be brought to less than 0.1 V. Internal data is guaranteed to be retained after V_{DD} exceeds 3.0 V.



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}	6.0	V
Output current	I_{OUT}	95	mA
Logic input voltage	V_{IN}	–0.3 to V_{DD} + 0.3 (Note 1)	V
Output voltage	V_{OUT}	–0.3 to 17	V
Operating temperature	T_{opr}	–40 to 85	°C
Storage temperature	T_{stg}	–55 to 150	°C
Thermal resistance	$R_{th(j-a)}$	94 (Note 2)	°C/W
Power dissipation	P_D	1.32 (Notes 2 and 3)	W

Note 1: However, do not exceed 6.0 V.

Note 2: When mounted on a PCB (76.2 × 114.3 × 1.6 mm; Cu = 30%; 35-μm-thick; SEMI-compliant)

Note 3: Power dissipation is reduced by $1/R_{th\ (j-a)}$ for each °C above 25°C ambient.

Operating Ranges (unless otherwise specified, V_{DD} = 3.0 to 5.5 V, Ta = –40°C to 85°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	3.0	—	5.5	V
High level logic input voltage	V_{IH}	Test terminal are SIN, SCK, TRANS, $\overline{\text{ENABLE}}$	0.7×V_{DD}	—	V_{DD}	V
Low level logic input voltage	V_{IL}	Test terminal are SIN, SCK, TRANS, $\overline{\text{ENABLE}}$	GND	—	0.3×V_{DD}	V
High level SOUT output current	I_{OH}	—	—	—	–1	mA
Low level SOUT output current	I_{OL}	—	—	—	1	mA
Constant current output	I_{OUT}	Test terminal is $\overline{\text{OUTn}}$	1.5	—	90	mA

AC Characteristics (Unless otherwise noted, V_{DD} = 5.0 V, T_a = 25 °C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Serial data transfer frequency	f_{SCK}	Cascade connect	—	—	25	MHz
SCK pulse width	t_{wSCK}	SCK="H" or "L"	20	—	—	ns
TRANS pulse width	t_{wTRANS}	TRANS="H"	20	—	—	ns
$\overline{\text{ENABLE}}$ pulse width	t_{wENA}	$\overline{\text{ENABLE}}$ ="H" or "L" R_{EXT} =200 Ω to 12 kΩ	25	—	—	ns
Serial data setup time	t_{SETUP1}	Test terminal are SIN-SCK	1	—	—	ns
	t_{SETUP2}	Test terminal are TRANS-SCK	5	—	—	
Serial data hold time	t_{HOLD1}	Test terminal are SIN-SCK	3	—	—	ns
	t_{HOLD2}	Test terminal are TRANS-SCK	7	—	—	

AC Characteristics (Unless otherwise noted, V_{DD} = 3.3 V, T_a = 25 °C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Serial data transfer frequency	f_{SCK}	Cascade connect	—	—	25	MHz
SCK pulse width	t_{wSCK}	SCK="H" or "L"	20	—	—	ns
TRANS pulse width	t_{wTRANS}	TRANS="H"	20	—	—	ns
$\overline{\text{ENABLE}}$ pulse width	t_{wENA}	$\overline{\text{ENABLE}}$ ="H" or "L" R_{EXT} =200 Ω to 12 kΩ	25	—	—	ns
Serial data setup time	t_{SETUP1}	Test terminal are SIN-SCK	1	—	—	ns
	t_{SETUP2}	Test terminal are TRANS-SCK	5	—	—	
Serial data hold time	t_{HOLD1}	Test terminal are SIN-SCK	3	—	—	ns
	t_{HOLD2}	Test terminal are TRANS-SCK	7	—	—	

Electrical Characteristics (Unless otherwise specified, V_{DD} = 5.0 V ,Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Conditions		Min	Typ.	Max	Unit
High level SOUT output voltage	V_{OH}	1	T_a=-40 to +85°C	I_{OH}=−1mA	V_{DD} − 0.3	—	V_{DD}	V
Low level SOUT output voltage	V_{OL}	1		I_{OL}=+1mA	GND	—	0.3	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD} Test terminal are $\overline{ENABLE}$, SIN, SCK		—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND Test terminal are SIN, SCK, TRANS		—	—	-1	μA
Power supply current	I_{DD1}	4	Stand-by mode, V_{OUT}=1.0V, SCK="L"		—	—	1.0	μA
	I_{DD2}	4	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, All output off		—	—	7.0	mA
Constant current error (IC to IC) (S rank)	$\Delta I_{OUT(IC)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{OUT0}$ to $\overline{OUT15}$, 1ch output on		—	±1.0	±1.5	%
Constant current error (Ch to Ch) (S rank)	$\Delta I_{OUT(Ch)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{OUT0}$ to $\overline{OUT15}$, 1ch output on		—	±1.0	±1.5	%
Constant current error (IC to IC) (N rank)	$\Delta I_{OUT(IC)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{OUT0}$ to $\overline{OUT15}$, 1ch output on		—	±1.0	±2.5	%
Constant current error (Ch to Ch) (N rank)	$\Delta I_{OUT(Ch)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{OUT0}$ to $\overline{OUT15}$, 1ch output on		—	±1.0	±2.5	%
Output OFF leak current	I_{OK}	5	V_{OUT}=17V, R_{EXT}=1.2kΩ, $\overline{OUTn}$ off		—	—	0.5	μA
Constant current output power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=4.5 to 5.5V, V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{OUT0}$ to $\overline{OUT15}$, 1ch output on		—	±1	±5	%/V
Constant current output output voltage regulation	$\%V_{OUT}$	5	V_{OUT}=1.0 to 3.0V, R_{EXT}=1.2kΩ, $\overline{OUT0}$ to $\overline{OUT15}$, 1ch output on		—	±0.1	±0.5	%/V
Pull-up resistor	$R_{(Up)}$	3	Test terminal is $\overline{ENABLE}$		240	300	360	kΩ
Pull-down resistor	$R_{(Down)}$	2	Test terminal is TRANS		240	300	360	kΩ
OOD voltage	V_{OOD}	7	R_{EXT}=200Ω to 12kΩ		0.2	0.3	0.4	V
OSD voltage	V_{OSD1}	7	R_{EXT}=200Ω to 12kΩ		V_{DD} − 1.3	V_{DD} − 1.4	V_{DD} − 1.5	V
	V_{OSD2}	7	R_{EXT}=200Ω to 12kΩ		0.5 × V_{DD}	0.525 × V_{DD}	0.55 × V_{DD}	
TSD start temperature	$T_{TSD(ON)}$	—	Junction temperature		150	—	—	°C
Return time of normal mode from SHDN mode	t_{ON}	—	Time until output current after it becomes the Normal mode from SHDN mode flows		—	—	30	μs

Electrical Characteristics (Unless otherwise specified, V_{DD} = 3.3 V ,Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Conditions	Min	Typ.	Max	Unit
High level SOUT output voltage	V_{OH}	1	T_a=-40 to +85°C, I_{OH}=−1mA	V_{DD} − 0.3	—	V_{DD}	V
Low level SOUT output voltage	V_{OL}	1	T_a=-40 to +85°C, I_{OL}=+1mA	GND	—	0.3	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD} Test terminal are $\overline{\text{ENABLE}}$, SIN, SCK	—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND Test terminal are SIN, SCK, TRANS	—	—	-1	μA
Power supply current	I_{DD1}	4	Stand-by mode, V_{OUT}=1.0V, SCK="L"	—	—	1.0	μA
	I_{DD2}	4	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, All output off	—	—	7.0	mA
Constant current error (IC to IC) (S rank)	$\Delta I_{OUT(IC)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$, 1ch output on	—	±1.0	±1.5	%
Constant current error (Ch to Ch) (S rank)	$\Delta I_{OUT(Ch)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$, 1ch output on	—	±1.0	±1.5	%
Constant current error (IC to IC) (N rank)	$\Delta I_{OUT(IC)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$, 1ch output on	—	±1.0	±2.5	%
Constant current error (Ch to Ch) (N rank)	$\Delta I_{OUT(Ch)}$	5	V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$, 1ch output on	—	±1.0	±2.5	%
Output OFF leak current	I_{OK}	5	V_{OUT}=17V, R_{EXT}=1.2kΩ, $\overline{\text{OUTn}}$ off	—	—	0.5	μA
Constant current output power supply voltage regulation	$\%V_{DD}$	5	V_{DD}=3.0 to 3.6V, V_{OUT}=1.0V, R_{EXT}=1.2kΩ, $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$, 1ch output on	—	±1	±5	%/V
Constant current output output voltage regulation	$\%V_{OUT}$	5	V_{OUT}=1.0 to 3.0V, R_{EXT}=1.2kΩ, $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$, 1ch output on	—	±0.1	±0.5	%/V
Pull-up resistor	$R_{(Up)}$	3	Test terminal is $\overline{\text{ENABLE}}$	240	300	360	kΩ
Pull-down resistor	$R_{(Down)}$	2	Test terminal is TRANS	240	300	360	kΩ
OOD voltage	V_{OOD}	7	R_{EXT}=200Ω to 12kΩ	0.2	0.3	0.4	V
OSD voltage	V_{OSD1}	7	R_{EXT}=200Ω to 12kΩ	V_{DD} − 1.3	V_{DD} − 1.4	V_{DD} − 1.5	V
	V_{OSD2}	7	R_{EXT}=200Ω to 12kΩ	0.5 × V_{DD}	0.525 × V_{DD}	0.55 × V_{DD}	V
TSD start temperature	$T_{TSD(ON)}$	—	Junction temperature	150	—	—	°C
Return time of normal mode from SHDN mode	t_{ON}	—	Time until output current after it becomes the Normal mode from SHDN mode flows	—	—	30	μs

Switching Characteristics (Unless otherwise specified, V_{DD} = 5.0V ,Ta = 25°C)

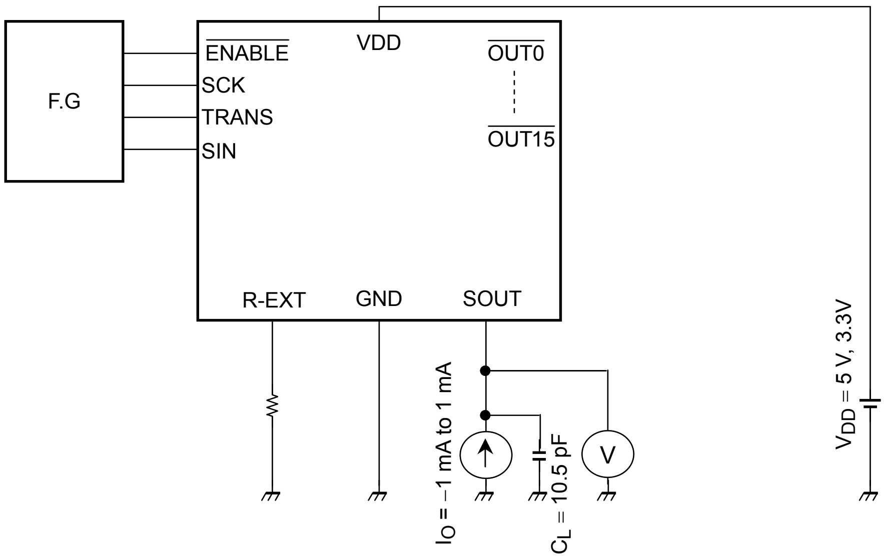
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time	SCK↑-SOUT	t_{PD1U}	6	Up edge trigger mode	6	16	30	ns
	SCK↓-SOUT	t_{PD1D}	6	Down edge trigger mode	2	12	16	
	$\overline{\text{ENABLE}}$ - $\overline{\text{OUTn}}$	t_{PD2}	6	R_{EXT} = 1.2kΩ	—	30	40	
	TRANS- $\overline{\text{OUTn}}$	t_{PD3}	6	$\overline{\text{ENABLE}}$ =“L”	—	30	40	
Output rise time		t_{or}	6	10% to 90% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ voltage waveforms	—	10	20	
Output fall time		t_{of}	6	90% to 10% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ voltage waveforms	—	10	20	
Output delay time		$t_{DLY\ (ON)}$	6	Reference timing waveforms	1	4	9	
		$t_{DLY\ (OFF)}$	6	Reference timing waveforms	1	4	9	

Switching Characteristics (Unless otherwise specified, VDD = 3.3 V ,Ta = 25°C)

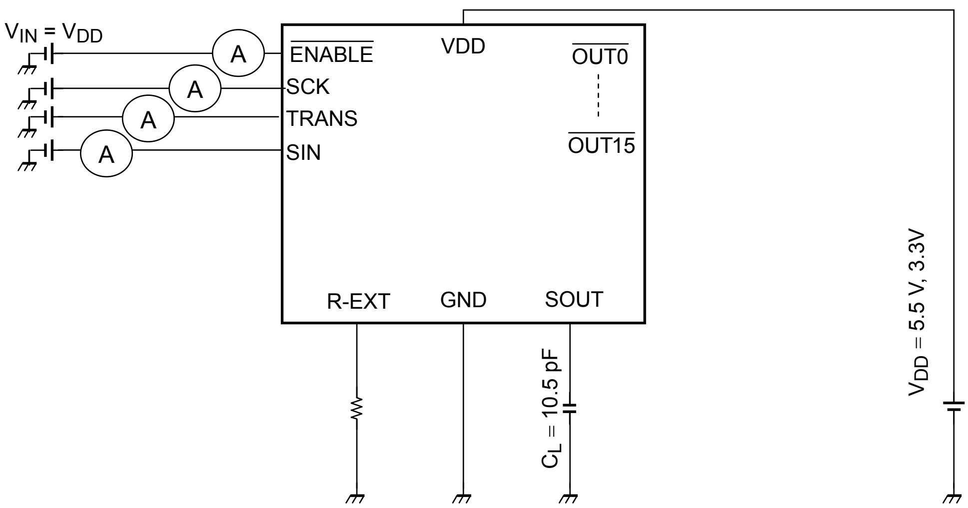
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time	SCK↑-SOUT	t_{PD1U}	6	Up edge trigger mode	6	16	30	ns
	SCK↓-SOUT	t_{PD1D}	6	Down edge trigger mode	2	14	18	
	$\overline{\text{ENABLE}}$ - $\overline{\text{OUTn}}$	t_{PD2}	6	R_{EXT} = 1.2kΩ	—	30	40	
	TRANS- $\overline{\text{OUTn}}$	t_{PD3}	6	$\overline{\text{ENABLE}}$ =“L”	—	30	40	
Output rise time		t_{or}	6	10% to 90% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ voltage waveforms	—	10	20	
Output fall time		t_{of}	6	90% to 10% points of $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ voltage waveforms	—	10	20	
Output delay time		$t_{DLY\ (ON)}$	6	Reference timing waveforms R_{EXT} = 1.2kΩ	2	6	12	
		$t_{DLY\ (OFF)}$	6	Reference timing waveforms R_{EXT} = 1.2kΩ	2	6	12	

Test Circuits

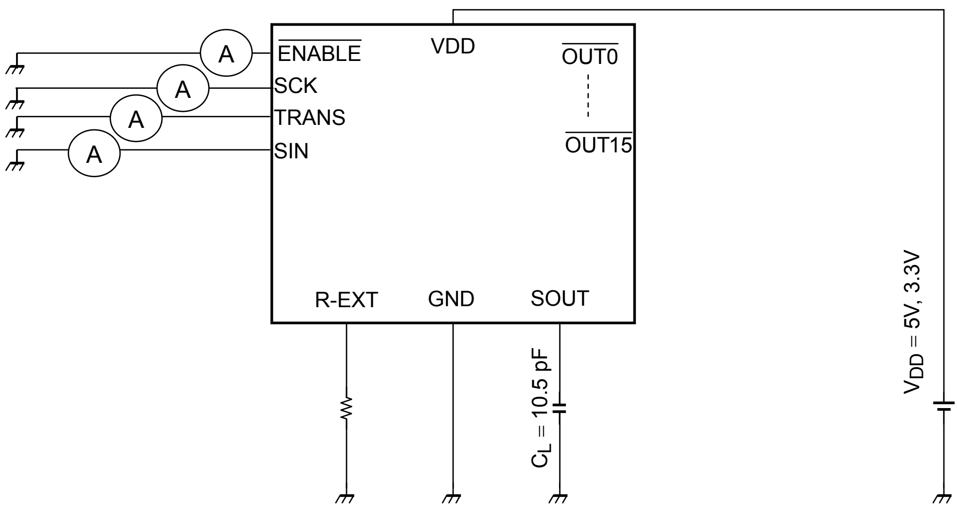
Test Circuit 1: High level SOUT output voltage / Low level SOUT output voltage



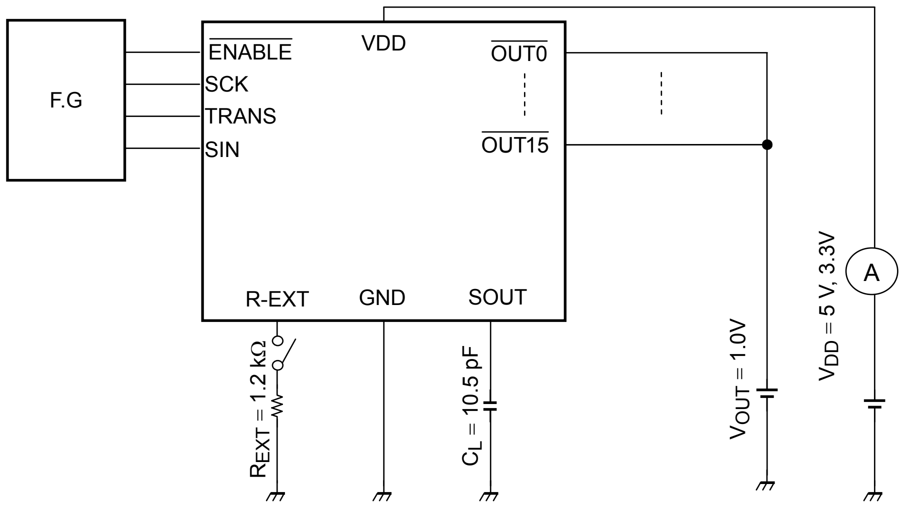
Test Circuit 2: High level logic input current / Pull-down resistor



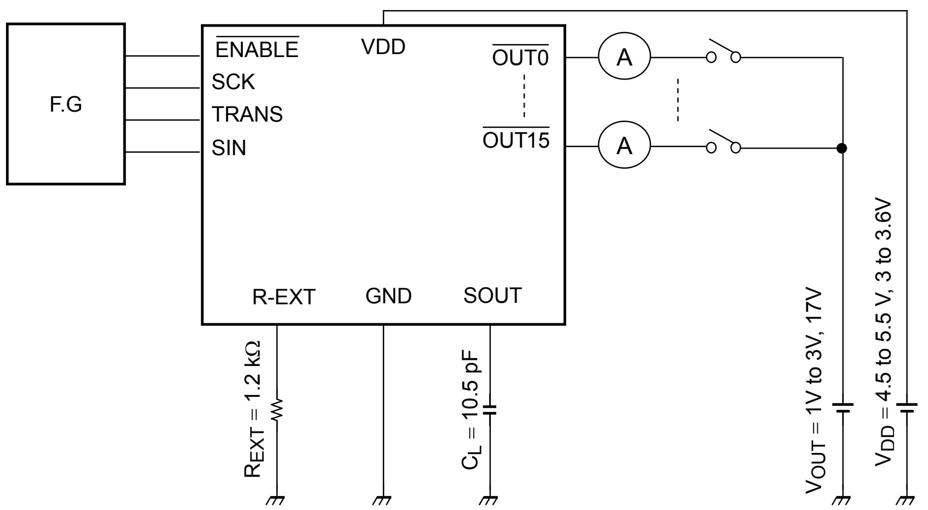
Test Circuit 3: Low level logic input current / Pull-up resistor



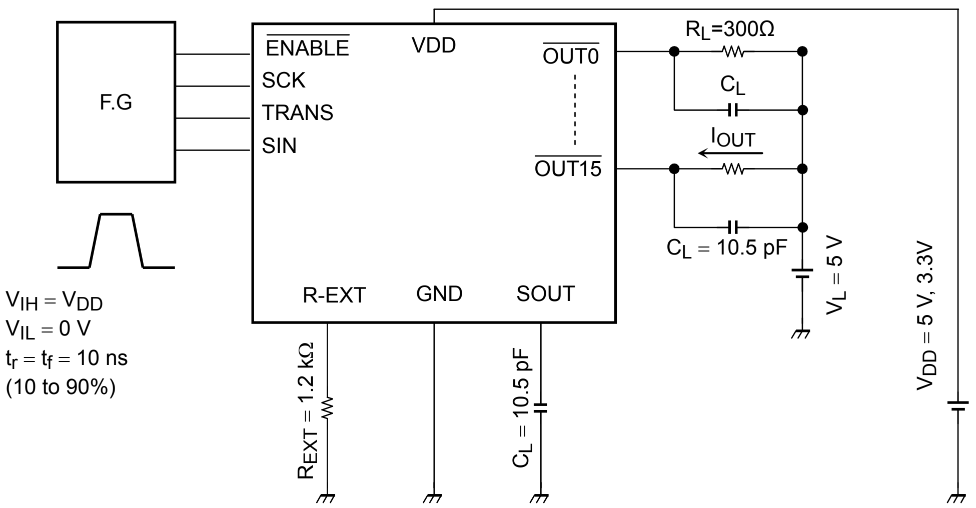
Test Circuit 4: Supply Current



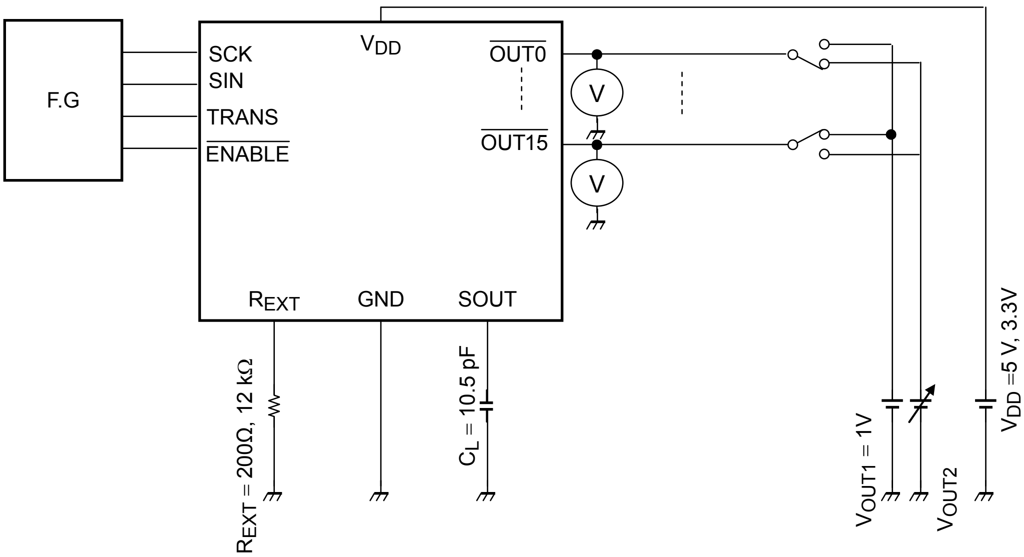
Test Circuit 5: Constant current error(IC to IC) / Constant current error(ch to ch)
Output OFF leak current
Constant current output power supply voltage regulation
Constant current output voltage regulation



Test Circuit 6: Switching Characteristics



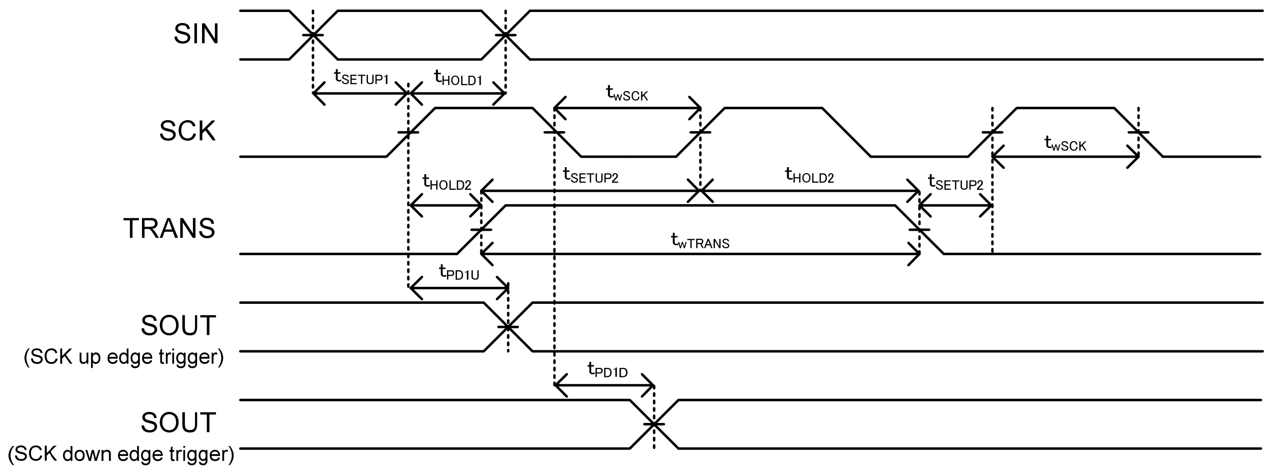
Test Circuit 7: ODD and OSD voltage



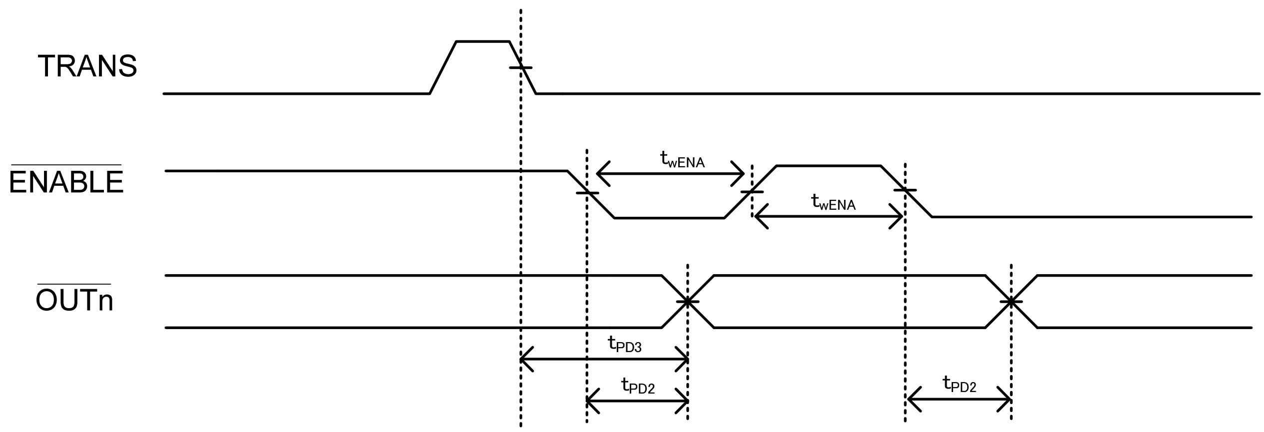
All outputs are configured to be on. One output is connected to V_{DS2}, and the other outputs are connected to V_{DS1}.V_{OOD} and V_{OSD} are measured by changing V_{DS2} and monitoring the other output voltages and error detection results from SOUT.

Timing Waveforms

1. SCK, TRANS, SIN, SOUT



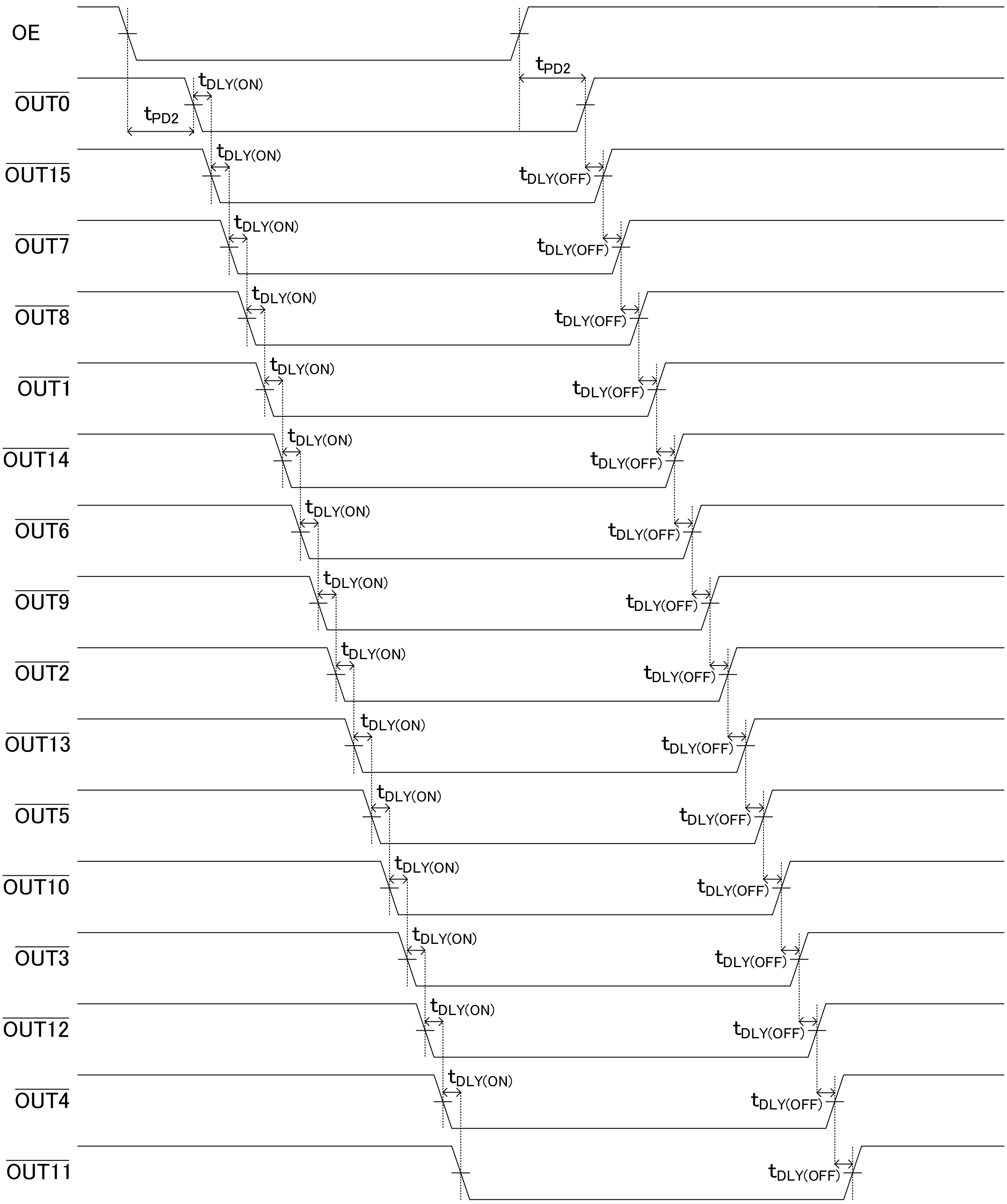
2. TRANS, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



3. $\overline{\text{OUTn}}$

$\overline{\text{OUTn}}$ are Voltage waveform.

4. $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$

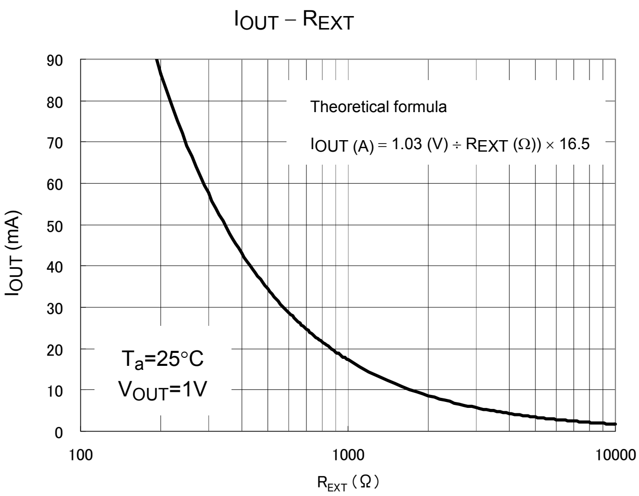


$\overline{\text{OUTn}}$ are Voltage waveform.

Reference data

The above data is for reference only, not guaranteed. Careful evaluation is required prior to creating a production design.

Output Current vs. External Resistor

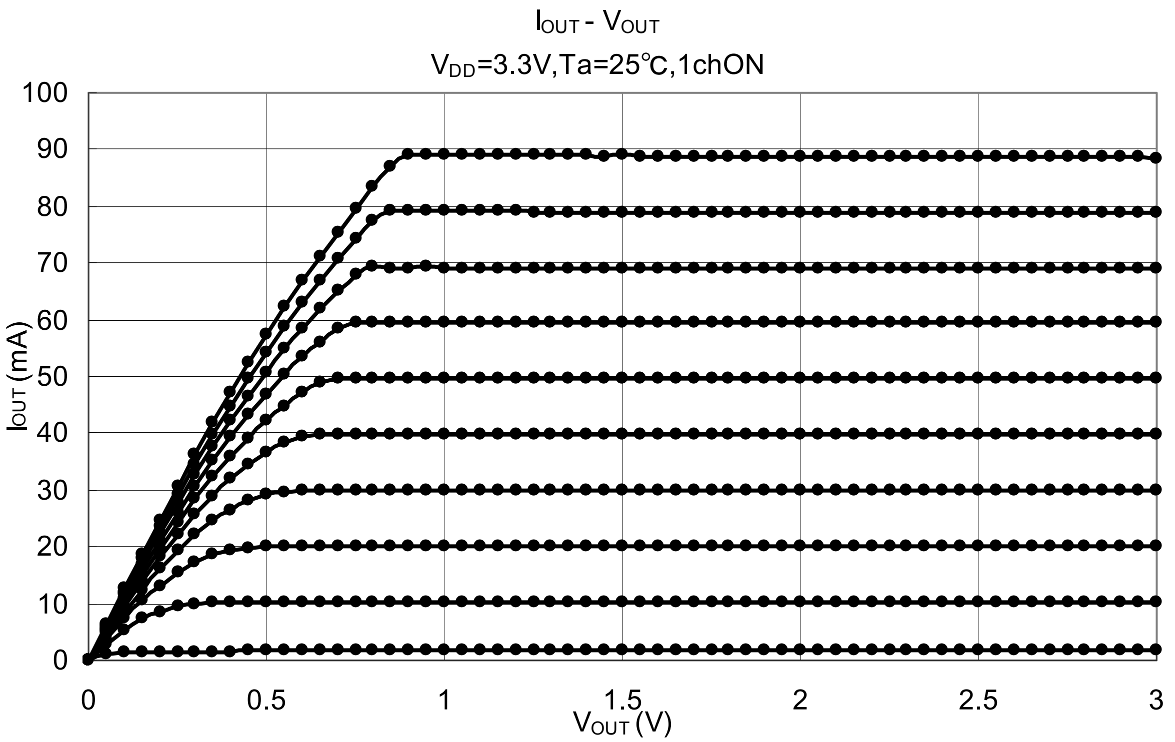


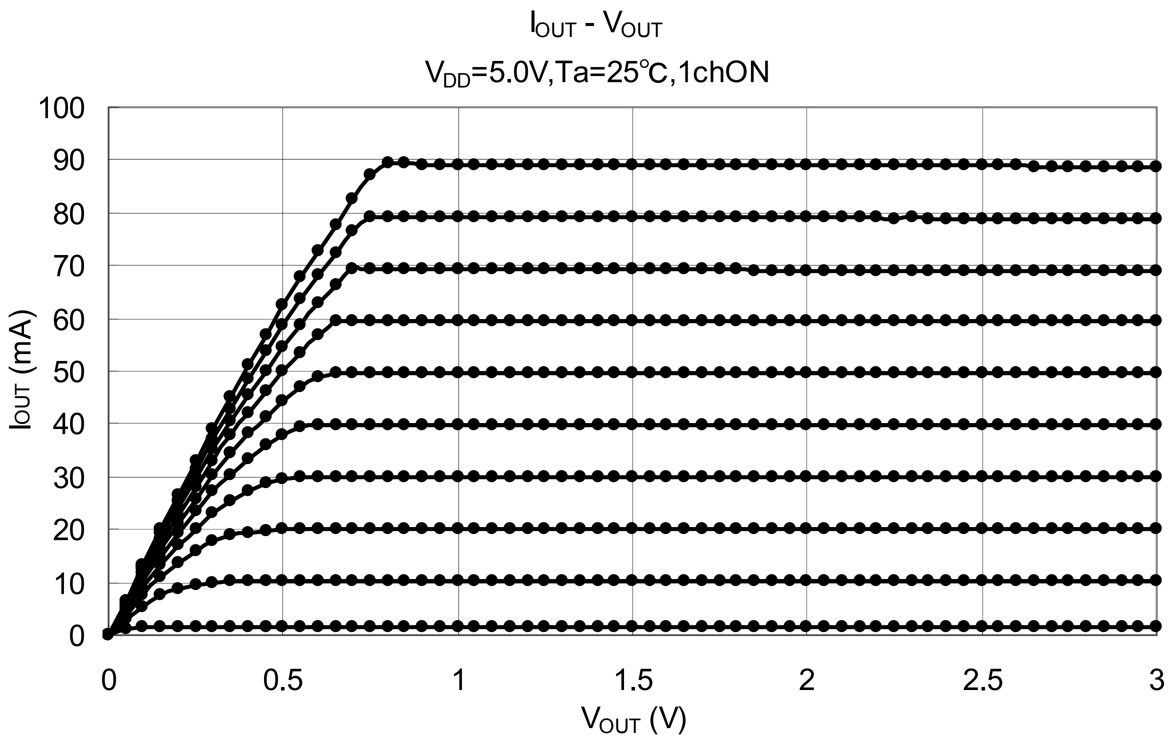
This graph shows the characteristics per channel when all the outputs are on.

Reference data

The above data is for reference only, not guaranteed. Careful evaluation is required prior to creating a production design.

Output current (I_{OUT}) – Output voltage (V_{OUT})





Notes on design of ICs

1. Decoupling capacitors between power supply and GND
   It is recommended to place decoupling capacitors between power supply and GND as close to the IC as possible.

2. Output current setting resistors
   When the output current setting resistors (R_{EXT}) are shared among multiple ICs, production design should be evaluated carefully.

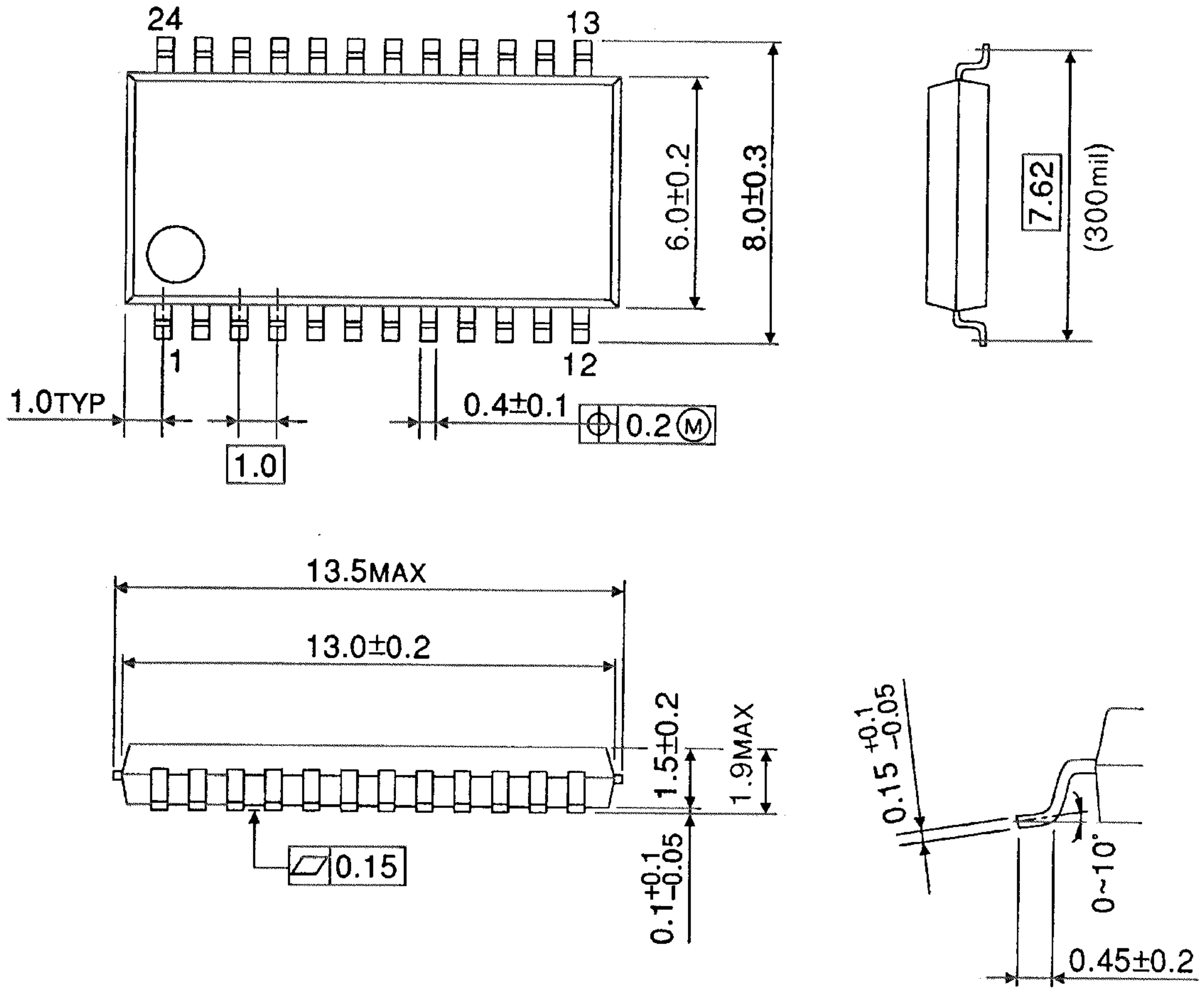
3. Board layout
   Ground noise generated by output switching might cause the IC to malfunction if the ground line exhibits inductance and resistance due to PC board traces and wire leads. Also, the inductance between the IC output pins and the LED cathode pins might cause large surge voltage, damaging LEDs and the IC outputs. To avoid this situation, PC board traces and wire leads should be carefully laid out.

4. Consult the latest technical information for mass production.

Package Dimensions

CFG Type
SSOP24-P-300-1.00B

Unit : mm



Weight : 0.32g Typ.

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

(3) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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