

## SWITCHING REGULATOR APPLICATIONS

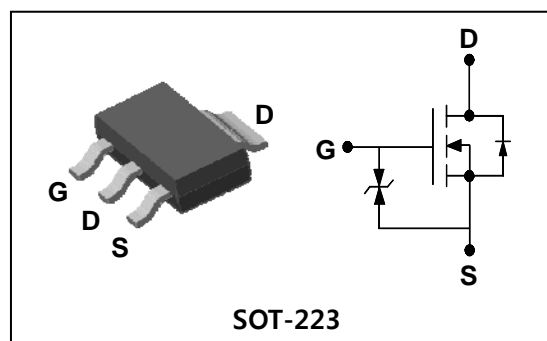
### Features

- High Voltage :  $BV_{DSS}=300V(\text{Min.})$
- Low  $C_{RSS}$  :  $C_{RSS}=3.2pF(\text{Typ.})$
- Low gate charge :  $Q_g=2.9nC(\text{Typ.})$
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=8\Omega(\text{Max.})$

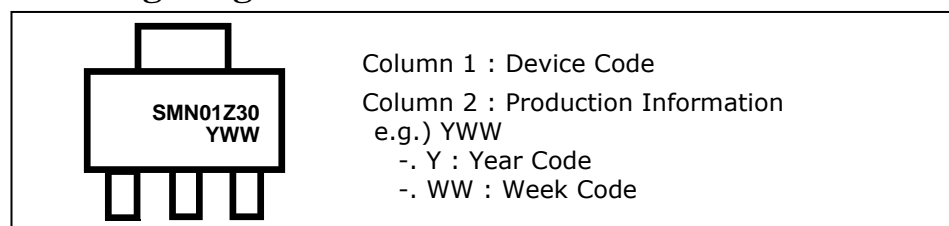
### Ordering Information

Type No.	Marking	Package Code
SMN01Z30Q	SMN01Z30	SOT-223

### PIN Connection



### Marking Diagram



### Absolute maximum ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	300	V	
Gate-source voltage	$V_{GSS}$	$\pm 20$	V	
Drain current (DC) *	$I_D$	$T_C=25^\circ\text{C}$	1.3	A
		$T_C=100^\circ\text{C}$	0.78	A
Drain current (Pulsed) *	$I_{DM}$	5.2	A	
Power dissipation	$P_D$	2.1	W	
Avalanche current (Single) ②	$I_{AS}$	1.3	A	
Single pulsed avalanche energy ②	$E_{AS}$	182.6	mJ	
Avalanche current (Repetitive) ①	$I_{AR}$	1.3	A	
Repetitive avalanche energy ①	$E_{AR}$	0.2	mJ	
Junction temperature	$T_J$	150	$^\circ\text{C}$	
Storage temperature range	$T_{stg}$	-55~150		

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max.	Unit
Thermal resistance Junction-ambient	$R_{th(J-A)}$	-	60	$^\circ\text{C/W}$

## Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	300	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	1.5	2.0	2.5	V
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =300V, V <sub>GS</sub> =0V	-	-	1	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±15V	-	-	±10	μA
Drain-source on-resistance ④	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =650mA	-	6.9	8	Ω
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =650mA	-	0.4	-	S
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V f=1 MHz	-	101	130	pF
Output capacitance	C <sub>oss</sub>		-	15	20	
Reverse transfer capacitance	C <sub>rss</sub>		-	3.2	5.0	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =150V, I <sub>D</sub> =1.3A R <sub>G</sub> =25Ω	-	5	20	ns
Rise time	t <sub>r</sub>		-	17	44	
Turn-off delay time	t <sub>d(off)</sub>		-	21	52	
Fall time	t <sub>f</sub>		-	35	80	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =240V, V <sub>GS</sub> =10V I <sub>D</sub> =1.3A	-	2.9	4.5	nC
Gate-source charge	Q <sub>gs</sub>		-	0.4	-	
Gate-drain charge	Q <sub>gd</sub>		-	0.7	-	

## Source-Drain Diode Ratings and Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	1.3	A
Source current (Pulsed) ①	I <sub>SM</sub>		-	-	5.2	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1.3A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =1.3A, V <sub>GS</sub> =0V dI <sub>F</sub> /dt=100A/μs	-	270	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	0.27	-	μC

## Gate to Source Zener Diode (T<sub>C</sub>=25°C unless otherwise noted)

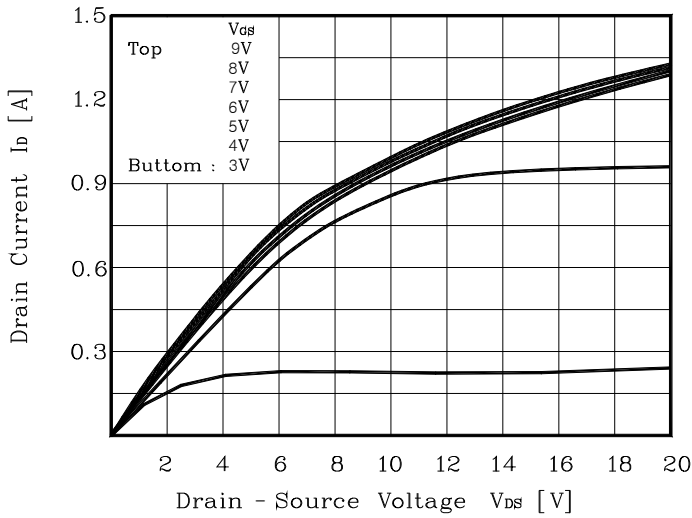
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Gate-Source Breakdown Voltage	±BV <sub>GSO</sub>	I <sub>G</sub> =±1mA, V <sub>DS</sub> =0V	±20	±24	-	V

Note ;

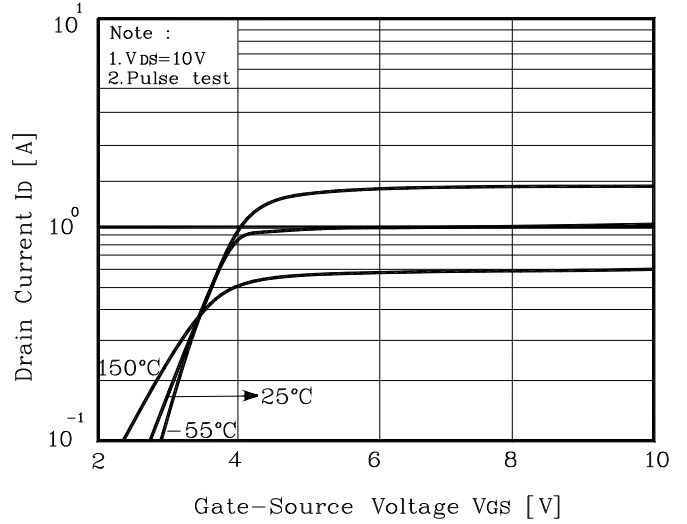
- ① Repetitive rating : Pulse width limited by maximum junction temperature
- ② L=180mH, I<sub>AS</sub>=1.3A, V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25°C
- ③ Pulse Test : Pulse width≤300μs, Duty cycle≤2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

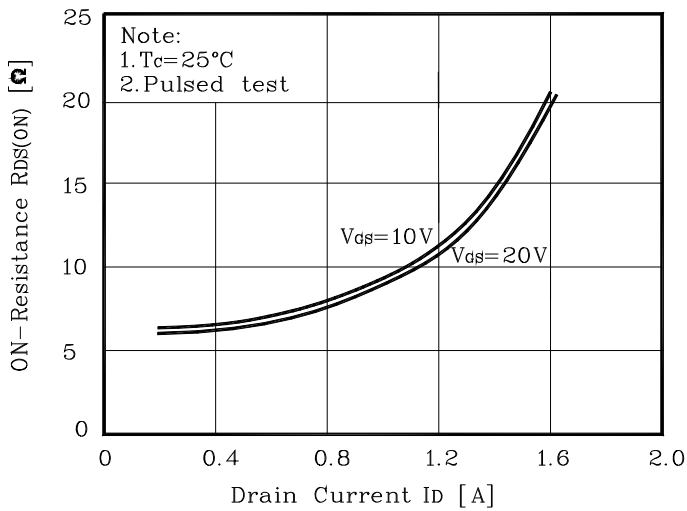
**Fig. 1  $I_D - V_{DS}$**



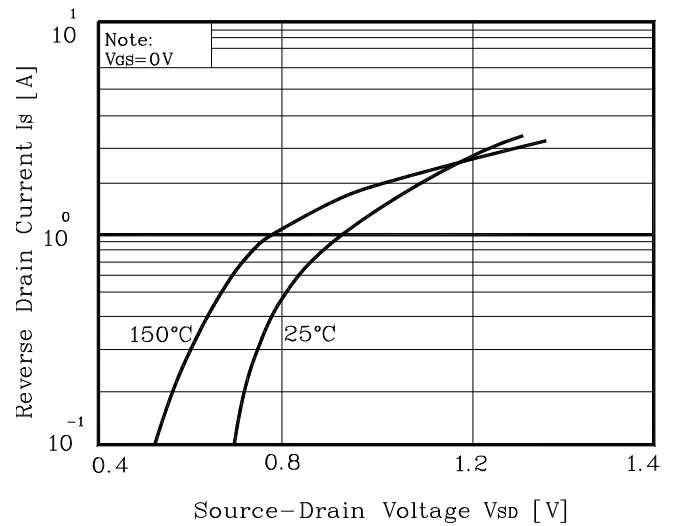
**Fig. 2  $I_D - V_{GS}$**



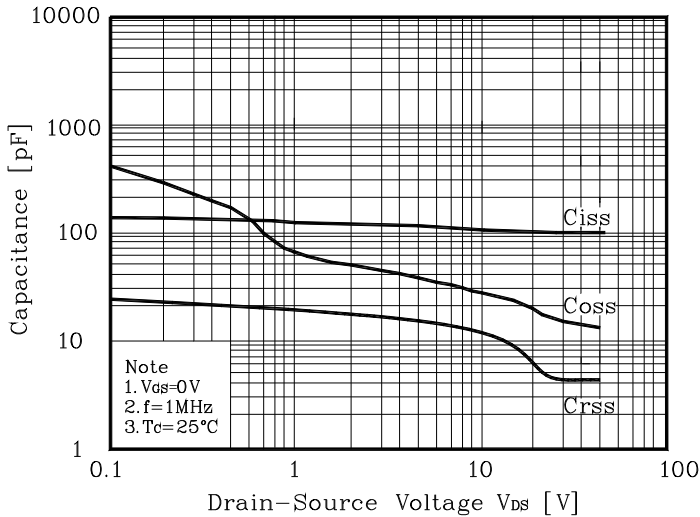
**Fig. 3  $R_{DS(on)} - I_D$**



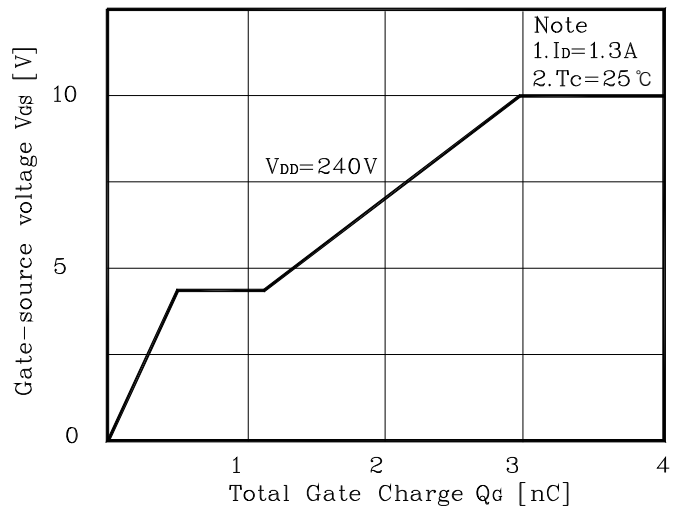
**Fig. 4  $I_S - V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**

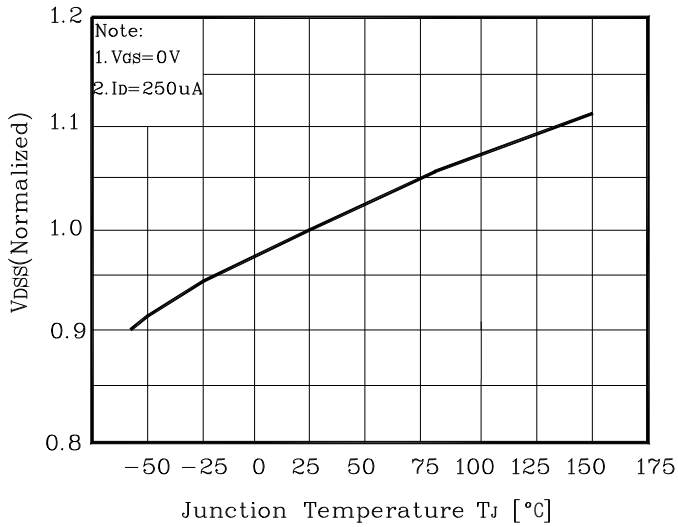


**Fig. 6  $V_{GS} - Q_G$**

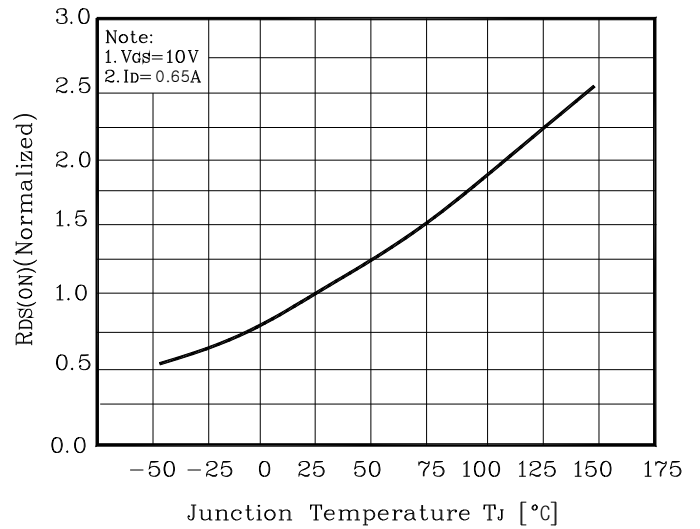


## Electrical Characteristic Curves

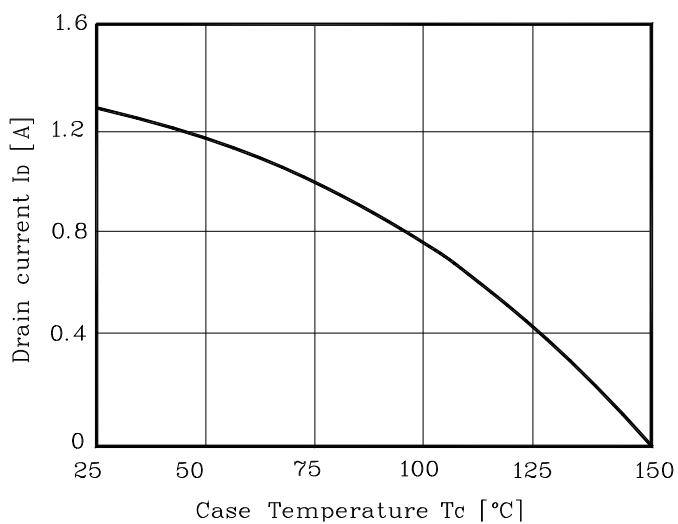
**Fig. 7  $V_{DSS} - T_J$**



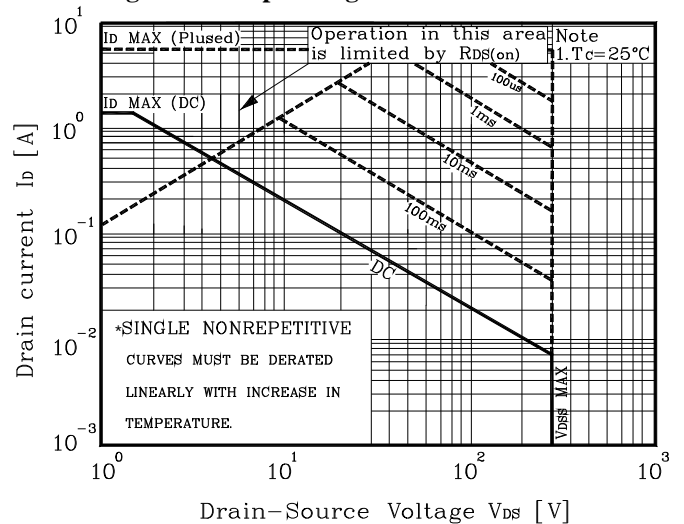
**Fig. 8  $R_{DS(on)} - T_J$**



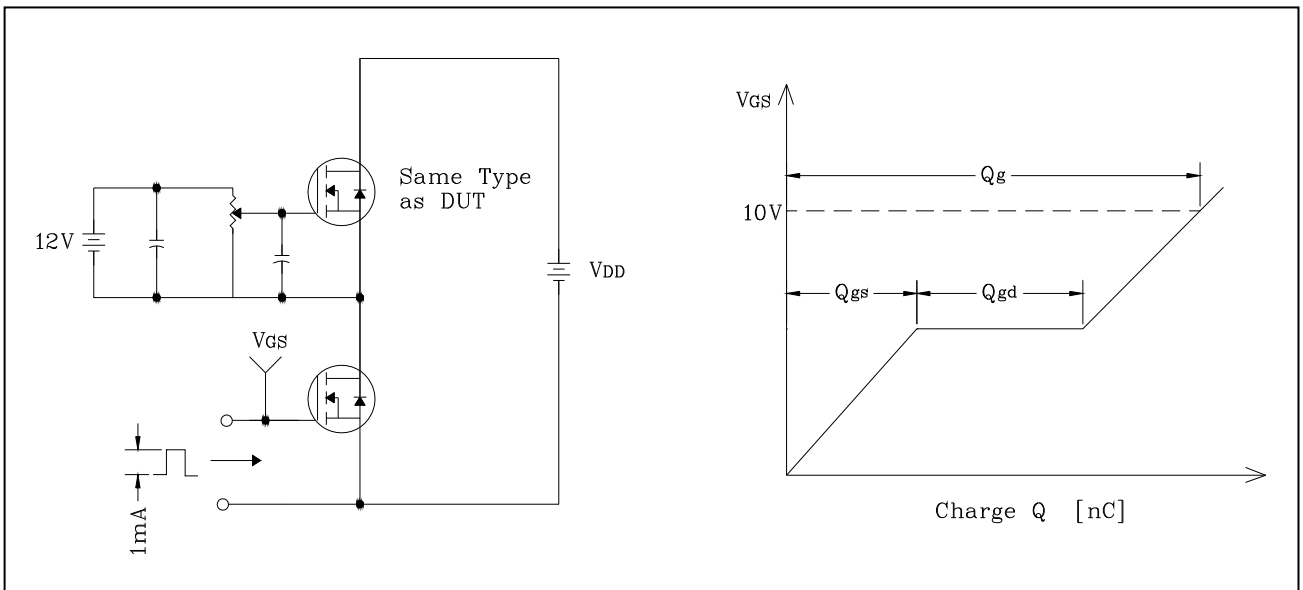
**Fig. 9  $I_D - T_C$**



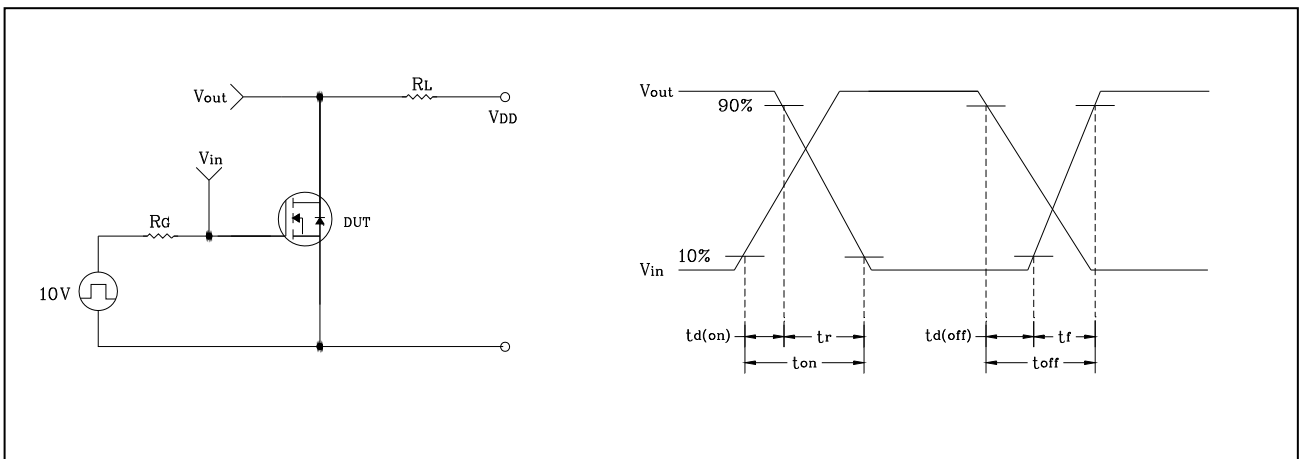
**Fig. 10 Safe Operating Area**



**Fig. 11 Gate Charge Test Circuit & Waveform**



**Fig. 12 Switching Time Test Circuit & Waveform**



**Fig. 13  $E_{AS}$  Test Circuit & Waveform**

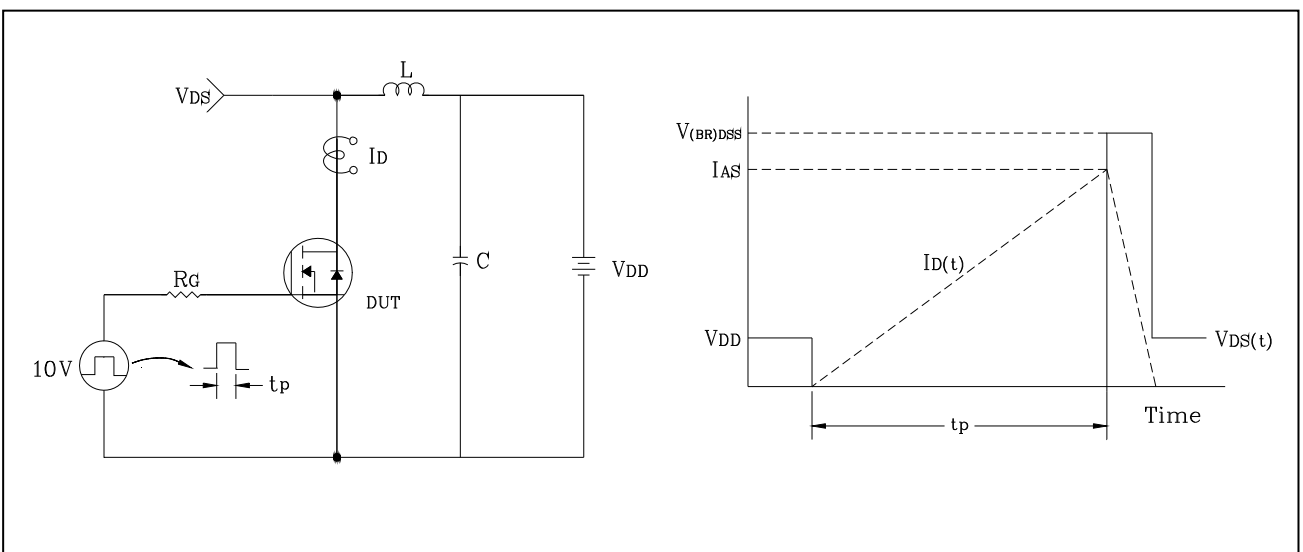
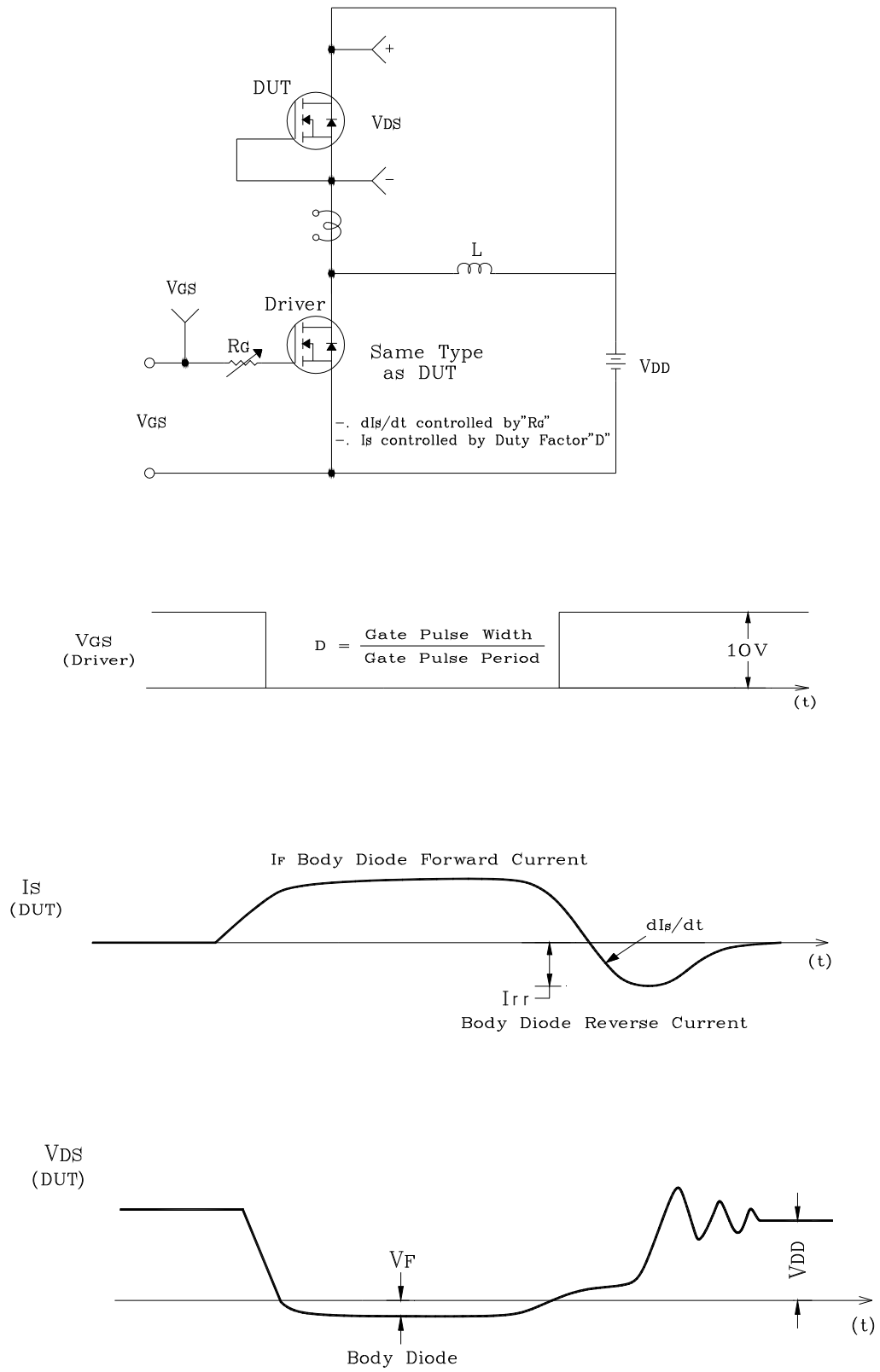
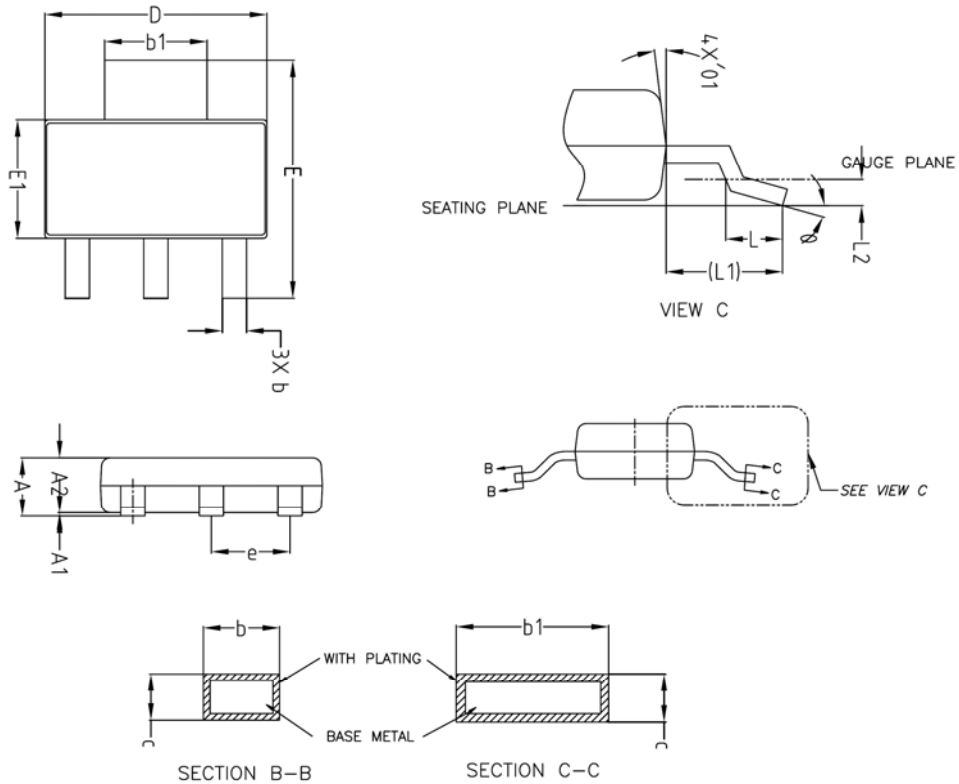


Fig. 14 Peak Diode Recovery dv/dt Test Circuit & Waveform



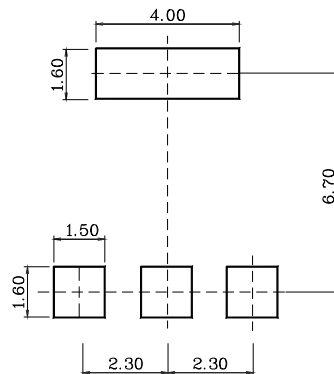
## Outline Dimension

unit : mm



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	—	—	1.80	
A1	0.00	—	0.10	
A2	1.60	1.65	1.70	
b	0.68	—	0.76	
b1	2.95	—	3.07	
c	0.23	—	0.28	
D	6.40	6.50	6.60	
E	6.80	7.00	7.20	
E1	3.40	3.50	3.60	
e	2.30 BSC			
L	0.45	—	0.65	
L1	1.75 REF			
L2	0.10 BSC			
θ	0°	—	10°	
θ1	5°	—	10°	

### ※ Recommended Land Pattern [unit: mm]



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